CSCE 4914/5914: Advanced Digital Design

Catalog Description:
This senior/graduate level course covers all aspects of VLSI design and engineering. The lectures mainly focus on theoretical understanding of CMOS fabrication process; MOS transistors and circuits; Circuit and datapath unit design; Standard cell design and timing characterization; Memory design; Clock tree synthesis; Static timing and power analysis; Floorplanning, placement, and routing; VLSI testing and design for testability.
This course includes a lab session, which introduces standard VLSI design flow and commercial CAD tools. Topics include circuit simulation (Synopsys HSpice), standard cell design (Cadence Virtuoso), logic synthesis (Synopsys Design Compiler), automatic place & route (Cadence Innovus), static timing and power analysis (Synopsys Primetime), DRC and LVS (Mentor Graphics Calibre).
The final design projects go through a complete VLSI design cycle from standard cell design, circuit design, logic synthesis, physical design, and sign-off verification.

Corequisite: Lab component
Prequisite:

- For undergrads: CSCE 2114/ELEG 2904 Digital Design (with an A) **or** CSCE 3953 System Synthesis and Modeling (C or higher) **or** ELEG 3933 Circuits and Electronic (C or higher)
- For graduates: A BS degree in Electrical Engineering, Computer Engineering, Computer Science or equivalent majors

Textbook/required material:
There is no required textbook for this course. Course notes for all lectures will be used. However, the following books are recommended:

- CMOS VLSI Design: A Circuits and Systems Perspective, Neil Weste and David Harris, 2011, ISBN 978-0321547743
- Digital Integrated Circuits: A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Pearson, 2003, ISBN 978-0130909961
- Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, Erik Brunvand, Pearson, 2010, ISBN 978-0321547996

Course objective:
After completing this course, students should be able to do the following:

- Understand the theory and modeling of the basic factors affecting the design: performance, power, area, and cost.
- Design standard cells and properly size transistors
- Design and Layout large scale digital integrated circuits
- Optimize propagation delay in CMOS digital circuitry on an integrated circuit chip
- Use CAD tools to simulate, synthesis, layout and verify VLSI circuits

Topics covered:

- Introduction to VLSI Systems
- CMOS Transistor Theory
- Fabrication, Layout, and Design Rules
- Design and Optimization of Static CMOS Gates
- Design of Flip-Flops, Latches, and Sequential Circuits
- Parasitic Extraction and RC Delay Model
- Clock Generation and Distribution, Static Timing Analysis for Sequential Circuits
- Power Distribution and Dissipation, Static and Dynamic Power Analysis.
- Floorplanning and Placement
- Routing and Timing Closure
- Sign-off Verification
- Datapath Element Design for Synchronous Circuits
- Memory Block Design
- Introduction to Dynamic Circuit and Asynchronous Circuit

Class schedule:
Meets either 3 times a week for 50 minutes or 2 times a week for 1 hour 20 minutes for 15 weeks.

Course Website:

You must check these websites on a regular basis for most up-to-date information!

- Main Website:
  - Including course materials, grades, and reports
  - https://e3da.csce.uark.edu/teaching/CSCE5914
- Blackboard:
  - Used for announcement and assignment submission
  - Make sure to turn on email notifications
  - https://learn.uark.edu/
- Piazza Q&A Forum:
  - Used for FAQs and Student discussion and online participation
  - https://piazza.com/class/CSCE5914

Homework assignments and project:
Homework will be assigned. The final project will be used instead of the final exam.

Grading:
Class Attendance and Participation: 10%
Homework and Labs: 40%
Midterm Exams: 20%
Final Project: 30%

Grading will be regularly updated on the course website. It's your responsibility to check and

report if the posted grades are incorrect.

Only exam grades may be curved. Graduate students may have a higher quality requirement standard. We will use the following scale to assign final grades:

A: [90, 100] B: [80, 90), C: [70, 80), D: [60, 70), F: below 60%

Absences:

You must notify the instructor via email if you are not able to attend a test or will be late with an assignment. You are to notify the instructor **before** the test or assignment due date if at all possible. Excused absences are allowed with a **written** record for illness, death of a family member, and other reasonable emergencies. For student sickness, you can use the course absence form after visiting a doctor or Pat Walker Health Center: http://e3da.csce.uark.edu/teaching/download/class_absence.pdf

Academic Honesty:

As a core part of its mission, the University of Arkansas provides students with the opportunity to further their educational goals through programs of study and research in an environment that promotes freedom of inquiry and academic responsibility. Accomplishing this mission is only possible when intellectual honesty and individual integrity prevail.

Each University of Arkansas student is required to be familiar with and abide by the University's 'Academic Integrity Policy' which may be found at honesty.uark.edu/policy. Students with questions about how these policies apply to a particular course or assignment should immediately contact their instructor.

Emergency Preparedness:

Many types of emergencies can occur on campus; instructions for specific emergencies such as severe weather, active shooter, or fire can be found at emergency.uark.edu. The University of Arkansas has a campus-wide alert system for any hazardous conditions that may arise on campus. To learn more and to sign up: http://safety.uark.edu/emergency-preparedness/emergency-notification-system/

Inclement Weather:

If the university is officially closed, class will not be held. When the university is open, you are expected to make a reasonable effort to attend class, but not if you do not feel that you can get to campus safely. Any changes to due dates or the class schedule will be communicated via email to your uark email address.

Academic Support:

University of Arkansas Academic Policy Series 1520.10 requires that students with disabilities are provided reasonable accommodations to ensure their equal access to course content. If you have a documented disability and require accommodations, please contact me privately at the beginning of the semester to make arrangements for necessary classroom adjustments. Please note, you must first verify your eligibility for these through the Center for Educational Access (contact 479–575–3104 or visit http://cea.uark.edu for more information on registration procedures).

Relationship of course to Computer Engineering Program Student Outcomes:

- (a) An ability to apply knowledge of mathematics, science, and engineering.
- (b) An ability to design and conduct experiments, as well as to analyze and interpret data.
- (e) An ability to identify, formulate, and solve engineering problems.
- (k) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

Relationship of course to Computer Science Program Student Outcomes:

- (a) An ability to apply knowledge of computing and mathematics appropriate to the discipline.
- (b) An ability to analyze a problem, and identify and define the computing requirements appropriate to its solution.
- (c) An ability to design, implement and evaluate a computer-based system, process, component or program to meet desired needs.
- (i) An ability to use current techniques, skills, and tools necessary for computing practices.