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# PowerSynth 2: Automated Power Electronics Physical Design Synthesis With Custom and Heterogeneous Components

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**ABSTRACT** Electronics Design Automation (EDA) has shown significant importance in the power electronics industry. As power electronic circuits become more complex, the traditional trial-and-error approach in physical design becomes less effective and time-consuming. Novel packaging technologies and intelligent physical design automation solutions are crucial to overcome these challenges and produce reliable solutions. PowerSynth 2 is an EDA tool for generating and optimizing power module layouts. To extend the layout synthesis capability beyond power modules, the layout engine needs to consider various custom components such as capacitors, inductors, and gate drivers. This research presents a novel framework for the layout synthesis process in PowerSynth 2 to allow importing user-defined components. The proposed algorithm can effectively generate a Power Electronics layout by introducing a hierarchical framework for custom components and pin pads. It will extend the physical design process to broader design types, such as converters and server boards. Examples of converter designs are tested, demonstrating the efficiency and scalability of the proposed design tools.

**INDEX TERMS** Heterogeneous integration, layout optimization, physical design automation, power converters, power electronics.

## I. INTRODUCTION

The growing demand for silicon carbide (SiC) devices, alongside the advent of new technologies like gallium nitride (GaN) in sectors such as electric vehicles (EVs), renewable energy sources including solar and wind, smart grids, and data centers (DCs), underscores the urgent necessity for Power Electronics Electric Design Automation (PE-EDA). The power module layout generation and optimization have been proposed and researched along with the development of industry design tools [1]. The traditional physical design is heavily relying on human experiences with tedious efforts. The best layout is usually manually chosen after hundreds of error-and-try iterations. This process is time-consuming, even with a limited choice of candidate layouts [2]. However, the design process for advanced power converters is increasingly tricky with various heterogeneous components and multiple device and trace layers compactly stacked in a 3D structure with various types of interconnections.

The research on the PE-EDA has emerged recently. First, researchers focused on the power electronics circuit parameters design, such as power loss, selecting the optimal components, and finding the optimal frequency, efficiency, and power density. An AI-assisted design method is proposed for optimizing the parameters design of power converters in [3]. They used a data-driven model for power losses and ripples. In addition, Genetic Algorithm (GA) is used for optimal design parameters with optimal efficiency. An ANN-based design approach is proposed to enhance the design performance of wide-bandgap power electronics converters in [4]. The approach generates optimal designs on the efficiency-power density Pareto-front curve. In [5] the authors advocate for design automation in power electronics, addressing three key challenges in designing converters

for harsh environments. It includes accessible component databases, automated collaboration between circuit and finite element simulations for co-design, and a hierarchical, exclusion-based workflow to reduce computationa demands.

The second focus is power converter physical design synthesis, verification, and fabrication. In [6] the authors introduced an iterative automatic layout design workflow for power electronics PCB design based on the Genetic Algorithm (GA). The layout design process consists of two design steps. The first step involves a GA-based layout generation loop. After several iterations and selections, the best layout candidate that meets the user-defined objectives will go through the second step of layout optimization, which involves copper pouring to guarantee a reasonable layout design with thermal stability. In [7] a graph model is proposed to describe heterogeneous layouts with all interconnectivity and design constraints. Initially, a graph model is constructed to represent heterogeneous layouts while preserving all interconnectivity and design constraints. Utilizing this model, integer programming is employed to create layout templates featuring variable geometric topologies. Subsequently, in conjunction with a self-developed discrete extractor, the Pareto front is derived using a genetic algorithm, which establishes a trade-off boundary for loop inductance and branch mismatch. Another research [8] established a Multi-Objective Electro-Thermal design framework utilizing NSGA-II for the optimization of chip layouts in power modules. The parasitic inductance and thermal resistance are both subjected to numerical analysis using the same multiphysics simulation model based on finite element methods. A combination of a GA and a Dijkstra algorithm is proposed to generate different PCB layout designs [9]. In this research, the device location is constant, and routing is optimized by the proposed method to minimize the inductance loop.

The principles of PCB layout design are rooted in foundational research on signal integrity [10] and EMI/EMC mitigation [11], which highlight the importance of controlled impedance, effective ground plane strategies, and minimizing loop areas. Industry standards, along with studies on thermal management [12], [13], focus on manufacturability and heat dissipation. However, the process of generating layouts currently lacks an automated synthesis and optimization approach, relying instead on manual calculations and the use of various tools for electrical, thermal, and reliability assessments.

Numerous design strategies from conventional VLSI physical design processes can be adapted to enhance the automatic layout design of power modules. However, these algorithms cannot be directly applied to power electronics designs since the design characteristics and optimization targets are fundamentally different. The lack of industrial standard and public benchmark designs makes it even more challenging to design a generic EDA flow. With much fewer devices but more heterogeneous types of design components, power electronics exhibit different dimensions of physical design, layout optimization, and EDA algorithm space which deserves to be explored with care.

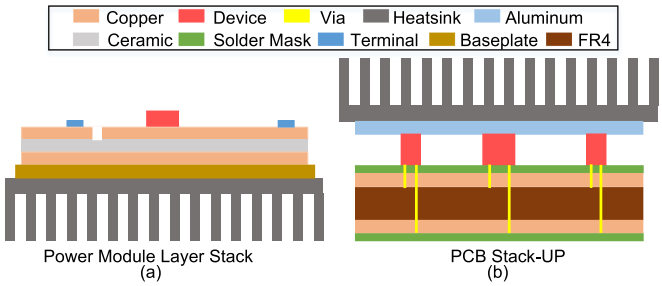


**FIGURE 1. Layer stack of (a) DBC power module and (b) PCB power converter.**

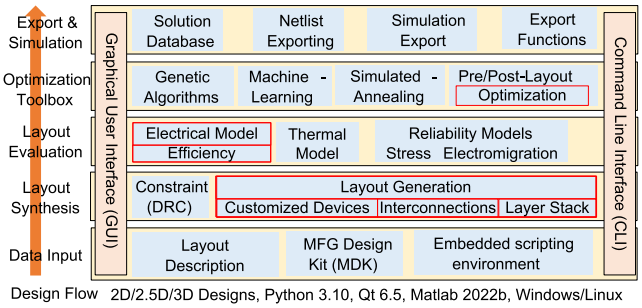


**FIGURE 2. PowerSynth 2 architecture (v2.2) with new modules in this paper highlighted.**

PowerSynth Evolution: The foundational work in [14] introduced "Power-CAD," a concurrent electrothermal optimization approach for discrete power modules. After that, the "PowerSynth v1.4" EDA tool for optimizing multi-chip power modules (MCPMs) was launched in [15]. PowerSynth v1.4 features rapid, precise, hardware-validated electrical and thermal models within a multi-objective optimization framework. To optimize and validate the 2.5-D CAD workflow in PowerSynth v1.9 [16], a hierarchical corner stitching data structure combined with a computational geometry evaluation technique is utilized. PowerSynth 2 is the state-of-the-art tool for MCPM layout optimization, which uses the hierarchical corner stitching (CS) data structure with a constraint graph (CG) technique to generate and optimize the MCPM layouts [17] including 2D PCB design and 2.5D/3D power modules, shown in Fig. 1. In traditional EDA algorithms compaction is a primary criterion for physical design. In contrast, Power Electronics takes into account both compaction and expansion to enhance electrical and thermal performance in physical design. Consequently, optimizing the physical layout is essential for power electronics. PowerSynth 2's architecture, shown in Fig. 2, includes built-in algorithms, methodologies, and modeling techniques, with both graphical and command-line interfaces for compatibility with Windows and Linux [18].

Currently, PowerSynth v2.1 supports built-in devices like bare die SiC MOSFETs and diodes but lacks support for

custom device types. Modern power electronics design, requires a variety of components, including passive elements (Capacitors, Inductors, and Transformers), GaN HEMTs, gate drivers, and user-defined components. This study introduces a new hierarchical layout structure to enhance PowerSynth 2 for optimizing custom components in power converter layouts. Additionally, a multi-objective electro-thermal optimization approach is presented for generating these layouts. This positions PowerSynth as a CAD tool capable of simultaneously optimizing power converter parameters and generating layouts. Compared to generic PCB editor tools like Altium Designer, PowerSynth is a layout synthesis tool that can be integrated with various models and optimization frameworks to generate layouts based on the designer's preferences. With increasing design complexity, layout engineers need dedicated power electronics design tools and models for more accurate analysis in terms of efficiency, electrical, thermal, and reliability.

In this paper, we present PowerSynth v2.2 with our key contributions include: (1) A hierarchical framework for handling custom components; (2) A new layout synthesis framework for power converter and PCB designs; (3) Extending the device types to allow user-define components for power converter designs; (4) An integrated multi-objective electro-thermal optimization. The paper provides an overview of PowerSynth 2, discusses the limitations of the current layout engine for converter design in Section II. Section III outlines the design methodology and algorithms used for layout synthesis to cover a broad range of power electronics design types. Section IV explains the proposed method by a power module design with a custom device. Section V examines two case studies in detail: a boost and a buck converter, and a runtime comparison and potential future applications are mentioned in Section VII.

## II. POWERSYNTH 2 OVERVIEW

### A. LAYOUT REPRESENTATION ALGORITHMS

PowerSynth 2 uses hierarchical CS and CG for layout representation which are briefly described in the following [17]. The layout engine offers three modes of layout generation: minimum-sized layout (Mode-0), variable-sized layout (Mode-1), and fixed-sized layout (Mode-2). Currently, the layout engine can handle 2D, 2.5D, and 3D Manhattan layouts with integrated heterogeneous design of power modules.

*Corner Stitch:* The data structure [19] represents a planar layout with non-overlapping tiles of two types: empty and solid. Each tile has four pointers to traverse neighbor tiles. There are two variants: horizontal corner stitch (HCS) and vertical corner stitch (VCS). The algorithms for creating corner-stitched planes are efficient, making them suitable for power module layout representation.

*Constraint Graph:* A graph represents inequality relationships between vertices using edge weights as minimum constraint values. Each corner-stitched tile is converted into two vertices in the graph, connected by an edge with a minimum constraint value. There are two types of constraint graphs: horizontal (HCG) and vertical (VCG). The HCG ensures minimum relative horizontal location among components, while the VCG maintains minimum relative vertical location.

### B. LAYOUT SYNTHESIS PROCESS

PowerSynth has a multi-objective optimizer that can generate layouts based on objective functions. To perform such optimization, PowerSynth considers electrical and thermal models as objective functions for power module layout optimization. The electrical model measures the electrical parasitics such as loop inductance, resistance, and capacitance. On the other hand, the thermal model obtains the maximum temperature of the power modules.

### C. CURRENT LAYOUT ENGINE LIMITATIONS

Currently, PowerSynth 2 layout engine is designed for power modules. In addition, it uses pre-defined devices such as bare-die SiC MOSFETs and Diodes, assuming a pre-defined vertical device structure. Although its algorithm design framework is generic, many built-in assumptions regarding dimensions and design constraints are considered in the current implementation. To address the limitation with custom-designed devices, we introduced a novel concept for the definition of arbitrary components and added a new hierarchical level for components in the layout engine. This new idea enhances the layout engine for power modules, power converters, and other PCB designs.

Fig. 1(a) illustrates the Power Module layer stack structure. From the bottom, a heatsink is placed for thermal management, and on top of that, a direct bond copper (DBC) substrate, which consists of one ceramic layer between two copper layers, is considered. On the other hand, Fig. 1(b) shows a PCB 2-layer stack-up structure that is considered for power converter baseline. For simplicity, the heatsink is modeled on the top of the PCB on the devices. After the device layer, the solder mask layer is considered to protect the trace layer. Then, the copper layer for routing is followed by FR4. After that, the second trace layer and solder mask layer are placed. All material's thermodynamics specifications, such as heat conductivity, heat capacity, and density, along with dimensions and boundary conditions, are considered for thermal evaluation. It is noted that, due to the modular structure in PowerSynth 2, users can define arbitrary layer stack structures for both the Power Module and Power Converter design.

## III. DESIGN ALGORITHMS AND METHODOLOGY

Power Converter's layout design process is different compared to power modules. The Power converter design process deals with large and bulky components, large component numbers, and multiple PCB layers. In addition, different design and optimization objectives can be considered compared to power modules. In this section, design challenges and constraints, algorithms, and performance models are elaborated in detail through an example.

**Algorithm 1:** The PowerSynth2 High-level Design Flow.

```
Read the the information and each hierarchical level
Create a root node and sub-nodes of the structure
Create a virtual interface layer
for each layer do
    Perform Component Representation algorithm
    Perform bottom-up constraint propagation
Evaluate components location & size at root node
Propagate shared locations to sub-nodes
for each layer do
    apply top-down components location & size
      propagation
```

**Algorithm 2:** Custom Component Representation Algorithm.

```
for each device do
    Define a new hierarchical level
    Create Hierarchical HCS and VCS
for each tile of HCS/VCS do
    if the layer is the component layer then
        Determine the Component ID
        Load the corresponding component footprint
        Create a vertex and an fixed edge for the tile
        Set the edge weight by Component footprint
    else if layer is the trace layer then
        Create the edges based on design constraints
Create HCG and VCG by vertices and edges
Evaluate the HCG and VCG
```

### A. DESIGN CHALLENGES WITH HETEROGENEOUS INTEGRATION

There are several critical design challenges and constraints for the layout engine in processing PCB designs and power converter layouts. (1) The pins must be relative to the device's origin while allowing device movement and rotation. (2) The device and pin connectivity should be preserved during the layout optimization. (3) The device may overlap with the trace while its volume must not collide with another. (4) Trace layers should be updated based on the location and orientation of the device. (5) In a multi-layer design, the connectivity between the device and the corresponding layer should be preserved during layout optimization.

To overcome these challenges, we introduce two layers for device layout: the component layer and the trace layer. In the component layer, the component location and footprint are defined in the input layout template. Further, the trace layer maintains connectivity information for device pins, while the pin location is determined from the component database. For layout optimization with custom devices, we proposed a component representation framework based on the structure of the current layout engine in PowerSynth. In previous work, the device was only considered as a simple box without any dependencies. In this work, we added a new hierarchy for custom components into the layout engine to allow device pin and volume management.

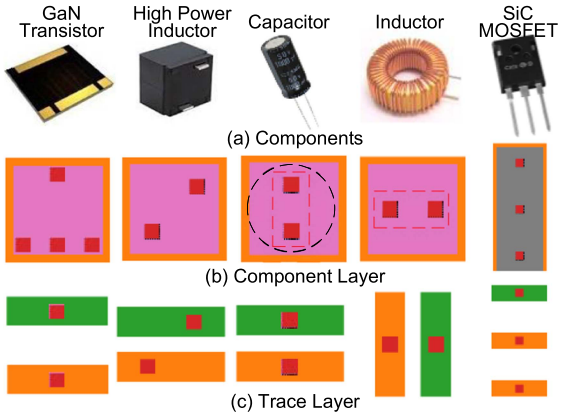


**FIGURE 3.** Power converter components and representation in the new engine.

### B. GENERIC LAYOUT REPRESENTATION

Fig. 3 illustrates some commonly-used components in the power converters and their representation in the updated layout engine. Fig. 3(b) and (c) show the component and trace layer respectively. For 2-pin components such as capacitors, the corresponding device area and pins area are shown. Due to the Manhattan layout engine, the round footprint is converted to a square to represent its occupied space. For inductors, the footprint is a rectangle, while its pins are modeled as squares. This method is like 3-pin components such as MOSFET and half-bridge power modules.

Fig. 4 shows the proposed method for a 3-pin power device. Fig. 4(a) shows the vertical corner stitch (VCS) and the horizontal corner stitch (HCS). In contrast, Fig. 4(b) shows the initial and final VCGs and HCGs corresponding with VCS and HCS of the component respectively. E1 and E2 are enclosure rules, and S1 and S2 are spacing rules between the pins. $L_P$ and $L_D$ are the lengths of pins and the components, respectively. A CG graph consists of vertices and edges G (V, E). Every CG has four types of vertices. Firstly, there are the source vertex and the sink vertex. Then, the independent vertex has a fixed minimum location but no maximum location. Finally, the dependent vertex has a fixed distance to an independent vertex. In addition, in a CG, there are usually two types of edges: Self-edges are generated from the corresponding corner-stitched tile, and propagated edges are derived from the lower-level constraint graph. In the component layer, the edge weights come from the device footprint. From Fig. 4(a), the final VCG shows that the Y1-Y6 vertices become dependent vertices, and the edges become fixed edges. The same process is carried out on HCG.

### C. HETEROGENEOUS COMPONENT REPRESENTATION

Algorithm 1 shows the workflow of generating a layout solution. After reading the input information and component database, the root node and sub-nodes will be created. Then,

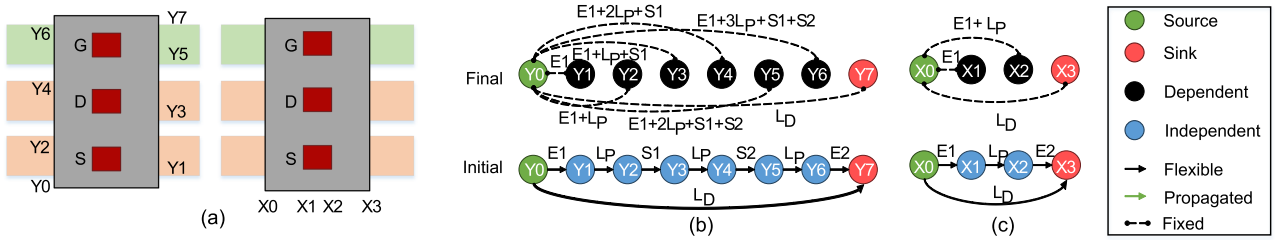


**FIGURE 4.** Component representation with 3 pins (MOSFET) (a) VCS, and HCS. (b) VCG, (c) HCG.

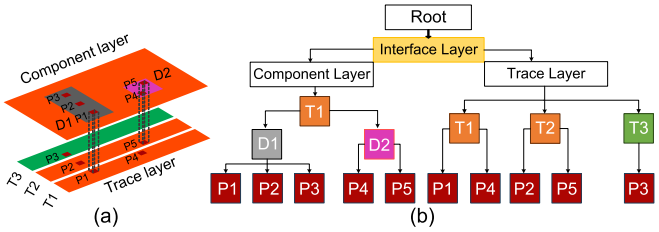


**FIGURE 5.** (a) Multi-layer multi-device example structure and (b) its hierarchy.

a virtual interfacing layer is inserted to connect pins between the component and trace layers. Next, the edge handling algorithm is applied to layers, and the bottom-up constraint propagation is performed on each layer until the root node receives all essential constraints. After that, the location and size of components at root node and sub-nodes will be evaluated. Finally, top-down location propagation is applied to each sub-node to determine the location and size of each component.

The detailed implementation of the process of component representation algorithm is shown in Algorithm 2. First, for each device in the component layer, the HCS and VCS are created based on a new hierarchical level. Then, for each tile of HCS/VCS in each layer, the component ID is determined in the component layer. A fixed edge is created based on its footprint, while a vertex is created based on the coordination. Design constraints, such as trace width and space between traces, are used for edge weights. After that, HCG and VCG are evaluated. This new hierarchical framework allows users to define their custom components with arbitrary pin shapes and numbers, bringing PowerSynth scalability and flexibility with heterogeneously-integrated custom components. For example, in power converter design, users can define their power modules instead of commercial ones.

## IV. LAYOUT EXAMPLE RESULTS

### A. SAMPLE LAYOUT STRUCTURE

To demonstrate the proposed method, a multi-layer multi-device sample structure and the corresponding hierarchical layout description are shown in Fig. 5. The structure consists of two layers and two components: A 3-pin device and a 2-pin device. The upper layer is the component layer, and the bottom layer is the trace layer. From Fig. 5(b), T1 is within the component layer while being the parent of components D1 and D2. Based on the new hierarchy level inside components,

**Algorithm 3:** Multi-Objective Optimization.

```
Generate initial population randomly
for each population do
    evaluate the electrical model and extract components' power dissipation
    evaluate the thermal model using the power dissipation
    Evaluate and find the best solution
while Maximum Iteration is not met do
    Generate new solutions based on the existing ones
    for new solutions do
        evaluate the electrical model and extract components' power dissipation
        evaluate the thermal model using the power dissipation
    update the best solution
Create the Pareto Front from the best solutions
```

D1 is the parent of pins P1-P3, and D2 is the parent of pins P1 and P2. On the other hand, in the trace layer, T1-T3 are the parents of the P1, P4, and P2, P5, and P3, respectively.

Fig. 6 illustrates the computed CGs for this sample structure. Fig. 6(a) and (b) show the initial and final VCG for the 3-pin device and 2-pin device with edges derived from the corresponding corner stitch tiles. All device-related edges in the final VCG are defined as fixed edges. All vertices Y1-Y6 at D1 and Y1-Y4 at D2 are dependent nodes due to fixed edges. Similarly, Fig. 6(c)–(e) demonstrates the same process for the trace layer, with CGs used for T1, T2, and T3, respectively. Once all the necessary constraints are propagated to the root node, the graphs are ready for evaluation and layout generation.

This suggested approach presents a universal framework for 2D/2.D, and 3D design, emphasizing the importance of vertical interconnections and the alignment of layers. Furthermore, this concept facilitates the straightforward application of heterogeneous component integration within the same layer.

### B. POWER CONVERTER LAYOUT EVALUATION

The solutions generated by PowerSynth are evaluated using both electrical and thermal models. In this study for Power Converter design, we introduced a coupled multi-objective electric-thermal assessment.

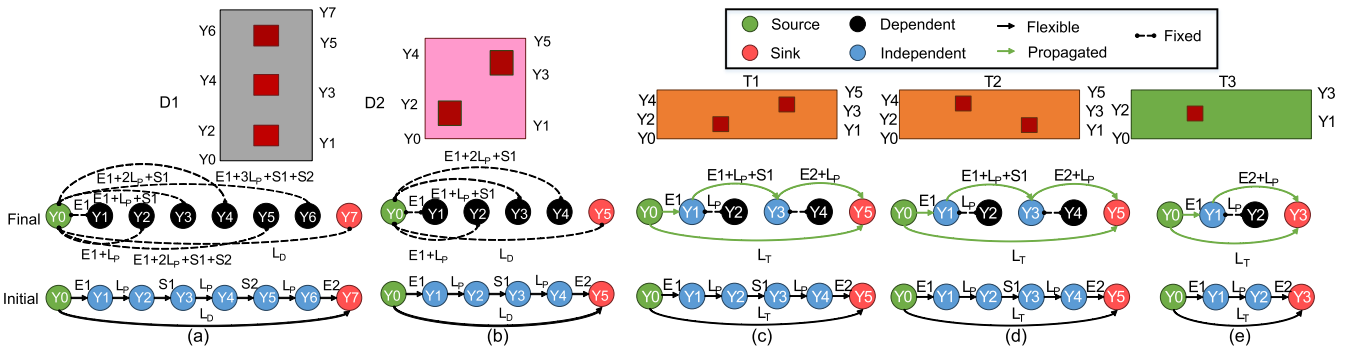


**FIGURE 6.** The initial and final VCG of (a) D1 and (b) D2 (c) T1, (d) T2, (e) T3 .

*Electrical Efficiency Model:* In Power Module design PowerSynth uses a build-in partial element equivalent circuit (PEEC) model and FastHenry for electrical assessment [20]. For power converter design, two criteria should be considered: efficiency and parasitic parameters. Parasitics in the design of power converters encompass the resistances, inductances, and capacitances that are intrinsic to actual components and circuit configurations. These parasitic elements have a considerable influence on the performance, efficiency, and reliability of the system. Typically, the parasitics associated with circuit layouts are significantly smaller than those of the components themselves. In this research focused on optimizing converter layouts, we analyze the parasitics of the devices in relation to those of the circuit layouts, particularly in terms of efficiency as represented in an electrical model. In this paper, the efficiency of the converter that involves parasitics of the devices used as the main electrical optimization objective. Additionally, one effective strategy for mitigating parasitics involves careful component selection. The component selection process and parameters introduced in [21] can be used to optimize efficiency and power density by implementing Monte Carlo Simulation (MSC). Efficiency can be defined as $(P_2 + Losses)/P_2$, in which $P_2$ is output power, and *Losses* is the sum of the component's power loss such as MOSFET, Inductor, Diode, Capacitor, and other devices. After the electrical assessment based on the converter type, the value of power loss of each component is used for the thermal model evaluation.

Electromagnetic Interference (EMI) is a significant issue in the design of power converters, particularly as switching frequencies rise to achieve greater efficiency and compactness. EMI is generated by the rapid fluctuations of voltages and currents, producing high-frequency noise that can interfere with nearby electronic devices or breach regulatory requirements. The frequency is a crucial factor in both the creation and reduction of EMI. In this research, the frequency is within the kHz range, and therefore, the effects of EMI are not addressed. Design automation is essential for expediting EMI analysis and mitigation in power converter design. It simplifies intricate workflows, minimizes human error, and facilitates quick iterations. Parasitic elements frequently contribute to EMI problems. Through automation, designers can obtain accurate information regarding parasitic effects early in the design process, which greatly enhances the effectiveness of conducted EMI mitigation. Additionally, layout optimizations can also improve radiated EMI performance.

*Reduced-order Thermal Model:* PowerSynth 2 uses an open source model for thermal analysis [22]. The reduced-order model employed a three-dimensional nodal network (mesh) to determine the temperatures and thermal stresses of the devices. It was assumed that heat flux originated near the upper surface of each device, subsequently being conducted through the packaging structure and dissipated via convection. In this study, we consider the maximum temperature as a design parameter. In addition, the surface temperature based on the mesh structure is captured for further analysis. The inputs are the geometry of the generated layout, the PCB stack-up, and the power dissipation of each component, which is calculated by the electrical model.

### C. LAYOUT OPTIMIZATION WITH HETEROGENEOUS COMPONENTS

PowerSynth v2.1 has a hierarchical multi-objective optimization framework that consists of multi-objective particle swarm optimization (MOPSO), a non-dominated sorting genetic algorithm (NSGAII), and a build-in Randomization (RAND) method for layout synthesis. Minimize the loop inductance and maximum temperature are considered for power module design while, in power converter design maximizing the efficiency and temperature are regarded. The decision variables obtain from the flexible edges of HCG and VCG and are divided into horizontal and vertical decision variables in a hierarchical structure.

The multi-objective optimization framework for layout synthesis, is detailed in Algorithm 3. This algorithm initiates with a randomly generated initial population. Each population is subsequently assessed using an electrical model, from which the power dissipation of individual components is derived and utilized for the thermal model evaluation. The main loop of the algorithm generates a new population by evolving the current one according to the chosen optimization method. In the following step, each new population is evaluated for efficiency and maximum temperature. This iterative process continues until the predetermined maximum number of

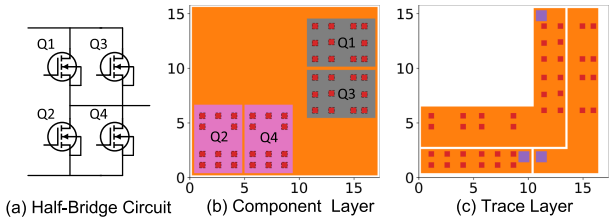


**FIGURE 7.** The minimum sized layout for flip-chip power module.

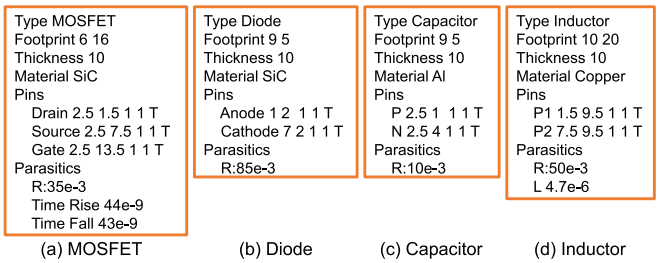


**FIGURE 8.** Different types of device definitions in PowerSynth 2.

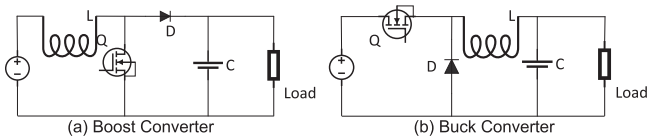


**FIGURE 9.** Two common power converters schematic design.

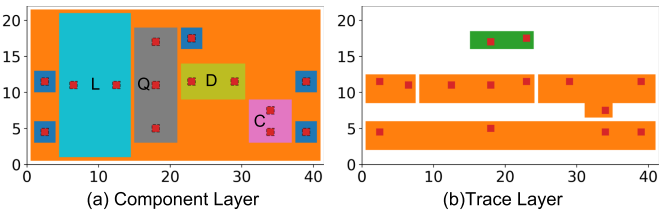


**FIGURE 10.** Boost converter minimum-sized layout.

iterations is achieved, ultimately resulting in the generation of the Pareto Front solution set. More details about the optimization framework and its interaction with the layout engine and the electrical and thermal model can be found in [23].

### D. POWER MODULE EXAMPLE WITH CUSTOM-DEVICES

Commercial SiC power devices in bare die form are usually vertical, with a bottom pad and multiple top pads that vary by device type (e.g., Schottky, MOSFET, IGBT). Wire bonding is used for electrical connections. Conversely, Flip-chip power devices feature a lateral design and do not require wire bonds, as they utilize solder balls for electrical connections. Similarly, the electrical connections in GaN devices are all situated on one side of the die, which eliminates the need for complex two-sided packaging that often limits the performance of vertical SiC power MOSFETs.

In this section, a Flip-chip design-based SiC Half-Bridge Power Module is considered to demonstrate the flexibility of the proposed method. Details about the Flip-chip SiC MOSFET are based in [24]. For layout synthesis, we consider the minimum-sized solution. Fig. 7(a) shows the Half-Bridge module circuit, which is used in this example. Fig. 7(b) and (c) demonstrate the mode-0 result for the component and trace layers. The minimum size is 17.4 mm × 15.8 mm. The result shows that the proposed methodology has flexibility for all Power Module technology packaging.

## V. POWER CONVERTER CASE STUDIES

To demonstrate the efficacy of the proposed method, we only consider the basic Boost and Buck converter as case study. It is important to note that the algorithms for representing heterogeneous components can accommodate nearly all existing components as well as those defined by users. For instance, in the case of the boost converter, designers can specify different types of capacitors (such as surface-mounted or round-shaped), and the layout optimization engine will take their impacts into account during the layout optimization process. For layout synthesis, in each case study, we consider two Scenarios: 1) maximizing power density through a minimum-sized solution (Mode-0). In this mode, the floorplan size is determined by measuring the longest distance between the source and sink vertices in the root node using the minimum weights for all edges. 2) Three different floorplan sizes are generated through the fixed-sized solutions (Mode-2).

Fig. 8 shows the definition of the most commonly implemented components in power converters such as MOSFET, diode, inductor, and capacitor. Every component should contain sections such as type, dimension (footprint, thickness), material, pin's name, and corresponding coordination, as well as parasitics and other necessary parameters for electrical and thermal analysis based on its type.

### A. BOOST CONVERTER DESIGN

A conventional boost converter is considered to demonstrate the efficacy of the proposed method. Fig. 9(a) shows the circuit design with corresponding components. The efficiency calculation for the electrical model can be found in [25].

$$\eta = P_{Out}/(P_{Out} + P_{Switch} + P_{Cap} + P_{Ind} + P_{Diode}) \quad (1)$$

Where $P_{Out}$ is the output power of the converter, $P_{Switch}$ is the power loss of MOSFET, and $P_{Cap}$ and $P_{Ind}$ are the power loss of the capacitor and inductor respectively. Also, $P_{Diode}$ is the power loss of diode. The input and output voltage are considered 24V and 48V. The output current is considered 4.8A. In addition, the switching frequency is 200kHz. The ambient temperature is regarded as 25°C. The IRF540 SiC MOSFET model is used, which has a drain-source on-state resistance of 0.077 Ω. The inductance is 4.7 $\mu$H, and the diode is assumed as SR5100.

Fig. 10(b) and (c) show the results for Mode 0 for both the component layer and trace layer. The minimum size is 41.5 mm × 22 mm. The values of efficiency and maximum temperature are 96.60% and 45.3 °C. The temperature distribution on the components' surface and trace layer are shown in Fig. 11.

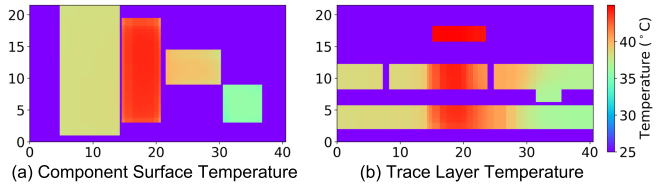


**FIGURE 11.** Boost converter temperature: (a) Component and (b) trace layer.

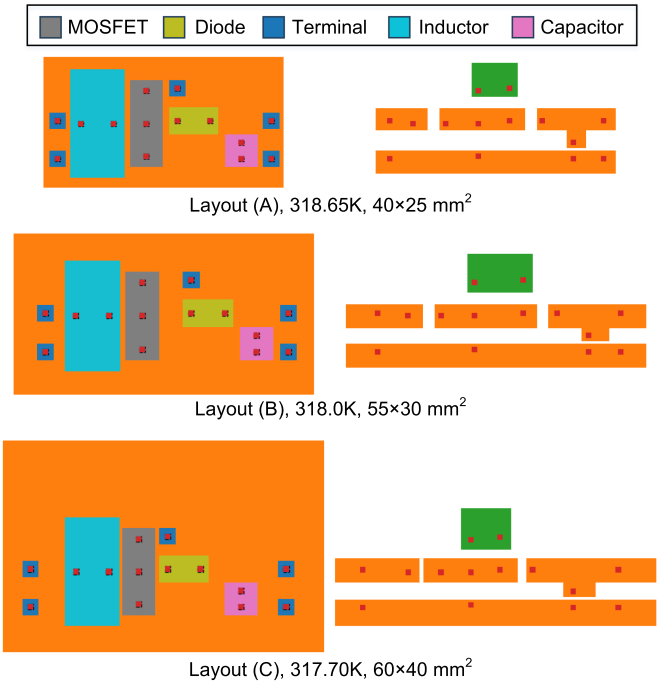


**FIGURE 12.** Three selected parato front boost converter layouts generated by RAND with 96.60% efficiency.

Shown in Fig. 11(a), the maximum temperature shown in the MOSFET as 45.3 °C. The average surface temperatures of MOSFET, Inductor, Diode, and Capacitor are 43.40, 38.30, 39.30, and 35.70 °C respectively. From Fig. 11(b), the minimum and maximum temperatures of trace layer are 36.5 and 44.9 °C. It is noted that the mesh size in thermal model in X, Y, and Z directions are 53, 31, and 15 cells, respectively, culminating in 24,645 points.

In Scenario 2 three distinct floorplan sizes are considered, ranging from 1125 mm$^2$ to 2400 mm$^2$. For each floorplan size, 100 solutions are generated using RAND algorithm. Efficiency and maximum temperature are used as cost functions. Fig. 12 shows the three selected solutions with corresponding layout and electrical and thermal values. Layout A has the highest temperature as it has the smallest floorplan size (45 mm × 25 mm). Overall, Layout C has the best thermal results, as it has the largest floorplan size (60 mm × 40 mm). Layout B represents a balanced tradeoff between the two extreme choices (55 mm ×30 mm). It is noted that all solutions have the same efficiency of 96.60%. The temperature variation is small for PCB designs because the heat conductivity of FR4

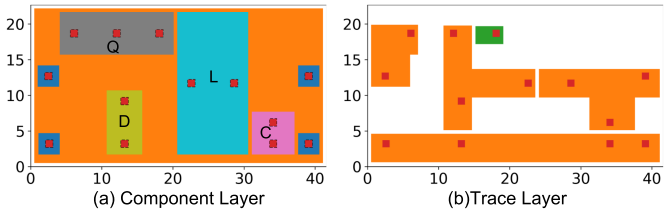


**FIGURE 13.** Buck converter minimum-sized layout.

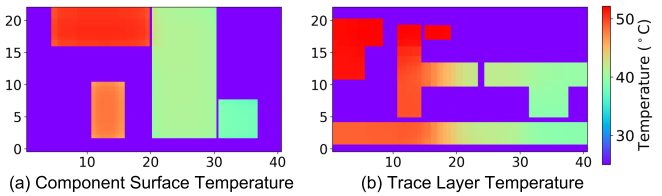


**FIGURE 14.** Buck converter temperature: (a) Component and (b) trace layer.

and solder mask is notably low compared to ceramics in DBC, which is commonly used in power modules.

### *B. BUCK CONVERTER DESIGN*

The effectiveness of the suggested approach is illustrated by utilizing a traditional buck converter. The schematic layout and respective components are shown in Fig. 9(b). The electrical model for efficiency calculation can be found in [26]. The efficiency equation is shown in (1). Input and output voltage are 24 V and 12 V, respectively with a 200 KHz switching frequency. The output current is considered 10 A. The ambient temperature is regarded as 25 °C. The IRLZ34 N SiC MOSFET is used, which has a 0.035 Ω drain-source on-state resistance. The Inductance value is 8 $\mu$H, and the diode is SR540.

Fig. 13(b) and (c) show the results for Mode 0 for both the component layer and trace layer. The minimum size is 41.6 mm × 22.7 mm. The values of efficiency and maximum temperature are 91.10 and 52.5 °C. The temperature distribution on the components' surface and trace layer are shown in Fig. 14. According to Fig. 14(a), the maximum temperature shown on the MOSFET is 52.5 °C. The average surface temperatures of MOSFET, Inductor, Diode, and Capacitor are 50.40, 41.10, 47.50, and 38.0 °C respectively. As shown in Fig. 14(b), the trace layer experiences temperatures ranging from 39 and 52.15°C. It should be highlighted that the mesh dimensions in the X, Y, and Z axes within the thermal model consist of 59, 39, and 14 cells, resulting in a total of 32,214 points.

In Scenario 2 three distinct floorplan sizes are considered, ranging from 1150 mm$^2$ to 2400 mm$^2$. For each floorplan size, 100 solutions are generated using MOPSO. The cost functions are efficiency and maximum temperature. Fig. 15 shows the three selected solutions with corresponding layout and electrical and thermal values. Layout A has the highest temperature as it has the smallest floorplan size (45 mm × 25

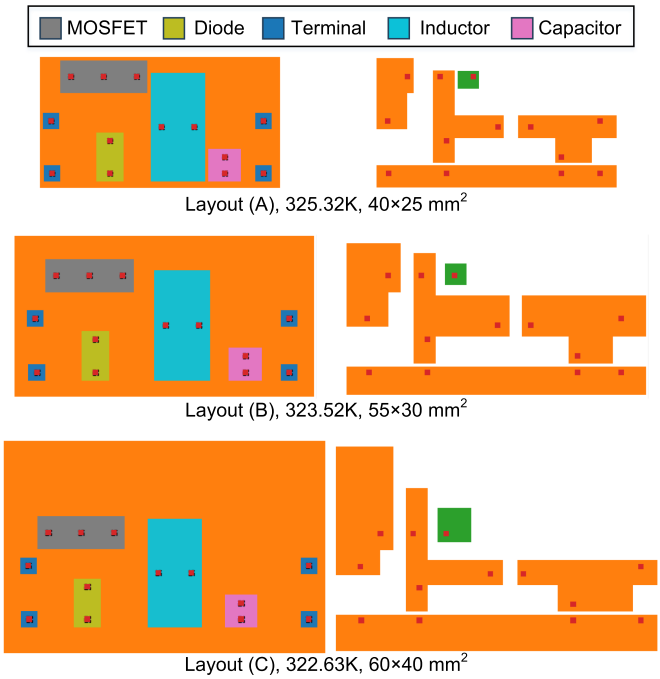


**FIGURE 15. Three selected parato front buck converter layouts generated by MOPSO with 91.10% efficiency.**

mm). Conversely, Layout C has the best thermal results, as it has the largest floorplan size (60 mm × 40 mm). Layout B represents a balanced tradeoff between the two extreme choices (55 mm × 30 mm). It is noted that the efficiency value for all solutions is the same by 91.10%. Similarly, the temperature difference is not significant due to the low heat conductivity values of FR4 and solder mask layers.

## VI. RUNTIME COMPARISON AND SUMMARY

The runtime comparison for power converter and power module design examples is studied. Runtime is measured on a server with dual Intel Xeon Silver 4210 processors. Currently, only one thread is utilized, but parallel evaluation will be implemented in the future. For the boost converter, RAND algorithm generates 100 layout. The total generation time is 80 s, and the evaluation time (electrical and thermal analysis) is 330 s. For the buck converter, MOPSO is used to generate 100 layouts. The total generation time is 100 s, and the evaluation time (electrical and thermal analysis) is 380 s. For the Power Module cases, NSGAII is used to generate 100 layouts. For a single layer half-bridge module, the total generation time is 70 s, and the evaluation time is 300 s, while for a multi-layer half-bridge module the generation and evaluation time are 100 s and 1700 s. Overall, the generation time is comparable to power module designs with fixed devices, showing the efficiency and scalability of the new layout engine.

## VII. CONCLUSION AND FUTURE WORK

In this work, PowerSynth 2 EDA algorithms have been updated from with pre-defined devices only for power modules to include heterogeneous devices used extensively in power converters. In addition, the proposed method can process user-defined components with arbitrary pin locations and shapes with more flexibility and scalability. With updated electrical and thermal models, it can synthesize new types of layouts with custom devices such as Flip-Chip SiC MOSFET. This generic physical design automation framework is further tested on two most common converters, a boost and buck power converter. Experimental results illustrate the proposed framework is generic and scalable for converter and power module layout design. Moreover, the new engine is compatible with the new optimization framework as well as thermal and electrical models for generating optimized layouts. The proposed method is opened sourced and released as PowerSynth v2.2 for public evaluation [18].

The proposed framework will be employed to expand powersynth beyond the realm of power electronics, targeting applications in data centers, heatsink design parameters, reliability assessments, and optimizations for data center operations. This will emphasize server board floor planning, and chiplet-based packaging in both air and water cooling configurations. Furthermore, we will explore a novel thermal-reliability methodology for enhanced analysis for new applications. The thermal assessment will utilize computational fluid dynamics (CFD) simulations through the OpenFOAM API to evaluate the effects of air and water cooling on various components in power electronics, and data center applications.

## ACKNOWLEDGMENT

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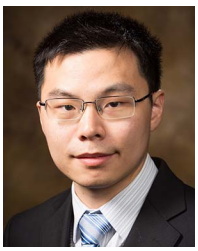

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