Automated Layout Optimization Methods of a Bidirectional DC-DC ZVS Converter Using PowerSynth

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***Abstract*— This research paper presents an advanced methodology for optimizing the design and automation of a bidirectional DC-DC converter with zero-voltage switching (ZVS). The optimization not only considers size, weight, power, and cost (SWaP-C) but also focuses on achieving an efficient and power-dense layout. It utilizes the PowerSynth tool for layout optimization. The paper introduces optimization algorithms for component selection to achieve high power density and employs the PowerSynth tool for physical layout optimization. It illustrates the tradeoff between low inductance and maximum junction temperature for different layout arrangements, aiding in selecting the optimum layout. In the optimization process, tradeoffs and critical design issues between low volume and high power are considered for the modular structure of the bidirectional boost converter. A Monte Carlo optimization method is utilized, exploring the design solution space. The physical layout solutions, including temperature and inductance values from PowerSynth, serve as input data for thermal analysis in Para Power, evaluating the associated risk for each layout design. Ultimately, this study aims to integrate mathematical design analysis with the PowerSynth 2 tool's layout optimization to automate and optimize the physical design of a ZVS bidirectional DC-DC converter.**

Keywords—Automated Optimization, Bidirectional DC-DC converter, SWaP-C parameters, PowerSynth.

I. INTRODUCTION

The automation of DC-DC converter design is of significant interest in various industrial applications, particularly in the field of electric vehicles (EVs), where achieving high power density and conversion efficiency is crucial. Bidirectional DC-DC converters capable of zero voltage switching (ZVS) operation have gained popularity in EV applications due to their low switching losses and bidirectional power flow [1-2].

Previous research works have presented optimization design methods for such converters, such as in [3]. However, most of these methods focus solely on optimizing the design based on available component databases. While these optimization algorithms contribute to striking a balance between these parameters, the physical design aspects of power converters and modules involve a wider range of factors that influence power conversion efficiency. Among the numerous parameters influencing the power density of power modules and converters, two critical ones are parasitic values (such as the parasitic inductance or capacitance between layers) and junction temperature. Later, computer-aided optimization methods are presented such as in [4-5]. However, many considerations are still not considered in these studies. In recent years, several designs of power modules using the PowerSynth tool have been presented, wherein the physical design parameters of parasitic inductance and junction temperature are considered [7-11]. In [12], the study integrates reliability metrics into power electronics module design, assessing how package geometry affects die-attachment material via simulations and machine learning optimization. An AI-driven approach automates power electronic system design for reliability, as demonstrated in [13] through a PV converter case study and nonparametric surrogate models that link design parameters to reliability metrics. In [14], industry requirements were surveyed, highlighting power semiconductor devices as the most vulnerable components. The study emphasizes the impact of environmental factors, transients, and heavy loads on power device reliability and design costs. However, the studies [12-14] have not addressed hardware-level considerations for power converter design.

The main objectives of the study are: optimizing the design of a bidirectional zero-voltage switching (ZVS) DC-DC converter, achieving a design with maximized efficiency and power density in the converter, using the PowerSynth tool for physical layout optimization, selecting components for high power density, determine the optimal number of modules of modular structure, employ Monte Carlo optimization for design exploration, perform thermal analysis to assess physical layouts risks, and automate and integrate the design process using PowerSynth 2.

II. CASE STUDY OF A BIDIRECTIONAL DC-DC CONVERTER

The structure of the utilized converter is given in Fig. 1. The presented converter has several advantages, including bidirectional power flow, ZVS-operated switches to avoid switching loss, simple switching pattern to avoid concurrent turning on both switches. It consists of two switches of S_{1p} and S_{2p}, a main inductor of L_1, an auxiliary inductor of L_{2p}, and the capacitances of C_{1p}, C_{2p}, and C_S. The low voltage side (V_l) and high voltage side (V_H) levels are set at 380V-460V and 900V-920V, respectively. The output power level of each module is

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1kW-5kW. The DC-DC converter can be applied to automotive wall chargers.

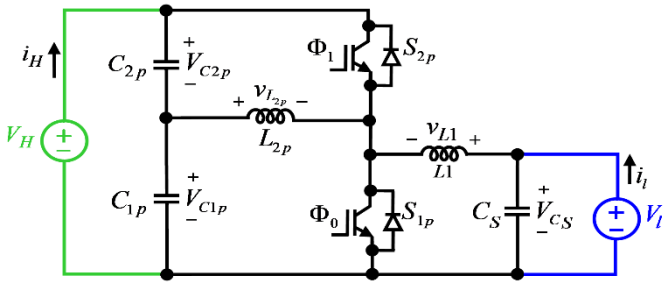


Fig. 1. Bidirectional ZVS dc-dc Converter

A. Design Considerations

Power: The nominal power for the low-voltage bus is estimated to be 22.5kW, with peak power reaching approximately 24kW [15]. To achieve this power level, multiple modules can be used in an input/output parallel connection. The optimized number of cells is determined through the proposed automation process.

Electromotive Interference (EMI): The Society of Automotive Engineers (SAE) has set the specification SAE J1113/41 to regulate EMI on the conventional 14V bus. Temperature: The prototype converter is designed to operate efficiently in ambient temperatures of up to 105°C.

Architecture: A single converter requires high-current and low-voltage components, which may result in the need for paralleled components and increased complexity. This leads to limited scalability and flexibility compared to a modular design. Instead, a modular converter improves flexibility and scalability due to the use of multiple paralleled converter cells. Moreover, interleaving cells can reduce ripple magnitude and increase the fundamental frequency of the ripple, reducing total conduction losses and power dissipation by distributing the load across multiple cells.

B. Optimization Process

The optimization process involves exploring the design space of the DC-DC converter to identify the designs that minimize a cost function. This cost function is a weighted sum of converter price, weight, and volume. The generated code considers various design variables, such as the number of cells (for high-power applications), cell switching frequency, ripple ratio, input and output filter topologies, and component types. It designs the converter using specific parts with their own price, weight, volume, and operating characteristics. The program utilizes detailed models to accurately predict the system behavior based on these specific parts. The optimization program employs a Monte Carlo design approach by starting from random points in the design space and designing converters that meet user-defined specifications. The final version of the code will be open-sourced later on GitHub.

The optimization process is visualized through flowchart presentations to generate the corresponding codes. This study aims to achieve several objectives in the design and optimization of the converter. First, an automated approach is proposed to identify the optimal design that minimizes the converter's cost, weight, and volume by selecting suitable components. Second, the sensitivity of the converter's cost-volume-weight to system-level parameters such as output power level, ambient temperature, and EMI limit is investigated. Third, the physical layout of the optimized converter is designed using PowerSynth, with the objective of minimizing parasitic effects and maximizing junction temperature. The selection of component placement in the physical design plays a crucial role in achieving high-power density for the optimized converter. Therefore, this study not only optimizes the component selection through mathematical equations but also provides the best layout design for the physical implementation of the converter, while aiming for high power density and efficiency as predicted by the theoretical equations. Fig. 2 (a) depicts the overall parameter optimization process. It shows the connection between the control loop and the design algorithm. Additionally, Fig. 2 (b) presents a flowchart specifically for the optimization algorithm, which outlines the steps involved in the optimization process in more detail. Furthermore, Fig. 2 (c) focuses on the power stage design and provides a flowchart dedicated to this aspect of the optimization process.

III. Power Analysis and Efficiency Modeling

In this part, the conduction and switching losses of the proposed converter are calculated to obtain the efficiency, power loss, and power density. So, the internal resistors of diodes (r_D), switches (r_S), inductors (r_{Lm}), capacitors (r_C), forward drop voltage of diodes, and forward drop voltage of switches are considered for calculating power losses. The voltage stress on switches is calculated as follows:

$$V_{S1p} = V_{S2p} = V_H \tag{1}$$

Average current stress on switches during conducting.

$$I_{S2p}\big|_{S2p:ON} = I_H / (1-D) = -I_{L1} \tag{2}$$

$$I_{S1p}\big|_{S1p:ON} = (I_H + I_{L1}) / D = I_{L1} \tag{3}$$

The voltage conversion ratio ($G = V_H / V_l$) between low and high voltage ports.

$$G = V_H / V_l = 1/(1-D) \tag{4}$$

where, in the boost operation, the output current is the current of the output load ($I_o = -I_H = V_H / R_H$).

The Conduction losses of the switch for boost operation are calculated as following equations:

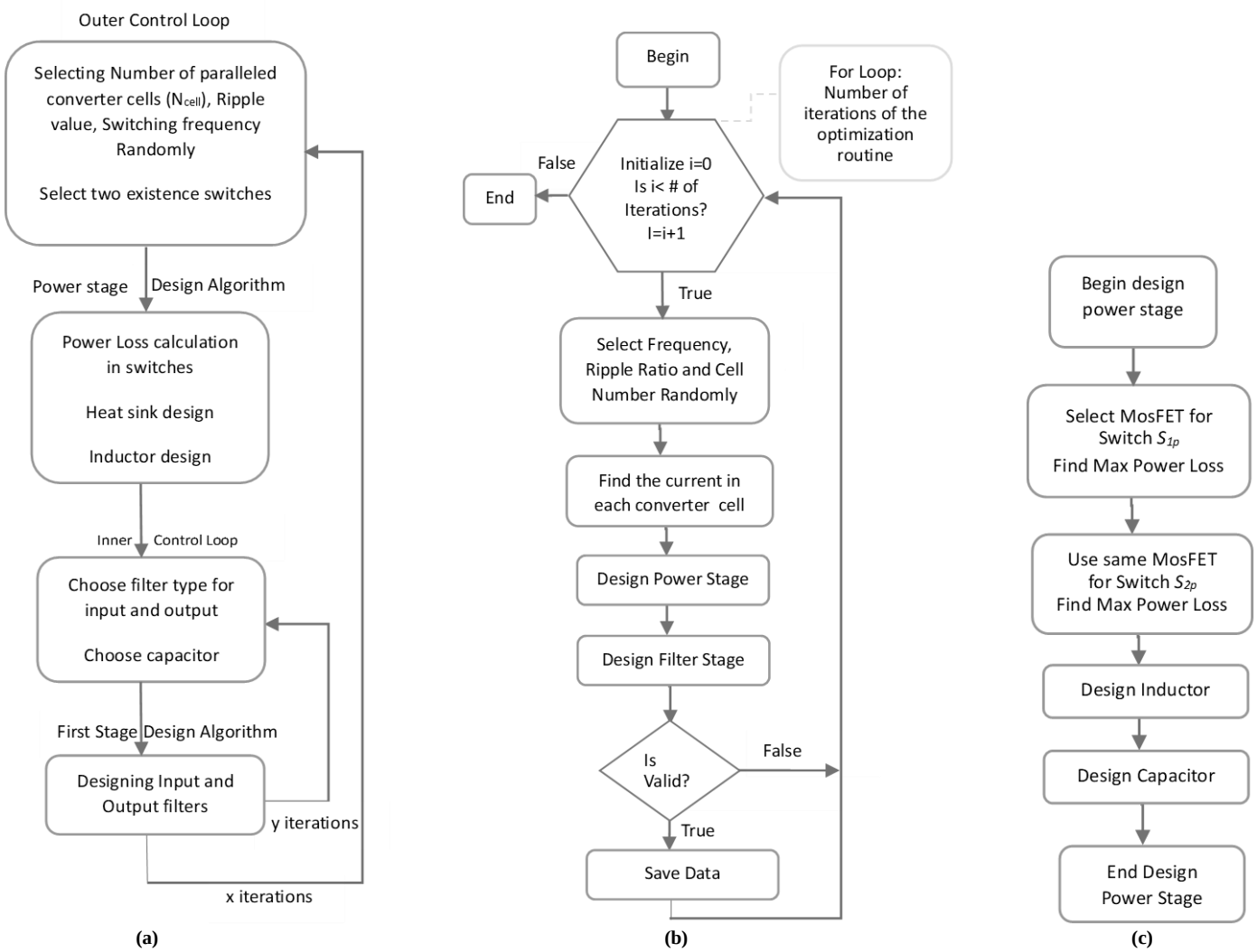


Fig. 2. Flowcharts of (a) parameter optimization process, (b) optimization algorithm, and (c) power stage design.

$$P_{Cond,S1} = \frac{1}{T_s}\int_0^{DT_s}(V_{FS1}i_{S1p} + r_{S1}{i_{S1p}}^2)dt$$
$$= (V_{FS1} + r_{S1}I_l)I_l D, \quad (5)$$
$$I_l = -I_H/(1-D)\ , I_H = V_H/R_H$$

$$P_{Cond,S2} = \frac{1}{T_s}\int_{DT_s}^{T_s}(V_{FS2}i_{S2} + r_{S2}{i_{S2}}^2)dt = \left[V_{FS2} + r_{S2}\frac{I_H}{1-D}\right]I_H \quad (6)$$

The switching losses for the switch S_2 is calculated as follows:

$$P_{sw,S2} = \frac{1}{T_s}\int_0^{t_{on}} v_{S2}i_{S2}dt + \frac{1}{T_s}\int_0^{t_{off}} v_{S2}i_{S2}dt = \frac{1}{6}f_S V_{S2}i_{S2}\big|_{t=toff}\, t_{off}$$
$$= -\frac{1}{6}f_S V_H\left[\frac{-I_H}{1-D} + \frac{-V_l DT_s}{2}\left(\frac{1}{L_1}+\frac{1}{L_{2p}}\right)\right]t_{off} \quad (7)$$

$$P_{sw,S1} = \frac{1}{T_s}\int_0^{t_{on}} v_{S1}i_{S1}dt + \frac{1}{T_s}\int_0^{t_{off}} v_{S1}i_{S1}dt = \frac{1}{6}f_S V_{S1}i_{S1}\big|_{t=toff}\, t_{off}$$
$$= \frac{1}{6}f_S V_H\left[\frac{-1}{1-D}I_H + \frac{V_l DT_s}{2}\left(\frac{1}{L_1}+\frac{1}{L_{p2}}\right)\right]t_{off} \quad (8)$$

As the two equations above show, the switching losses of switches at the moment of turning on are equal to zero. This is because, at this time, the voltage stress on the switch is zero due to zero voltage switching.

The power loss of switches and diodes (switching and conduction loss) in boost operation is calculated as follows:

$$P_{S,Tot} = P_{Cond,S2} + P_{sw,S2} + P_{Cond,S1} + P_{sw,S1} \quad (9)$$

The conduction losses of the capacitors are calculated as follows:

$$P_{Cond,C1p} = \frac{1}{T_s}\int_0^{T_s} r_{C1p}{i_{C1p}}^2 dt$$
$$= \frac{1}{T_s}\left[\int_0^{DT_s} r_{C1p}(i_H)^2 dt + \int_{DT_s}^{T_s} r_{C1p}[D/(1-D)]^2 {i_H}^2 dt\right] \quad (10)$$
$$= r_{C1p}{I_H}^2[D/(1-D)]$$

$$P_{Cond,C2p} = \frac{1}{T_s}\int_0^{T_s} r_{C2p}{i_{C2p}}^2 dt = r_{C2p}{I_H}^2[D/(1-D)] \quad (11)$$

$$P_{Cond,C} = P_{Cond,C1p} + P_{Cond,C2p} \quad (12)$$

The conduction losses of the inductors are calculated as following equations:

$$P_{Cond,L1} = r_{L1}{I_{L1}}^2 = r_{L1}{I_l}^2 \quad (13)$$

$$P_{Cond,L2p} = \left[2\int_0^{\frac{DT_s}{2}} r_{L2p} i_{L2p}{}^2 dt + 2\int_{DT_s}^{T_s-\frac{(1-D)T_s}{2}} r_{L2p} i_{L2p}{}^2 dt \right] = r_{L2p} \frac{1}{2} I_{Lp2-\max} = r_{L2p} \frac{V_l DT_s}{4L_{2p}} \quad (14)$$

As a result, the total power loss P_{Loss} for boost operation is written as follows:

$$P_{Loss\_boost} = P_{swS,Tot} + P_{CondS,Tot} + P_{Cond,CTot} + P_{Cond,LTot} \quad (15)$$

The efficiency of the proposed converter for boost operation (η_{boost}), is calculated as follows:

$$\eta_{boost} = \frac{P_H}{P_H + P_{Loss\_boost}} \quad (16)$$

where is output power for boost operation that is written as $P_H = V_H{}^2 / R_H$. As a result, the power density equation is written as follows.

$$Power\ Density = (P_l - P_{Loss})/Volume \quad (17)$$

From equations (1)-(17), one can derive and understand several key aspects of the circuit related to power conversion and dissipation including voltage and current relations: Equations 1, 2, and 3 define relationships between voltage and current in different components of the system (S_{1p}, S_{2p}, etc.); Gain and duty cycle: Equation 4 defines the system's gain in terms of the input and output voltages and the duty cycle (D); Power dissipation: Equations 5 to 8 calculate the power dissipation in various components of the system, including conductors, switches, and specific conductors like C_{1p}, C_{2p}, L_1, and L_{2p}; Total power dissipation: Equation 9 calculates the total power dissipation in the entire system by summing up contributions from different components; Efficiency: Equation 16 calculates the system's efficiency, which is the ratio of the power delivered to the load to the total power loss; Finally power density: Equation 18 calculates the power density, which can be useful for understanding how power is distributed within the system relative to its volume. The constants and variables in these equations are determined first by the system's requirements and second by the components that will be employed.

IV. Design Tradeoff and Methodology

A. Required number of modules

In the design of a DC/DC converter, various intricate tradeoffs must be carefully navigated. These tradeoffs encompass the choice between constructing a single, large converter or dividing it into multiple paralleled cells, with the latter option often chosen for the benefits of interleaving cells to reduce ripple and enhance efficiency. The number of cells significantly impacts the current ripple in input and output buses, necessitating the precise determination of cell inductance. Moreover, the number of cells influences the required heatsink size and power losses, with potential gains in efficiency offset by increased complexity. Additionally, the selection of switches and their configuration plays a crucial role in power dissipation and temperature management. Balancing these factors and considering filter design is pivotal in optimizing the performance and efficiency of a DC/DC converter. In this regard, by using the algorithm in Fig. 3, the optimized number of modules is obtained to be 5, which meets the power density of 5kW/l in the frequency range of 100kHz-300kHz.

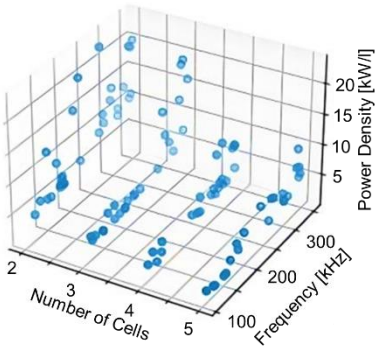


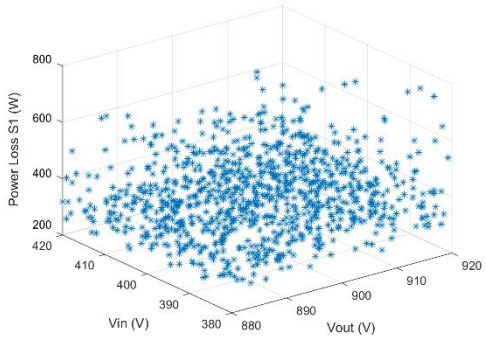
Fig. 3. The selection process on module numbers.

B. System Specifications

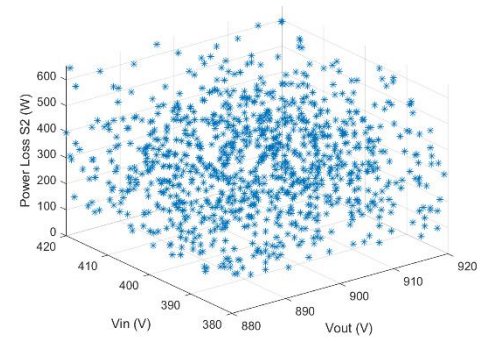
The following baseline system parameters were considered in our analysis: The input voltage range, Vin, is spanned from a minimum of 380 V to a maximum of 460 V, while the output voltage, V_{out}, is varied between a minimum of 900 V and a maximum of 920 V. A maximum output current of 60 A can be accommodated by the system. Concerning input power, it is found to fall within the range of 22.5 kW to 24 kW. The duty cycle of switches is set at 0.5, with a switching frequency ranging from 100 kHz to 500 kHz and a step size of 20,000 Hz. The acceptable Ripple Ratio varies from a minimum of 0.1 to a maximum of 1.5. The system configuration allows for a minimum of 2 cells and can be extended up to 5 cells. The ambient temperature is maintained at 100°C, with a maximum junction temperature of 140°C. The price of the PCB is \$0.18/cm^2, and the outer loop iterations amount to 20,000. These parameters form the foundation for subsequent analysis and optimization efforts.

C. Switching Device Selection

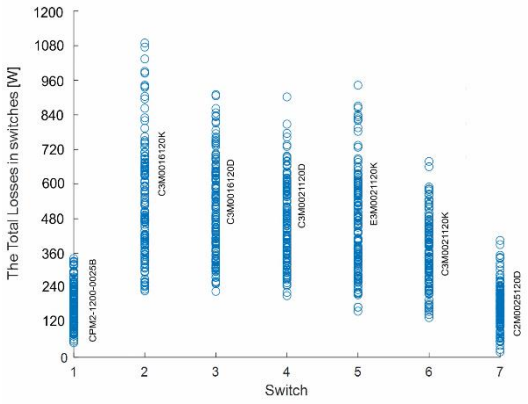
When considering the inductors as out-of-module components, the most critical aspect of the optimized design becomes the selection of switches. In this context, the power losses of the switches within the chosen input and output voltage ranges are displayed in Figures 4(a) and 4(b). Consequently, seven different switches are used as input data for optimization, which are already present in the PowerSynth library. The list of switches includes CPM2-1200-0025B, C3M0016120D, C3M0016120K, E3M0021120K, C3M0021120D, C3M0021120K, and C2M0025120D. Among these switches, as shown in Figure 3, it can be observed that the highest power density and the lowest power loss are achieved with Switch number 1 (CPM2-1200-0025B) when each module is operated at a 5kW output power level and the target power level of 24kW. This switch has the lowest mean total losses shown in Fig. 4; therefore, it has been selected for designing the physical layout in Power Synth 2.



(a) High-side switch (S2)



(b) Low-side switch (S1)



(c) Total Losses

Fig. 4. Power Losses of the switches.

D. Reliability and Risk Analysis

Automated optimization of component selection and physical layout design for reliable bidirectional DC-DC converters in Electronic Design Automation (EDA) is achieved through the integration of the ParaPower Tool with PowerSynth. This process extracts maximum temperature data, with a focus on solder joints, and compares current temperatures to the designated melting point (set at 217°C for SAC 405 solder joints) to assess layout design risks. These comprehensive assessments guide the selection of the most dependable converter design, with homologous temperature (current temperature divided by melting temperature) serving as a key metric for evaluating solder joint thermal performance and severity risk scores shown in Fig. 5.

V. Initial Results with an Optimized Layout

Figs. 6(a) and 6(b) show results generated by the NG-RANDOM algorithm with 10 layout variations, using SiC switches available in PowerSynth 2. This tool broadens design possibilities, ensuring freedom from switch-type limitations. During the initial design phase, key factors like switching frequency and inductance are determined to ensure continuous conduction mode (CCM). To optimize for lower component count and minimize output voltage/current ripple through interleaving, three converter cells are chosen. Switches are selected based on their voltage and current tolerance, following traditional design procedures. The program explores diverse design options within specified parameters to identify an optimized Pareto Front of converter designs. This selection process involves minimizing a cost function that factors in price, weight, and volume. The physical layout design is then achieved by employing the chosen optimal components in PowerSynth to reduce parasitic effects and maximize junction temperature. Fig. 6(c) illustrates the relationship between maximum temperature in Kelvin and module inductance, with a preference for lower inductance in this application.

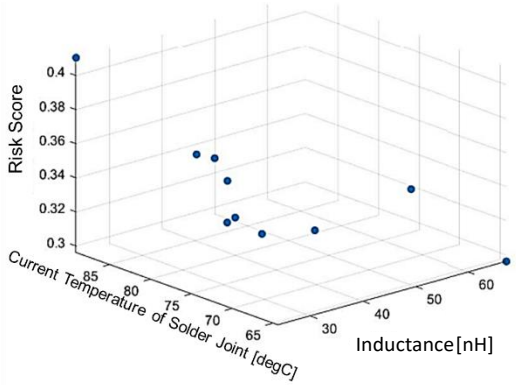


Fig. 5. Risk Score versus Inductance and Solder joint temperature for different layout models.

Additionally, in the layout design of a DC-DC converter, the incorporation of galvanic isolation may become necessary, especially when working with isolated converters or when implementing a transformer within the layout structure. To address this, a new function is developed, which can be integrated into MATLAB. It enables the generation of segments for spiral windings across different layers of the PCB. Although this specific feature is not currently included in PowerSynth, the isolation transformer for the gate drivers is represented as a black box. By customizing the core and adding the winding, the layout can accommodate the isolation transformer. It's worth noting that the future scope of this work includes the potential addition of magnetic optimization (for inductor and transformer design) capabilities to further enhance PowerSynth's functionality through various models and APIs. The extracted layout is presented in Fig. 7.

VI. Conclusion

This research paper presents a methodology for optimizing bidirectional DC-DC converter design and automation with a focus on zero-voltage switching (ZVS). It employs PowerSynth for layout optimization and utilizes Monte Carlo optimization for tradeoff analysis. The study emphasizes the importance of

component selection, particularly switches, and demonstrates the significance of temperature and inductance values in thermal analysis. By integrating mathematical design analysis with PowerSynth 2 and ParaPower tools, this research contributes to the automation and optimization of ZVS bidirectional DC-DC converter design, making it a valuable addition to design automation practices.

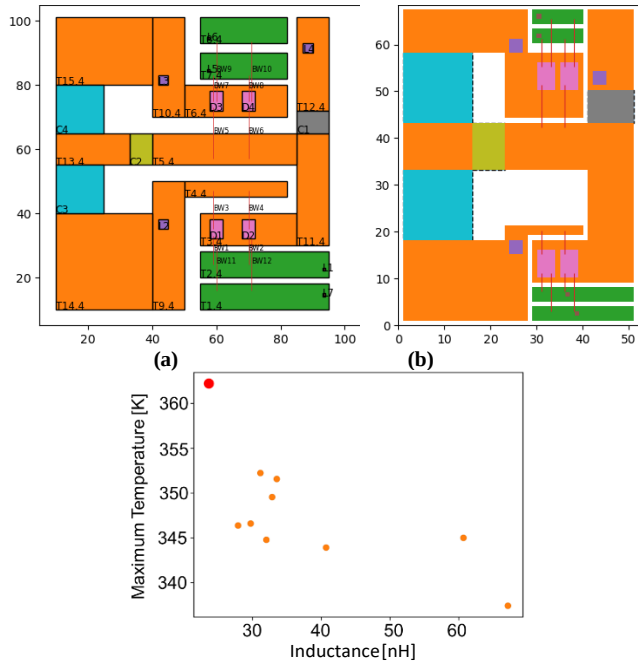


Fig. 6. Bidirectional dc-dc converter layout; **(a)** initial layout geometry of the converter, **(b)** layout geometry for Layout Mode=1, **(c)** Solution space for 2D layout optimization Layout Mode=1 (Fixed size solution).

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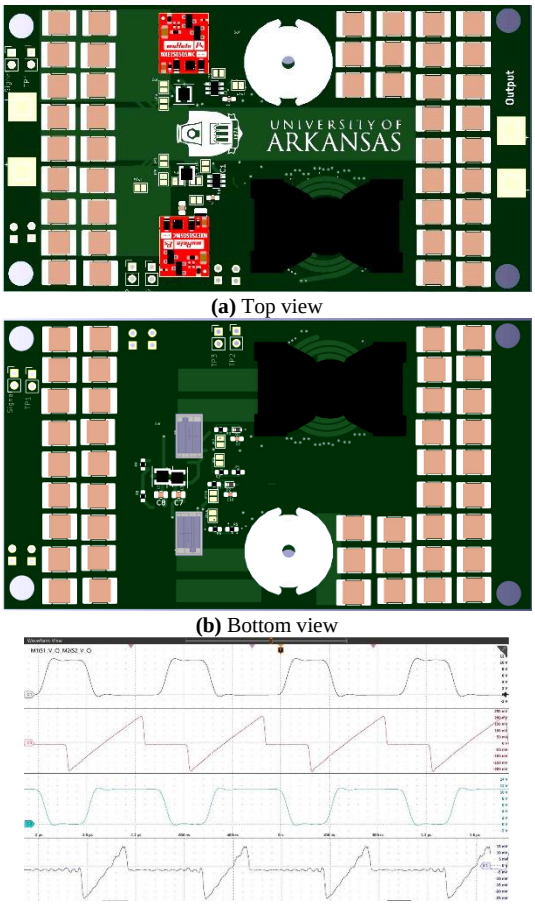

(a) Top view

(b) Bottom view

(c) Primary Experimental results

Fig. 7. The extracted layout with the primary experimental results.