Fast and Accurate Parasitic Extraction in Multichip Power Module Design Automation Considering Eddy-Current Losses

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***Abstract*— Recent studies in power electronic design automation have introduced various models for parasitic extraction of multichip power module layouts. However, none of these studies considers the eddy current effect in the direct-bonded-copper substrate, accounting for 40%–50% errors in the extraction result. This work introduces a methodology for eddy-current consideration through numerical simulation and regression modeling. The regression model utilized in the characterization process in this work is fast and memory-efficient compared to the finite element approach. This characterization process can improve the accuracy of any partial element model without sacrificing performance. Combining this characterization process and partial element approach achieves less than 10% extraction error compared to Ansys Q3D while showing a maximum speedup of 35× and 17× more memory efficiency. This method also significantly reduces the number of elements in the extracted netlist and the complexity of loop evaluation. This method is attractive for use with optimization routines and, therefore, has been used successfully in a layout optimization tool.**

***Index Terms*— Design automation, inductance extraction, multichip power module (MCPM), PowerSynth, regression model.**

I. Introduction

THE emerging research in multichip power module (MCPM) technologies has utilized the benefits of the wide bandgap (WBG) devices thanks to their higher thermal conductivity and current carrying characteristics [1], [2]. While WBG devices offer many known advantages, such as higher blocking voltage, faster operating frequency, and higher junction temperature, they also bring many challenges to the MCPM layout design, making this design process a multidisciplinary problem. Some main design aspects include electrical parasitics, thermal management, or mechanical reliability [3]–[5]. Among these design aspects, electrical design is the most crucial target for any MCPM layouts [6]–[8], and this aspect is a multidisciplinary problem in and of itself. The coupling among layout, WBG device parasitic parameters, and high di/dt and dv/dt during the transient produce many undesirable dynamics. These dynamics form high-voltage overshoot ($L \cdot di/dt$), leading to failure in the semiconductor device, increased switching losses and reduced system-level efficiency [9]–[11]. In addition, instability issues, such as false turn-on and self-sustained oscillation, can occur if the layout is not designed correctly [12], [13]. Therefore, electrical parasitics analysis, especially parasitic inductance extraction, is crucial to designing a proper MCPM layout. More importantly, fast and accurate electrical parasitic modeling is a required design target in emerging MCPMs' layout design automation and optimization trends. Generally, to achieve a

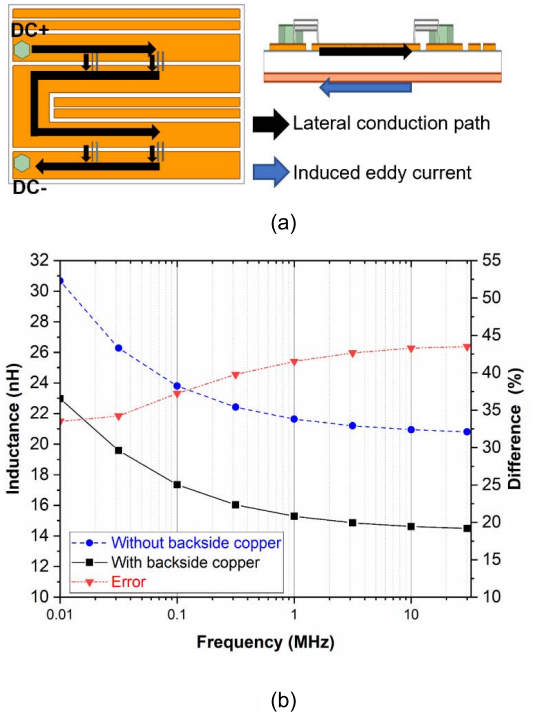

Fig. 1. (a) Lateral versus eddy current paths in an MCPM. (b) Impact of the eddy current on extraction result from Ansys Q3D.

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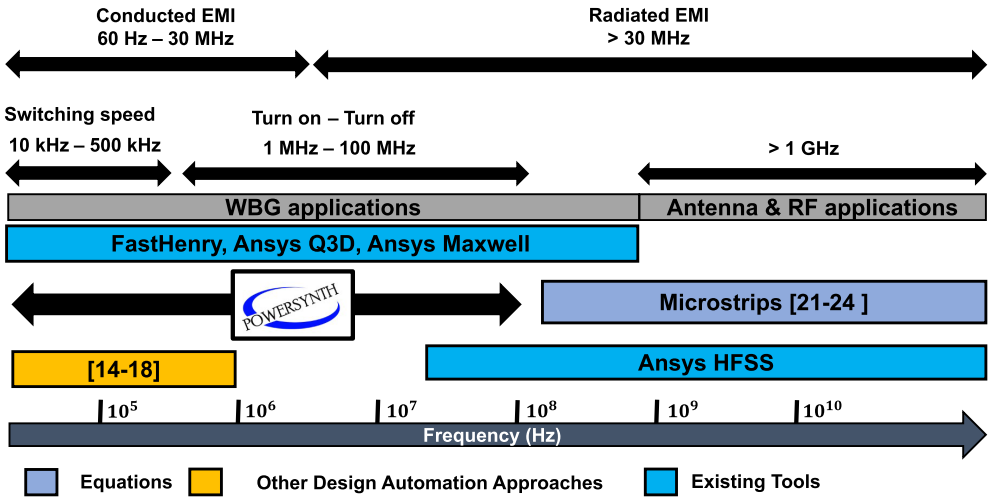

Fig. 2. Inductance extraction frequency range for WBG application and PowerSynth's target frequency range versus other approaches.

fast and accurate extraction of the MCPM layout structure, the model has to capture two critical physical aspects accurately [see Fig. 1(a)]: 1) the proximity effect among parallel conductors on of the lateral surface and 2) the induced eddy current on the DBC backside. Finite elements analysis (FEA) simulation tools, such as Ansys Q3D, consider these effects accurately by solving Maxwell equations. While being accurate, FEA tools require substantial computational resources through solving magnetic and electric integral equations. Hence, these tools are only suitable for a single manual layout design and are not very attractive for design automation. To fill the parasitic inductance modeling gap for the power electronic design automation, many research groups have offered self-developed models [14]–[19] to extract the layout parasitics parameters quickly. These models accurately capture lateral current commutation, which is crucial in reducing the parasitic loop inductance. However, these models often ignore the eddy current effect, leading to the possible overestimation of parasitic extraction results. This induced eddy current often exists on the backside copper of the DBC, which also often acts as a shielded ground plane. The half-bridge layout in Fig. 1 shows a maximum of 43% overestimation in the extraction result without eddy current consideration using Ansys Q3D. This overestimation can go up to 80%, as reported in [20]. While ignoring eddy current impact might not affect the optimization results of the lateral loop, this can lead to a high inaccuracy in voltage overshoot or gate-loop stability simulation. Therefore, the methodology in this work describes a regression model formulation through a trace characterization process. These regression models are used in a loop-based method for fast and accurate loop evaluation with a distributed netlist extraction capability. This combination of the regression model and the loop-based evaluation method enables a fast evaluation of parasitic parameters giving accurate electrical design insights in an optimization routine.

II. Literature Review

A. Extraction Frequency Range for MCPMs

There has been extensive study on impedance models that consider eddy current effects in other fields. One such example includes closed-form analytical equations for the parasitic inductance of microstrip structures. These microstrip models are commonly used in printed circuit boards (PCB) for antenna applications [21]–[23], with much smaller trace width and conductor thickness than DBC. These models are only correct for very high-frequency applications (GHz range). At this high-frequency range, the microstrip model assumes zero thickness conductors due to the submicrometer thickness value of the skin depth at the RF frequency region. Some microstrip models require complex integral or numerical evaluation, which is not computationally attractive for design automation [23]. An approximate partial element equivalent circuit (PEEC) based on a 2-D method expression for eddy-current losses has been derived in CMOS monolithic inductors and transformers design [24]. This method ensures accurate extraction for a high-frequency range (100 MHz–14 GHz). However, it also requires numerical integration for the self-impedance and the mutual impedance, which is quite computationally expensive.

In WBG applications, turn-on and turn-off rates of WBG devices dictate the concerned frequency range for MCPM. As reported from the literature, these values are about 27–50 ns for SiC and 5–10 ns for GaN devices [1], [2]. These turn-on and turn-off rates limit the frequency range for inductance extraction in an MCPM layout. In addition, an accurate parasitic model is also required for the conducted electromagnetic interference (EMI) analysis [25]. Hence, the effective frequency range for MCPM parasitic extraction needs to be accurate in the 10-kHz–30-MHz range (see Fig. 2). In this frequency range, quasistatic approximation techniques, such as the method of moments (MoM), PEEC [26], and other partial elements approximation models are used to extract the layout inductance. These models have been used in state-of-the-art (SOTA) analysis tools, such as Ansys and COMSOL, or the high fidelity open-source analysis tool, such as FastHenry [27]. While suitable for broadband frequency extraction, these models are usually computationally expensive, making it unfavorable for an optimization routine. In addition, it is hard to extract a distributed netlist for the further circuit simulation study. For example, MoM techniques usually report a single loop-inductance value. On the other hand, PEEC provides a

dense matrix with hundreds of thousands of elements. The designer needs to take an extra step to extract a multiport netlist, which requires more computational effort.

B. Parasitic Extraction Models in Power Electronics Design Automation

In design automation and layout optimization studies, the parasitic extraction models are usually modified or simplified to speed up the extraction time while maintaining acceptable extraction accuracy [14]–[19]. However, at the time of this writing, the induced eddy current is not considered in parasitic extraction modeling in many MCPM design automation studies. For example, Ning *et al.* [18] applied the MoM method to extract the parasitic loop inductance for layout optimization. This method claims to have a good agreement with state-of-the-art simulation tools and is efficient for layout optimization; however, the method only considers the current commutation on the top layer of the DBC, which gives overestimated parasitic loop result. Unlike MoM, which usually requires many mesh elements, the partial elements method divides the layout into long and thin segments, which reduces the total number of elements. Therefore, the partial elements method has been used more often in recent studies [14]–[17]. For instance, in [14], a tool named current bunch is developed where the model divides the MCPM layout into many parallel long segments, namely, current bunches. Each segment width in this current bunch tool is set to be close to the skin depth value at the extraction frequency, accurately capturing the proximity effect in the lateral conduction path. Each segment's self-inductance and segment-segment mutual inductance are evaluated using existing analytical equations. However, these equations are developed for open-loop cases where the current is assumed to return at infinity. This equation is not applicable for DBC-based MCPMs since the backside copper of the DBC substrate acts as a ground plane and a magnetic shield, which reduces the total loop inductance significantly.

There are two main goals for the electrical model used in the MCPM layout optimization tool PowerSynth [28]: 1) fast and accurate extraction of MCPM parasitic parameters and 2) a distributed netlist generation for fast, postlayout optimization circuit analyses. PowerSynth employs a different approach to consider eddy current: the self-inductance values with eddy current consideration are first extracted through running many FEA simulations where the response surface method [29] has been used to fit the simulated data to the geometrical parameters of MPCM trace. Through this initial computationally expensive characterization process, the characterized self-inductance model can be reused many times during layout optimization, which reduces the computational effort during this optimization process. The work in [30] combines PEEC and response surface models to improve extraction accuracy, which has been experimentally validated in [31]. However, as the PEEC matrices are dense and contain many elements, it is not scalable for more complex MCPM layouts with many parallel devices.

In the previous PowerSynth articles, the focus was on the layout optimization algorithm and lacked a thorough description of the parasitic extraction methodology itself. Moreover, the models described in [29] require running simulation tools, such as FastHenry or Ansys Q3D, to build the response surface method. These approaches also require scripting knowledge for these simulation tools, making it hard for other researchers to reimplement the model. Therefore, this article carefully explains the physics behind the eddy current effect and details an analytical approach for the regression model formation. Incorporating the loop-based approaches from very-large-scale-integration (VLSI) [32]–[34], the method developed in [19] is developed and improved for trace model characterization and the lateral evaluation of the MCPM layout. A relative comparison between this model and the previously mentioned models has been shown in Table I. This result has shown that this model is most suitable for layout optimization purposes. Furthermore, the model also provides a reduced-order distributed netlist extraction, which benefits the postlayout circuit simulation study.

III. Methodology and Theoretical Background

A. Physics Behind Eddy Current

In short, an alternating current in a nearby conductor creates an alternating magnetic field in the plane perpendicular to the conduction path. This alternating magnetic field, in turn, creates an induced current in the backside copper, which flows in the opposite direction to the alternating current from the source. In the case of MCPMs, the resulting induced current on the backside copper from the alternating current on the topside forms a loop. Fig. 3 shows the differences between the open-loop case and the MCPM case. In the open-loop case, the current is assumed to return in a plane infinitely far from the conduction path, which results in a much higher inductance value. Hence, using formulas for the open-loop self-inductance results in an overall overestimated loop value. A simulation study is performed to see the impact of the backside current density versus frequency. A simple MCPM trace structure is built in ANSYS Q3D with a width of 1 mm, a length of 25 mm, and a thickness of 0.2 mm on top of an alumina DBC substrate with a 0.64-mm isolation layer (see Fig. 4). As seen in Fig. 4(b) the result shows that the eddy current concentrates below the trace, and the current density peaks at the center location of the trace and gradually decreased at the locations further from the center. The eddy current value becomes insignificant at a fixed distance $x0$ from the center. Therefore, the resulted trace inductance will be the same for the backside copper width greater than $W = 2 \times x0$

$$\delta = \sqrt{\frac{2}{\omega u \sigma}}. \tag{1}$$

From the Maxwell equations, the work in [18] developed a closed form equation for the current density of a microstrip trace on PCB

$$J_{gr}(x) = \frac{I_i}{w\pi}\left[\arctan\frac{w-2x}{2h} + \arctan\frac{w+2x}{2h}\right] \tag{2}$$

TABLE I
COMPARISON AMONG EXISTING PARASITIC EXTRACTION METHODS FOR MCPM

Approach	Eddy Current	Extraction time	Accuracy	Flexibility	Distributed Netlist	Broadband
PEEC [26]	Yes	Slow	Very High	Very High	Hard to extract	Yes
Ansys Q3D	Yes	Slow	Very High	Very High	Hard to extract	Yes
FastHenry [27]	Yes	Average	Very High	Very High	Hard to extract	Yes
Horowitz [16]	Yes	Not Mentioned	Acceptable	High	Not mentioned	Yes
Ning [18]	No	Fast	Not Mentioned	High	Not mentioned	No
Current Bunch [14]	No	Fast	High	High	Yes (R, L, and M)	No
PowerSynth v1.1 [28]	Yes	Very Fast	Acceptable	Low	Yes (only R, L)	Yes
PowerSynth v1.9 [31]	Yes	Average	High	High	Yes (only R, L)	Yes
This work and [19]	Yes	Fast	High	High	Yes (R, L, and M)	Yes

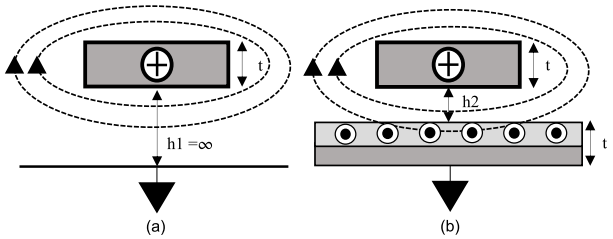

Fig. 3. Magnetic fluxes in (a) open-loop case and (b) MCPM case, where hi is the distance to ground plane, δ is the skin-depth value, and t is the copper thickness.

where Ii is the total current through the trace (normalized to 1A), w is the trace width, x is the distance from the trace center, and h is the distance from the trace to backside.

As can be seen from (2), this current density value is independent of trace length and thickness. With increasing isolation thickness h, the eddy current density also reduces. Fig. 4(b) shows the normalized distribution of the current density using (2) versus the simulated result from Ansys Q3D. As seen in the results from Fig. 4(b), the numerical simulation shows the same distribution versus the theoretical case using (2). Therefore, this equation can be used to evaluate the $x0$ value where the eddy current is zeroed out.

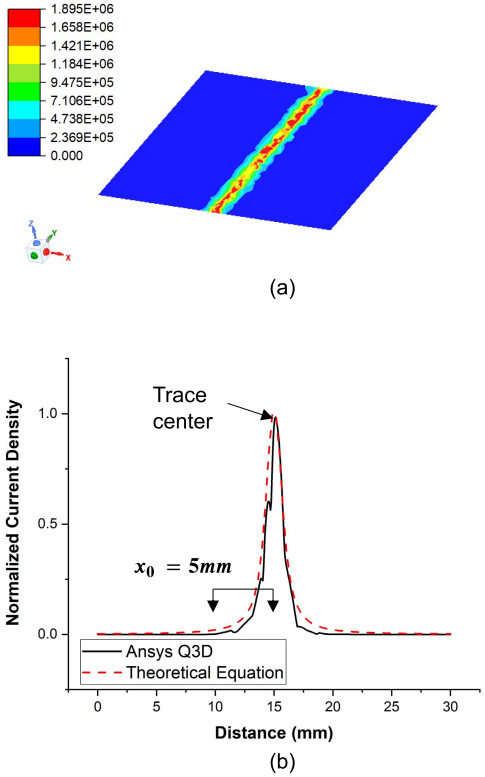

Fig. 4. (a) Backside current density at 10 MHz. (b) Normalized current density distribution.

B. Self-Inductance and Mutual Inductance Extractions for MCPM Traces

Under the scope of design automation and optimization, self-inductance and mutual inductance models must be fast while maintaining accuracy. In this article, input parameters are formed, where numerical simulations are run to collect the self-inductance and mutual inductance values. The results from these numerical simulations can be collected to form equations for L_{trace} and M_{trace}, which are later used in partial element methodology to evaluate the layout's lateral loop. This process is demonstrated in Fig. 5.

1) Input Parameters: A design of experiment (DOE) is first required to form the input parameters for the simulation. In the case of the MCPM application, the parameters are divided into two different sets. The first set is fixed parameters, including material, conductor thickness, and isolation thickness. These parameters are always provided in DBC's vendor datasheet. Because there is a limited number of DBC types, the model can be built only once for each different DBC configuration. The second set is the actual input parameters for the model, as illustrated in Fig. 6. For the self-inductance model, this is the width W and length L of the trace. For the mutual inductance model, the input parameters are the trace width W, the trace length L, and the distance between two traces d. Next, appropriate width and length values are needed for the model fitting for the self-inductance, while distance values are needed for mutual inductance. In this case, the minimum trace width range is decided by the skin depth at 100 MHz where the minimum trace length is set to 5× of this value. The maximum trace width is set to 1 mm, and the maximum trace length is 25 mm accordingly. A 2-D matrix of different trace widths and lengths can be formed using these ranges. In the case of mutual inductance, the distance range is set from 0 to 10 mm. Finally, the backside copper width can

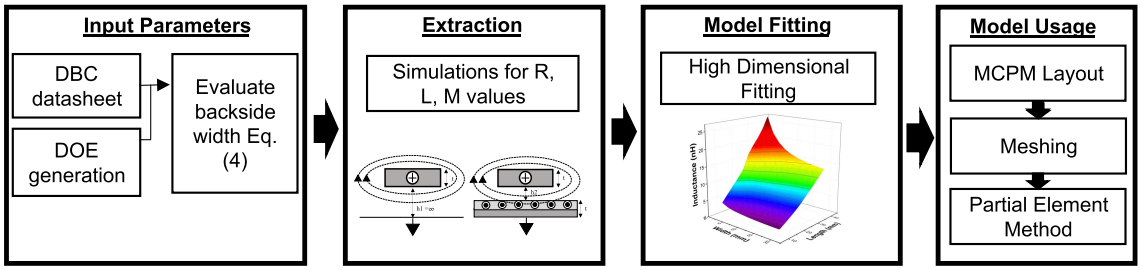

Fig. 5. Model characterization process.

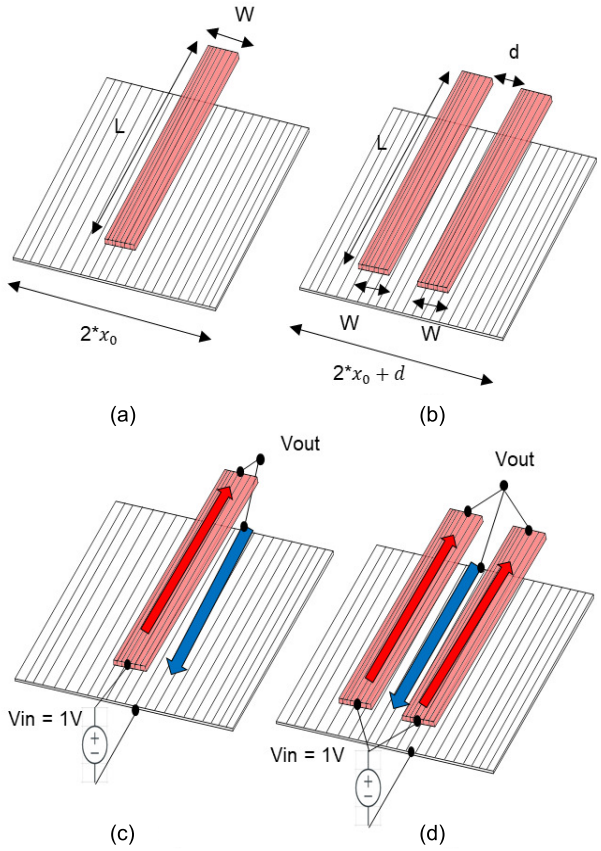

Fig. 6. Input parameters for (a) single-trace impedance and (b) mutual inductance between traces. Simulation setup for (c) single-trace impedance and (d) mutual inductance.

be defined through the datasheet parameters and trace widths values using (2). This equation has been used to make sure that the model captures most of the eddy-current impact. These input parameters cover some common dimensions from the MCPM layout. This places some initial boundaries on the model prediction range. The extraction data can be stored and continuously updated if there are any updates in the input parameters.

2) Impedance Extraction Using Loop-Based Extraction Method: In the extraction step, a structure in Fig. 6 is set up using the input parameters. FEA simulations can be used here to extract the self-inductance and mutual inductance values. However, this process can be very computationally expensive; for this structure, a partial element approach is much more efficient. Therefore, the loop-based method [19] is modified to extract the trace resistance, inductance, and mutual inductance values considering the backside effect. In this approach, the structure is meshed into parallel, thin, and long filaments. To ensure accurate extraction, the filament width is set to the skin depth of the maximum extracted frequency. Next, a set of analytical equations can be used to compute the resistance, inductance, and mutual inductance for the filaments [35]. All impedance values are stored in an $n \times n$ matrix $\mathbf{P}$, where n is the total number of elements, $\mathbf{P}(i, i)$ is the partial self-impedance, and $\mathbf{P}(i, j)$ is the partial mutual impedance between elements i and j. Then, an $n \times k$ mesh matrix $\mathbf{M}$ is formed, where k is the number of forward current elements. In this matrix $\mathbf{M}$, if an element i is in the forward current path, $\mathbf{M}(i, j)$ is 1, and 0 otherwise. A column vector $\mathbf{u}$ is also formed with n rows of one; this is a normalized vector for the voltage drop across each trace. Two equations are then formed and evaluated, as shown in the following:

$$Pa = u \quad \text{and} \quad PB = M. \tag{3}$$

Vector $\mathbf{a}$ is used to compute the current distribution in each element, which is unified to have a norm sum of 1. The result from matrix $\mathbf{B}$ along with this unified vector is then used to obtain the current matrix $\mathbf{I}$, whose jth column vector $\mathbf{I}(j)$ can be calculated using

$$I(j) = B(j) - V_{\text{out}} \times a \quad \text{where} \quad j = 1, 2, \ldots, n \tag{4}$$

where

$$B_{\text{out}} = \frac{\sum B(i, j)}{\sum a}. \tag{5}$$

Let k be the total number of loops forming from the top trace and backside. The total current through each loop is computed by

$$I_{\text{trace}} = M^T \times I. \tag{6}$$

Then,

$$Z_{\text{trace}} = \left(M^T \times I_{\text{trace}}\right)^{-1}. \tag{7}$$

The extraction is performed for all variations of parameters and the extracted frequency (f). The results for R_{trace}, L_{trace}, and M_{trace} are stored in the table form for the model fitting process. Fig. 7 shows the comparisons among the extraction using different models and for some selected input parameters. The result shows the error within 6% between the loop-based methods versus Ansys Q3D for both self-inductance and

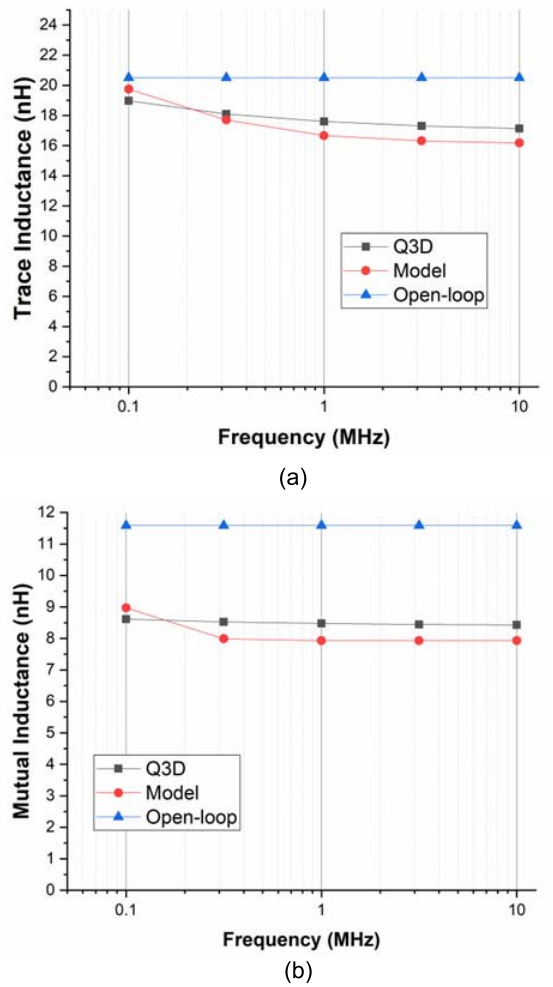

Fig. 7. L and M extraction results' comparison among different approaches for (a) $w = 1$ mm and $l = 25$ mm, and (b) $w = 1$ mm, $l = 25$ mm, and $d = 1$ mm.

TABLE II
PERFORMANCE VERSUS ANSYS Q3D FOR L AND M CHARACTERIZATIONS

	Ansys Q3D		Loop-based	
# Run	Time	Memory	Time	Memory
1	70 s	310 MB	9 s	5 MB
100	1 h 40 m	310 MB	15 m	5 MB

mutual inductance extractions. The open-loop equation shows 30%–40% errors for both self-inductance and mutual inductance cases. Table II shows the memory and time comparisons using the loop-based method versus FEA simulation using Ansys Q3D. On the same computer, for this simple structure, the model is 7× faster and 62× more memory-efficient than the FEA approach.

3) Regression Methodology for Model Characterization: Once all extraction results are collected, regression models can be built to evaluate for trace impedance values quickly. The Python Scikit-Learn library [36] offers many different regression techniques, such as linear, polynomials, support vectors, artificial neural networks, and so on. However, among these existing methodologies, the polynomial regression method is

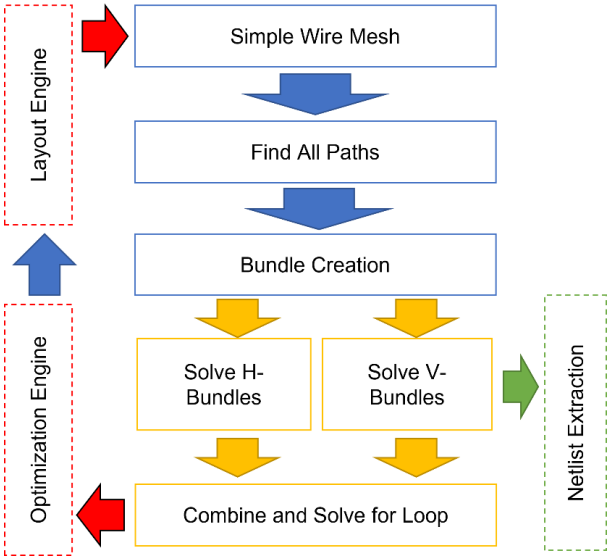

Fig. 8. Loop-based method extraction flow.

the most suitable for fitting the impedance equations. This is because this model allows a nonlinear fitting while having a simple equation form. The general polynomial equation forms in (8) and (9) have been used here to fit the model

$$f_{\mathrm{RL}}(W, L) = \sum_{0}^{K} a_k W^k + \sum_{0}^{K} a_k L^k + \ldots + \sum_{0}^{M} a_m W^m L^m \tag{8}$$

$$f_M(W, L, d) = \sum_{0}^{K} a_k W^k + \sum_{0}^{K} a_k L^k + \sum_{0}^{K} a_k d^k + \ldots + \sum_{0}^{M} a_m W^m L^m d^m \tag{9}$$

where W is width in mm, L is length in mm, d is distance in mm, a_i are coefficients to be fit, K is the number of degrees, and M is the number of interaction features.

A third-order polynomial ensures a fitting error of less than 10% for R_{trace} and 1% for L_{trace}. As for the mutual inductance model, a fourth-order polynomial equation form ensures a fitting error of less than 1%. Once the model is characterized, it can be reused many times for the same DBC structure. More importantly, the characterized model is much faster and memory-efficient than the simulation. Hence, it can be used in any partial element solver to evaluate the MCPM electrical parasitic parameters.

To consider the broad frequency band effect, the model is characterized in both low- (<1 kHz) and high-frequency regions (>10 MHz). Then, a ladder circuit model in [37] can be used to effectively estimate the inductance value for any frequency points. As mentioned in [37], this ladder circuit model is accurate for a maximum frequency of 6 GHz well beyond the frequency range considered for MCPM applications (see Fig. 2). Similar to self-inductance, the mutual inductance value is also frequency-dependent. However, there is no known circuit model in the literature for the mutual inductance versus frequency. Hence, to have the best approximation value for

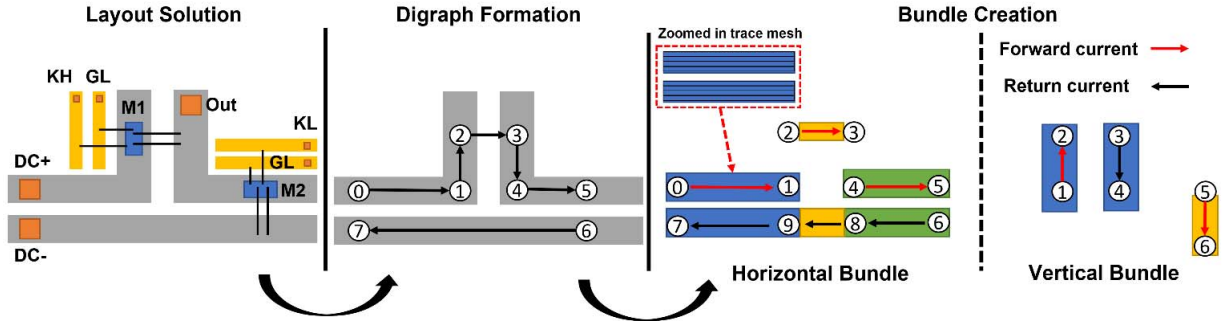

Fig. 9. Layout to the bundle formation process.

all frequency points, the mutual inductance model is built for every first frequency point per decade between dc and 30 MHz.

Algorithm 1: Digraph Formation

```
Input  : Initial Wire Mesh Graph (G)
Output: Digraph from source to sink (D)
if exist_path(G,source,sink) then
    paths = depth-first-search(source,sink)
else
    raise error: no path exist
    return
for i ← 0 to len_of(paths) do
    /*Get the array of nodes on paths*/
    p = paths[i]
    /*Loop through all node to form digraph*/
    for j ← 0 to len_of(p)-1 do
        if not(exist_path(D, p[j], p[j+1]) then
            add edge(D, p[j], p[j+1])
```

4) Using the Regression Model in Loop-Based Extraction Method: Fig. 8 illustrates the design flow of the loop-based method [14] to solve for the MCPM lateral-loop parameter. To begin with, a layout geometry from the layout engine [26] is transformed into a wire mesh using trace-edge location, device location, and bondwire landing location. These locations are represented as nodes where edges are formed if they share the same layout traces or bondwires. A pathfinding based on the depth-first search algorithm [38] (shown in Algorithm 1) finds all existing paths from the source and sink and transformed the wire mesh into a directed graph (see Fig. 9). The directed graph is further divided into two groups of the horizontal and vertical bundles with defined forward and return current directions. Also, for each bundle, a uniform mesh (see Fig. 9) is formed to consider the proximity effect among traces. While this might look similar to the current-bunch concept in [10], the key difference is using (3) to capture the current distribution among parallel traces. This gives a better frequency transition, whereas, in [10], each current-bunch object is assumed to have a uniform current distribution. Finally, using (4)–(8), the loop impedance for all horizontal and vertical bundles can be evaluated. Here, to consider the eddy current impact, (8) and (9) have been used in the formation of the partial impedance matrix P. Once all impedance values for the bundles

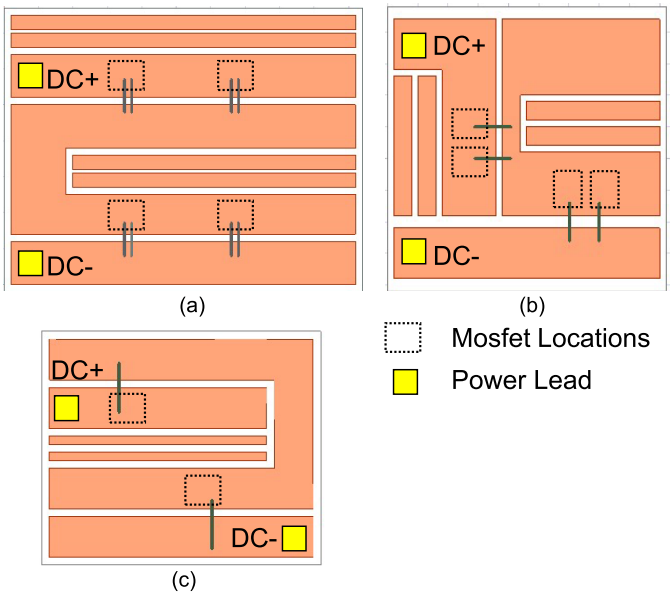

Fig. 10. (a) Layout-1 (52 × 40 mm^2) design under test (DUT) for experimental validation. (b) Layout-2 (50 × 47 mm^2). (c) Layout-3 (35 × 28 mm^2).

are updated, the impedance of each bundle is calculated; they are stored in a square matrix A with the size of $N \times N$, where N is the total number of horizontal and vertical loops. The loop impedance is then simply calculated using

$$AI_i = V_i \tag{10}$$

where I_i is the current vector for the total current through each loop and V_i is the input voltage vector.

By dividing the layout into multiple bundles, the total complexity for this algorithm is $O(N \times E^2)$, where E is the average number of elements in each bundle. The value of E is usually very small in the case of an MCPM layout.

IV. Experimental Validation and Performance Comparison

A. Experimental Validation for a Selected Layout Case

A device under test (DUT) for a 2-D half-bridge layout is fabricated on an Alumina DBC substrate with a copper thickness of 0.2 mm and an isolation thickness of 0.64 mm

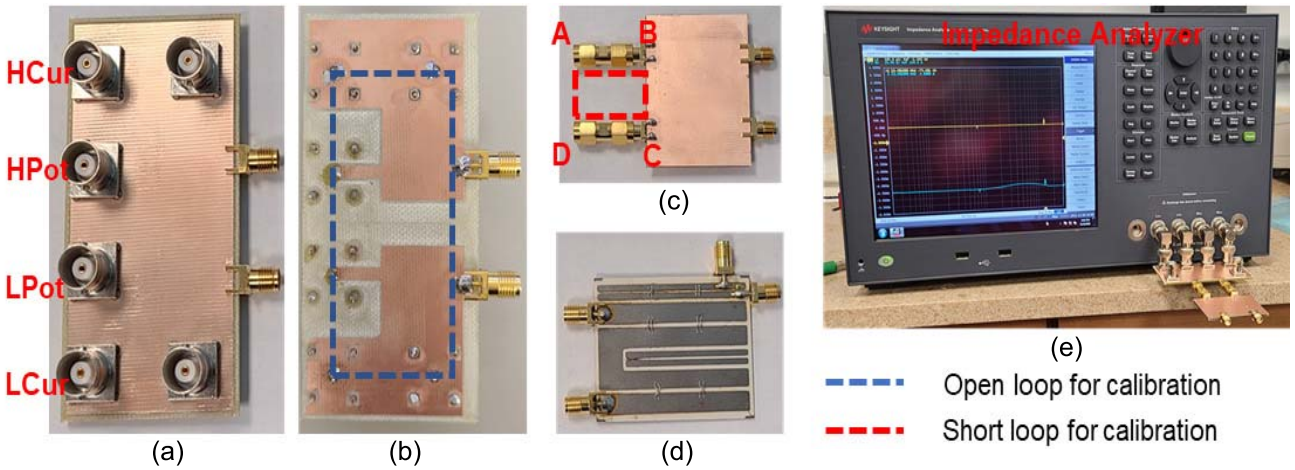

Fig. 11. (a) Topside of the custom-made PCB fixture, (b) bottom side of the PCB fixture, (c) board for the short calibration, (d) design under test layout, and (e) impedance analyzer.

[see Fig. 10(a)]. The layout is designed for a half-bridge circuit with two devices for each switching position on a 39.5 × 52 mm^2 footprint. However, bond-wire connections are used to form shorts at the locations of the devices to form the loop between dc+ and dc−. Two SMA connectors are connected to dc+ and dc− locations on the DUT to interface with the impedance analyzer [see Fig. 11(d)]. A Keysight E4990A impedance analyzer has been used to measure many power electronics systems in [39] and [40], and has also been used in this work to verify the power loop inductance against the extraction results. While E4990A is capable of impedance measurement between 20 and 30 MHz, there is a limit in the impedance resolution, making the impedance lower than 100 kHz inaccurate. There is a very small change in inductance for the frequency range greater than 10 MHz. Therefore, the frequency range has been selected between 100 kHz and 10 MHz for this measurement.

This impedance analyzer requires four BNC connections for high-low currents and high-low potential ports [HCur, LCur, HPot, and LPot in Fig. 11(a)]. Hence, for this measurement, a custom-made PCB fixture has been designed (see Fig. 11) to interface the impedance analyzer BNC ports and the layout's SMA ports. Two female–female SMA interfaces have been used to connect the layout to the PCB board. A small PCB with the same SMA connector's locations [see Fig. 11(c)] has been designed for short calibration. However, since MCPM layouts usually have inductance in the nH range, the impedance of the shorted fixture is quite significant to the MCPM loop inductance result. As seen in Fig. 11(c), the ABCD loop forms a shorted path for the current. In this case, the simulated value is between 9.1 and 8.4 nH for the selected frequency range. Therefore, one needs to consider both measurement and simulation for the most accurate comparison, and this additional inductance is extracted using Ansys Q3D for all selected frequency points (see Fig. 11). This shorted inductance value can be defined during the short calibration state in the measurement. The characterized models in Section III-B are used along with a partial element methodology to validate against the measurement results. Here, the loop-based method from [19] has been used to extract the total loop-inductance

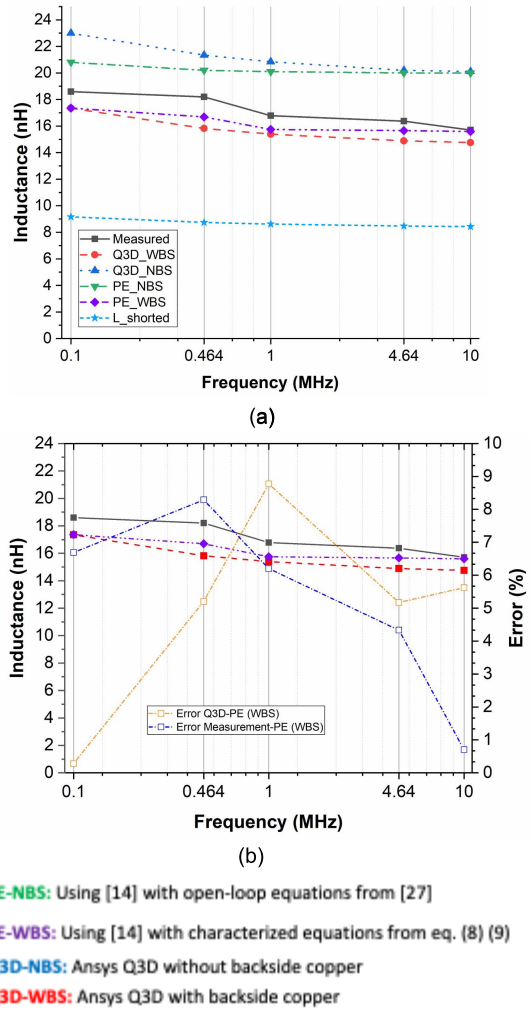

Fig. 12. (a) Comparison among different methods and measurements. (b) Error comparison among measurement and models with backside consideration.

for the lateral conduction paths in comparison to ANSYS Q3D results. Fig. 12(a) illustrates the comparison among different models. The results from PE-WBS are in good agreement

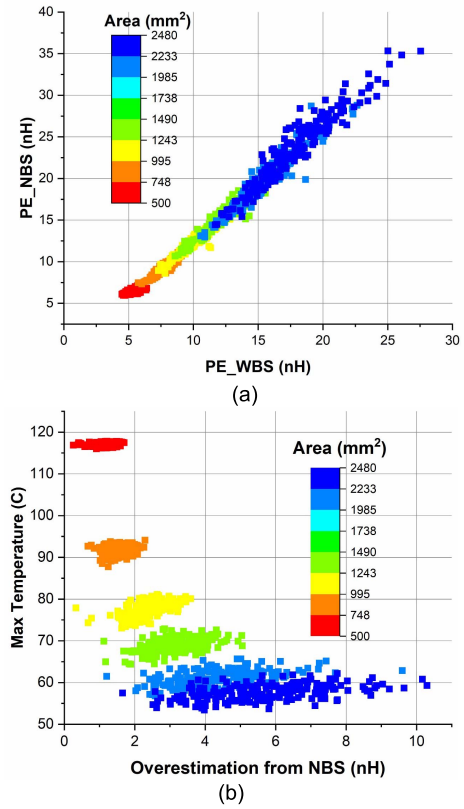

Fig. 13. (a) Direct comparison between two approaches. (b) Absolute difference between two approaches versus maximum temperature.

with Q3D-WBS and measurement results. The maximum error is only 8.5% between measurement versus PE-WBS and 9% between Q3D-WBS versus PE-WBS, while the minimum error is only 1% [see Fig. 12(b)]. On the other hand, the model without backside (NBS) copper shows about 4–6 nH, which is 30%–40% different in comparison to the measurement. These results have confirmed the importance of backside consideration in the extraction of trace inductance for MCPM layouts and shown that the method presented can model this effect with more than 90% accuracy.

B. Time and Memory Performance Comparison

The meshing effort for the MCPM structure can be significantly reduced by using the regression model. This, in turn, increases the performance of the partial element model, so the model can be used in an optimization process. In [19], it has been demonstrated that the loop-based approach is more efficient than the SOTA method in terms of speed and memory. However, the previous work in [19] did not include the backside impact. Hence, to illustrate the benefits of the method in this work, the extraction is performed on two more examples [see Fig. 10(b) and (c)] to have a comparison between this method and Ansys Q3D (see Table III). The experiment is run on an Ubuntu machine using a 2.2-GHz Intel Xeon Silver 4210 CPU. This experiment shows a maximum speedup of 34.6× in run time and 16.7× more memory-efficient using this method.

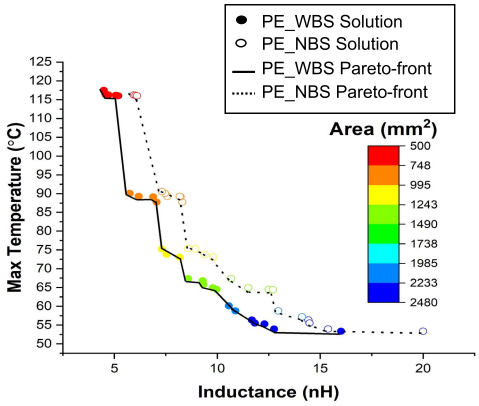

Fig. 14. Electrothermal Pareto frontiers' comparison between with and without backside consideration.

V. Layout Optimization and Circuit Simulation Study

A. Impact of Eddy Current on Layout Optimization

An optimization study is performed using both the PE-NBS and PE-WBS approaches to show the impact of eddy current consideration in a layout optimization problem. The models are implemented in the latest PowerSynth tool [41] where the layout generation algorithm in [31] allows a parametric study of multiple different footprint sizes, which has been used to generate the layout solution. The thermal model from [42] has been used through the application interface in [43] to demonstrate the impact of the eddy current on the optimized electrothermal solution space. Each of the device's heat dissipations is set to 10 W. The heat transfer coefficient is set to 150 W/m^2.K, and the ambient temperature is set to 300 K. The accuracy of the thermal model has been hardware validated in [31]; thus; it is not discussed in this work.

About 1200 layouts are generated with six different floorplan sizes ranging from 500 to 2475 mm^2. For each floorplan size, the maximum available area for randomization is calculated based on the difference between the minimum floorplan size and the given floorplan size. Then, the room is distributed following a weighted distribution to vary the trace dimensions and other components (i.e., devices and leads) locations. The time required for the 1200-layout inductance evaluation is about 2200 s using the PE-WBS or PE-NBS models. There is almost no difference in extraction time because (8) and (9) are simple and as fast as the open-loop equations from [35]. Conversely, it takes about 20 h using Ansys Q3D, which averages 35× speedups for each layout extraction. Fig. 13(a) shows the comparison between PE-NBS and PE-WBS models, and Fig. 13(b) shows the absolute difference between the two models versus maximum device temperature. As illustrated in Fig. 13(b), the maximum absolute difference between the two models increases with a larger floorplan, indicating that the PE-NBS model is more inaccurate with a larger floorplan size. A larger floorplan size is usually required for a more complicated MCPM layout (e.g., more devices per switching position). Therefore, the PE-NBS model is not recommended for circuit simulation of a more complicated MCPM layout. In addition, due to this inaccuracy, there is

TABLE III
EXTRACTION TIME AND MEMORY COMPARISON FOR DIFFERENT LAYOUT CASES

	This model			Ansys Q3D			Comparison		
ID	Ls (nH)	Runtime (s)	Memory (MB)	Ls (nH)	Runtime (s)	Memory (MB)	Error	Speedup	Memory
1	15.6	1.85	9.4	14.8	64	157	5.5%	× 34.6	1:16.7
2	18.4	1.5	4.7	17.4	40	74.5	5.7%	× 26.7	1:15.8
3	21.4	0.6	6.2	20.6	15	73.7	3.9%	× 25	1:11.8

TABLE IV
SELECTED OPTIMIZED LAYOUTS FROM PE_WBS PARETO FRONT

Layout ID	PE_WBS (nH)	PE_NBS (nH)	ΔL (nH)	Max Temp (°C)	Size (mm^2)
A	5.19	6.11	0.92	116	500
B	8.18	9.8	1.62	73.1	1050
C	11.83	14.87	3.04	55.3	2475

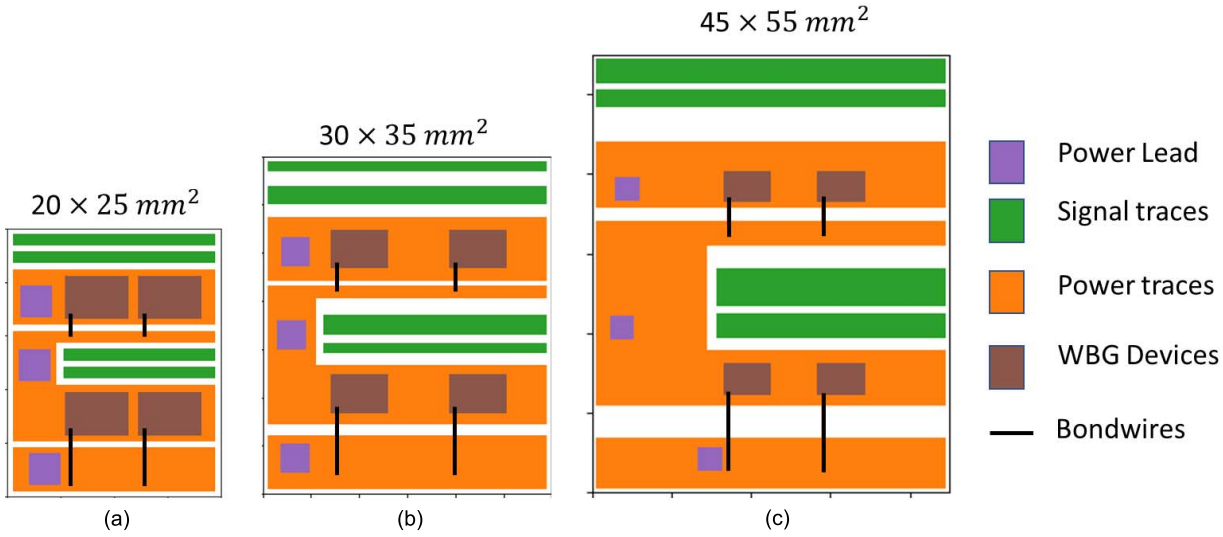

Fig. 15. Selected optimized layouts with various floorplan sizes. (a) 500 mm^2. (b) 1050 mm^2. (c) 2475 mm^2.

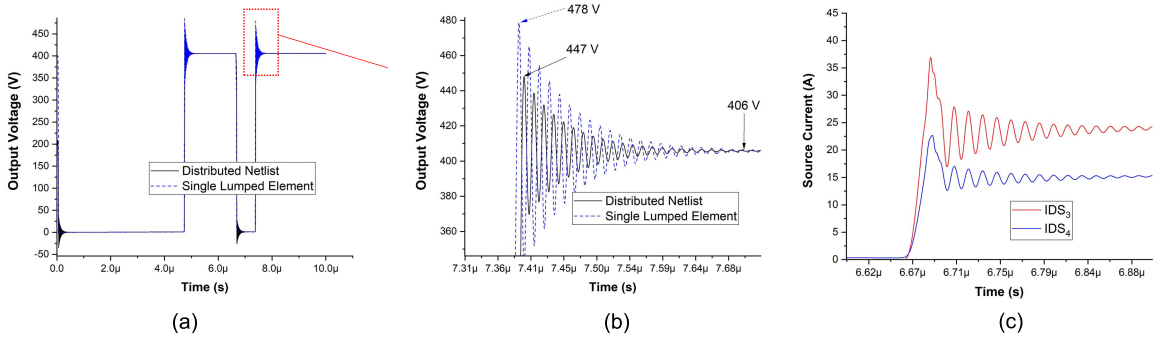

Fig. 16. (a) DPT VDS waveform, (b) zoomed-in view of VDS, and (c) source current comparison on lower side devices.

a shift in the optimized Pareto front using PE-NBS and PE-WBS models (see Fig. 14). Table IV shows the error comparison of some optimized solutions (see Fig. 15) selected from the PE-WBS Pareto front. The error margin expands with increased floorplan sizes. Despite the large error due to ignorance of eddy current, the PE-NBS model still shows the same trend within the same floorplan size [see Fig. 13(a)]. Therefore, one can still apply the PE-NBS to minimize the loop inductance for a fixed floorplan size problem. However, the extracted parasitic result is inaccurate for the further circuit simulation study. In this case, the characterization steps described in Section III above can be applied to improve the accuracy of the extracted parasitic parameters. In addition, as shown in Table II, this process only takes about 15 min to complete for a selected DBC substrate. Therefore, this characterization process can be applied to any partial element models (e.g., [14], [16], and [19]) to improve the extraction accuracy.

B. Circuit Simulation Study

The loop-based approach in this work also allows a distributed netlist generation, enabling a postlayout circuit simulation study and verification of a selected solution. While this process can be done using PEEC or FEA methods, it requires more effort to set up and run simulations, as discussed in [10]. A double-pulse test (DPT) circuit simulation is performed in LtSpice to demonstrate the importance of the distributed netlist. Here, for the half-bridge layout in Fig. 10(a), four CPM2-1200-0040B from Wolfspeed are switched with dc–dc voltage of 400 V, and the two pulses are shown in Fig. 16(a), where the rise and false times of the gate signal are 50 ns. The total load current is 40 A through the load inductor of 50 μH. The LtSpice device models [44] have been used to ensure the most accurate simulation results. Two simulations are run to compare the distributed netlist extracted from the model using the process in Section III-D and a single lumped element for the loop inductance of 15.5 nH at 10 MHz. As shown in Fig. 16(b), with the same loop inductance, the ringing oscillation in both cases shows the same resonance frequency of about 70 MHz. There is a 31-V difference in the peak overshoot voltage using the lumped versus the distributed model, which is about 75% difference, if a single lumped element is used. This is because, in the single lumped element, the simulation does not capture the switching behavior of each device correctly. On the other hand, the distributed netlist allows a more accurate analysis of the interaction between the layout parasitic parameters and device parameters (e.g., Ciss, Coss, and Crss). More importantly, a more detailed analysis of the current sharing among devices can be done using the distributed netlist [see Fig. 16(c)]. In the future, this would help the optimization tool decide on a more optimized layout in terms of current balancing.

VI. Conclusion

In this work, a parasitic extraction method is presented, combining a regression-based characterization process with a loop-based approach to capture the eddy current impact on MCPM layout. This method is more efficient than FEA simulation while showing less than 10% error compared to simulation and measurement for a broad frequency range. This method has shown a maximum speedup of 35$\times$ while being 17$\times$ more memory-efficient. While this method cannot beat the FEA approach in terms of flexibility, the method is more suitable in the design automation framework for MCPM layouts. Therefore, the method has been used in optimization tools, such as PowerSynth, for fast and accurate parasitic extraction. In the future, the accurate extracted parasitic results through a distributed netlist can be used to accurately predict power module dynamic performance aspects, such as voltage overshoot, current sharing, or gate signal instability.

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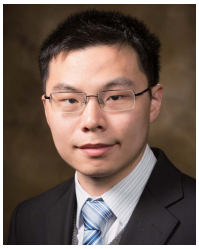

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