This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2022.3175150, IEEE Journal of Emerging and Selected Topics in Power Electronics

Fast and Accurate Parasitic Extraction in Multichip Power Module Design Automation Considering Eddy-Current Losses

Quang Le, *Student Member, IEEE*, Imam Al Razi, *Student Member, IEEE*, Tristan M. Evans, *Student Member, IEEE*, Shilpi Mukherjee, *Student Member, IEEE*, Yarui Peng, *Member, IEEE, and H. Alan Mantooth, Fellow, IEEE*

***Abstract*—Recent studies in power electronic design automation have introduced various models for parasitic extraction of multichip power module layouts. However, none of these studies consider the eddy current effect in the direct-bonded-copper substrate, accounting for 40-50% error in the extraction result. This work introduces a methodology for eddy-current consideration through numerical simulation and regression modeling. The regression model utilized in the characterization process in this work is fast and memory-efficient compared to the finite element approach. This characterization process can improve the accuracy of any partial element model without sacrificing performance. Combining this characterization process and partial element approach achieves less than 10% extraction error compared to Ansys Q3D while showing a maximum speed-up of 35× and 17× more memory efficiency. This method also significantly reduces the number of elements in the extracted netlist and the complexity of loop evaluation. This method is attractive for use with optimization routines and therefore has been used successfully in a layout optimization tool.**

***Keywords*—PowerSynth, Multi-Chip Power Module (MCPM), Design Automation, Inductance Extraction, Regression Model**

I. Introduction

The emerging research in multi-chip power module (MCPM) technologies have utilized the benefits of the Wide Bandgap (WBG) devices thanks to their higher thermal conductivity and current carrying characteristics [1, 2]. While WBG devices offer many known advantages such as higher blocking voltage, faster-operating frequency, and higher junction temperature, they also bring many challenges to the MCPM layout design, making this design process a multidisciplinary problem. Some main design aspects include electrical parasitics, thermal management, or mechanical reliability [3–5]. Among these design aspects, electrical design is the most crucial target for any MCPM layouts [6–8], and this aspect is a multidisciplinary problem in and of itself. The coupling among layout and WBG device parasitic parameters and high di/dt and dv/dt during the transient produces many undesirable dynamics. These dynamics form high voltage overshoot (L·di/dt), leading to failure in the semiconductor device, increased switching losses, and reduced system-level efficiency [9–11]. Additionally, instability issues such as false turn-on and self-sustained oscillation can occur if the layout is not designed correctly [12, 13]. Therefore, electrical parasitics analysis, especially parasitic inductance extraction, is crucial to designing a proper MCPM layout. More importantly, fast and accurate electrical parasitic modeling is a required design target in emerging MCPMs layout design automation and optimization trends. Generally, to achieve a fast and accurate extraction of the MCPM layout structure, the model has to capture two critical physical aspects accurately (Fig. 1 a): 1) the proximity effect among parallel conductors on of the lateral surface, and 2) the induced eddy current on the DBC backside. Finite Elements Analysis (FEA) simulation tool such as Ansys Q3D considers these effects accurately by solving Maxwell equations. While accurate, FEA tools require substantial computational resources through solving magnetic and electric integral equations. Hence these tools are

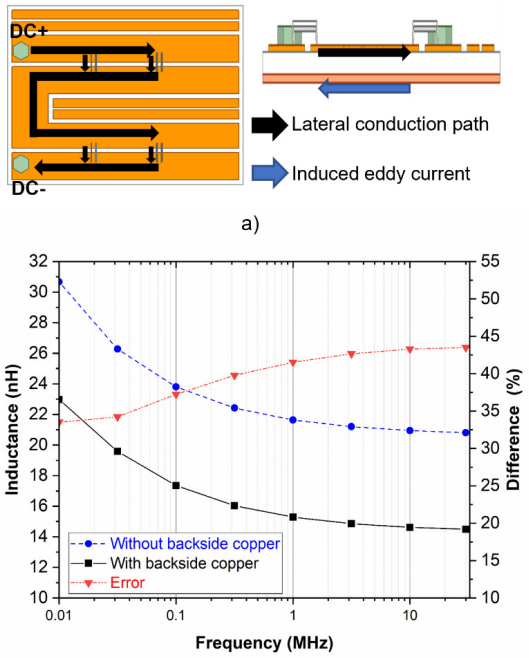


Fig. 1. a) Lateral versus eddy current paths in an MCPM b) the impact of eddy current on extraction result from Ansys Q3D

This material is based on work supported by The National Science Foundation under Grant No. EEC-1449548 and Army Research Lab Contract No. W911NF1820087. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not reflect the views of the National Science Foundation or Army Research Lab.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2022.3175150, IEEE Journal of Emerging and Selected Topics in Power Electronics

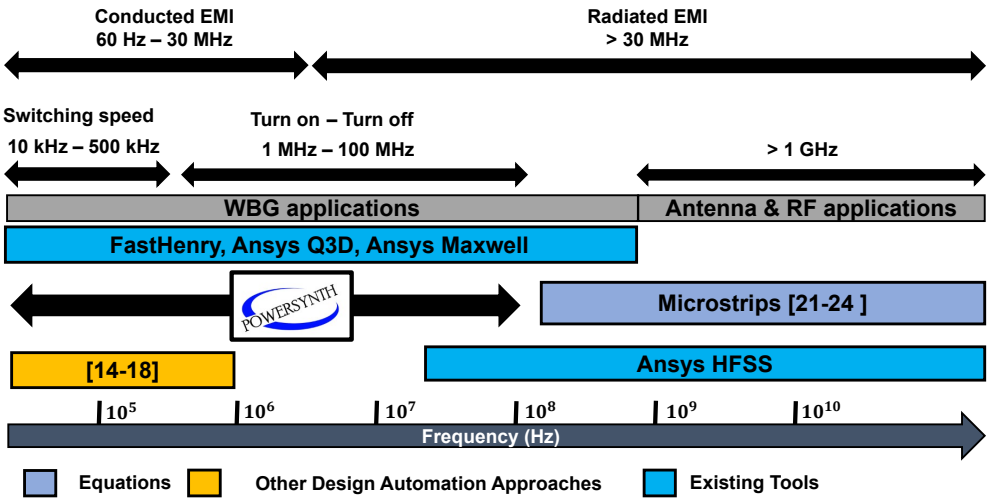


Fig. 2. Inductance extraction frequency range for WBG application and PowerSynth's target frequency range versus other approaches

only suitable for a single manual layout design and not very attractive for design automation. To fill the parasitic inductance modeling gap for the power electronic design automation, many research groups have offered self-developed models [14–19] to extract the layout parasitics parameters quickly. These models accurately capture lateral current commutation, which is crucial in reducing the parasitic loop inductance. However, these models often ignore the eddy current effect, leading to the possible overestimation of parasitic extraction results. This induced eddy current often exists on the backside copper of the DBC, which also often acts as a shielded ground plane. The half-bridge layout in Fig. 1 shows a maximum of 43% overestimation in the extraction result without eddy current consideration using Ansys Q3D. This overestimation can go up to 80%, as reported in [20]. While ignoring eddy current impact might not affect the optimization results of the lateral loop, this can lead to a high inaccuracy in voltage overshoot or gate-loop stability simulation. Therefore, the methodology in this work describes a regression model formulation through a trace characterization process. These regression models are used in a loop-based method for fast and accurate loop evaluation with a distributed netlist extraction capability. This combination of regression model and loop-based evaluation method enables a fast evaluation of parasitic parameters giving accurate electrical design insights in an optimization routine.

II. Literature Review

A. Extraction Frequency Range for MCPMs.

There has been extensive study on impedance models which consider eddy current effects in other fields. One such example includes closed-form analytical equations for the parasitic inductance of microstrip structures. These microstrip models are commonly used in Printed Circuit boards (PCB) for antenna applications [21–23], with much smaller trace width and conductor thickness than DBC. These models are only correct for very high-frequency applications (GHz range). At this high-frequency range, the microstrip model assumes zero thickness conductors due to the sub-micron thickness value of the skin depth at the RF frequency region. Some microstrip models require complex integral or numerical evaluation, which is not computationally attractive for design automation [23]. An approximate Partial Elements Equivalent Circuit (PEEC) based on a 2-D method expression for eddy-current losses has been derived in CMOS monolithic inductors and transformers design [24]. This method ensures accurate extraction for a high-frequency range (100 MHz – 14 GHz). However, it also requires numerical integration for the self and mutual impedances, which is quite computationally expensive.

In WBG applications, turn-on and turn-off rates of WBG devices dictate the concerned frequency range for MCPM. As reported from the literature, these values are about 27-50 ns for SiC and 5-10 ns for GaN devices [1, 2]. These turn-on and turn-off rates limit the frequency range for inductance extraction in an MCPM layout. Additionally, an accurate parasitic model is also required for the conducted Electromagnetic Interference (EMI) analysis [25]. Hence, the effective frequency range for MCPM parasitic extraction needs to be accurate in the 10 kHz-30 MHz range (Fig. 2). In this frequency range, quasistatic approximation techniques such as Method of Moments (MoM), PEEC [26], and other partial elements approximation models are used to extract the layout inductance. These models have been used in state-of-the-art (SOTA) analysis tools such as Ansys, COMSOL, or the high fidelity open-source analysis tool such as FastHenry [27]. While suitable for broadband frequency extraction, these models are usually computationally expensive, making it unfavorable for an optimization routine. In addition, it is hard to extract a distributed netlist for the further circuit simulation study. For example, MoM techniques usually report a single loop-inductance value. On the other hand, PEEC provides a dense matrix with hundreds of thousands of elements. The designer needs to take an extra step to extract a multi-port netlist, which requires more computational effort.

B. Parasitic Extraction Models in Power Electronics Design Automation.

In design automation and layout optimization studies, the parasitic extraction models are usually modified or simplified

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2022.3175150, IEEE Journal of Emerging and Selected Topics in Power Electronics

to speed up the extraction time while maintaining acceptable extraction accuracy [14–19]. However, at the time of this writing, the induced eddy current is not considered in parasitic extraction modeling in many MCPM design automation studies. For example, in [18], the author applied the MoM method to extract the parasitic loop inductance for layout optimization. This method claims to have a good agreement with state-of-the-art simulation tools and is efficient for layout optimization; however, the method only considers the current commutation on the top layer of the DBC, which gives overestimated parasitic loop result. Unlike MoM, which usually requires many mesh elements, the partial elements method divides the layout into long and thin segments, which reduces the total number of elements. Therefore, the partial elements method has been used more often in recent studies [14–17]. For instance, in [14], a tool named Current-Bunch is developed where the model divides the MCPM layout into many parallel long segments, namely current bunches. Each segment width in this Current Bunch tool is set to be close to the skin depth value at the extraction frequency, accurately capturing the proximity effect in the lateral conduction path. Each segment self-inductance and segment-segment mutual inductance are evaluated using existing analytical equations. However, these equations are developed for open-loop cases where the current is assumed to return at infinity. This equation is not applicable for DBC-based MCPMs since the backside copper of the DBC substrate acts as a ground plane and a magnetic shield which reduces the total loop inductance significantly.

There are two main goals for the electrical model used in the MCPM layout optimization tool PowerSynth [28]: 1. Fast and accurate extraction of MCPM parasitic parameters and 2. a distributed netlist generation for fast, post-layout optimization circuit analyses. PowerSynth employs a different approach to consider eddy current: the self-inductance values with eddy current consideration are first extracted through running many FEA simulations where the response surface method [29] has been used to fit the simulated data to the geometrical parameters of MPCM trace. Through this initial computationally expensive characterization process, the characterized self-inductance model can be reused many times during layout optimization which reduces the computational effort during this optimization process. The work in [30] combines PEEC and response surface models to improve extraction accuracy, which has been experimentally validated in [31]. However, as the PEEC matrices are dense and contain many elements, it is not scalable for more complex MCPM layouts with many parallel devices.

In the previous PowerSynth papers, the focus was on the layout optimization algorithm and lacked a thorough description of the parasitic extraction methodology itself. Moreover, the models described in [29] requires running simulation tools such as FastHenry or Ansys Q3D to build the response surface method. These approaches also require scripting knowledge for these simulation tools, making it hard for other researchers to reimplement the model. Therefore, this paper carefully explains the physics behind the eddy current effect and details an analytical approach for the regression model formation. Incorporating the loop-based approaches from Very-Large-Scale-Integration (VLSI) [32–34], the method developed in [19] is developed and improved for trace model characterization and the lateral evaluation of the MCPM layout. A relative comparison between this model and the previously mentioned models have been shown in Table. I. This result has shown that this model is most suitable for layout optimization purposes. Furthermore, the model also provides a reduced order distributed netlist extraction which benefits post-layout circuit simulation study.

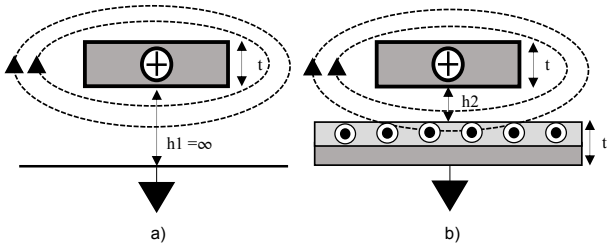


Fig. 3. Magnetic fluxes in a) Open-loop case b) MCPM case, where hi is the distance to ground plane, δ is the skin-depth value, and t is the copper thickness

III. Methodology and Theoretical Background

A. The Physics behind Eddy Current

In short, an alternating current in a nearby conductor creates an alternating magnetic field in the plane perpendicular to the conduction path. This alternating magnetic field in turn creates an induced current in the backside copper which flows in the opposite direction to the alternating current from the source. In the case of MCPMs, the resulting induced current on the backside copper from the alternating current on the topside forms a loop. Fig. 3 shows the differences between the open-loop case and the MCPM case. In the open-loop case, the current is assumed to return in a plane infinitely far from the conduction path which results in much higher inductance value. Hence, using formulas for the open-loop self-inductance results in an overall overestimated loop value. A simulation study is performed to see the impact of the backside current density versus frequency. A simple MCPM trace structure is built in ANSYS Q3D with the width of 1mm, length of 25 mm and thickness 0. 2 mm on top of an alumina DBC substrate with 0.64 mm isolation layer (Fig. 4). As seen in Fig. 4b, the result shows that eddy current concentrates below the trace, the current density peaks at the center location of the trace and gradually decreased at the locations further from the center. The eddy current value becomes insignificant at a fixed distance x0 from the center. Therefore, the resulted trace inductance will be same for the backside copper width greater than W=2×x0.

$$\delta = \sqrt{\frac{2}{\omega u \sigma}} \tag{1}$$

From Maxwell equations, the work in [18] developed a closed form equation for the current density of a microstrip trace on PCB:

$$J_{gr}(x) = \frac{I_i}{w\pi}[\arctan\frac{w-2x}{2h} + \arctan\frac{w+2x}{2h}] \tag{2}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2022.3175150, IEEE Journal of Emerging and Selected Topics in Power Electronics

Table I: Comparison among Existing Parasitic Extraction Methods for MCPM

Approach	Eddy Current	Extraction time	Accuracy	Flexibility	Distributed Netlist	Broadband
PEEC [26]	Yes	Slow	Very High	Very High	Hard to extract	Yes
Ansys Q3D	Yes	Slow	Very High	Very High	Hard to extract	Yes
FastHenry [27]	Yes	Average	Very High	Very High	Hard to extract	Yes
Horowitz [16]	Yes	Not Mentioned	Acceptable	High	Not mentioned	Yes
Ning [18]	No	Fast	Not Mentioned	High	Not mentioned	No
Current Bunch [14]	No	Fast	High	High	Yes (R, L, and M)	No
PowerSynth v1.1 [28]	Yes	Very Fast	Acceptable	Low	Yes (only R, L)	Yes
PowerSynth v1.9 [31]	Yes	Average	High	High	Yes (only R, L)	Yes
This work and [19]	Yes	Fast	High	High	Yes (R, L, and M)	Yes

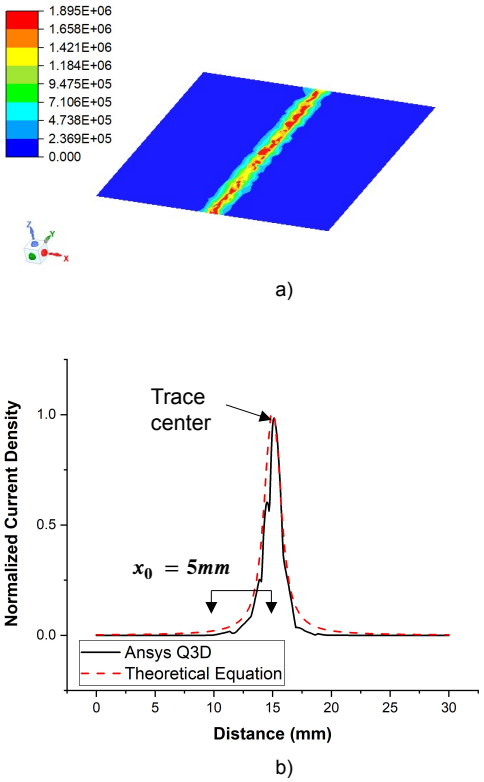


Fig. 4. a) Backside current density at 10 MHz b) Normalized current density distribution

where Ii is the total current through the trace (normalized to 1A), w is the trace width, x is the distance from the trace center, and h is the distance from the trace to backside.

As can be seen from Eq. (2), this current density value is independent of trace length and thickness. With increasing isolation thickness h, the eddy current density also reduces. Fig. 4b shows the normalized distribution of the current density using Eq. (2) versus simulated result from Ansys Q3D. As seen in the results from Fig. 4b, the numerical simulation shows the same distribution versus the theoretical case using Eq. (2). Therefore, this equation can be used to evaluate x0 value where eddy current zeroed out.

B. Self-inductance and Mutual Inductance Extraction for MCPM Traces

Under the scope of design automation and optimization, self and mutual inductance models must be fast while maintaining accuracy. In this paper, input parameters are formed, where numerical simulations are run to collect the self and mutual inductance values. The results from these numerical simulations can be collected to form equations for L_{trace} and M_{trace}, which are later used in partial element methodology to evaluate the layout's lateral loop. This process in demonstrated in Fig. 5.

1) Input Parameters: A Design of Experiment (DOE) is first required to form the input parameters for the simulation. In the case of the MCPM application, the parameters are divided into two different sets. The first set is fixed parameters, including material, conductor thickness, and isolation thickness. These parameters are always provided in DBC's vendor datasheet. Because there is a limited number of DBC types, the model can be built only once for each different DBC configuration. The second set is the actual input parameters for the model, as illustrated in Fig 6. For the self-inductance model this is width W and length L of the trace. For the mutual inductance model the input parameters are the trace widths W, trace length L and the distance between two traces d. Next, appropriate widths and lengths values are needed for the model fitting for the self- inductance, while distance values are needed for mutual inductance. In this case, the minimum trace width range is decided by the skin-depth at 100 MHz where minimum trace length is set to 5× of this value. The maximum trace width is set to 1 mm and the maximum trace length is 25 mm accordingly. A 2D matrix of different trace widths and lengths can be formed using these ranges. In the case of mutual inductance, the distance range is set from 0 mm to 10 mm. Finally, the backside copper width can be defined through the datasheet parameters and trace widths values using Eq. (2). This equation has been used to make sure the model capture most of the eddy-current impact. These input parameters cover some common dimensions from MCPM layout. This places some initial boundaries on the model prediction range. The extraction data can be stored and continuously updated if there are any updates in the input parameters.

2) Impedance Extraction Using Loop-based Extraction Method: In the Extraction step, a structure in Fig. 6 is setup using the input parameters. FEA simulations can be used here to extract the self and mutual inductance values. However, this process can be very computationally expensive, for this structure, a partial element approach is much more efficient. Therefore, the loop-based method [19] is modified to extract the trace resistance, inductance and mutual inductance values considering the backside effect. In this approach, the structure is meshed into parallel, thin and long filaments. To ensure accurate extraction, the filament width is set to the skin-depth

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2022.3175150, IEEE Journal of Emerging and Selected Topics in Power Electronics

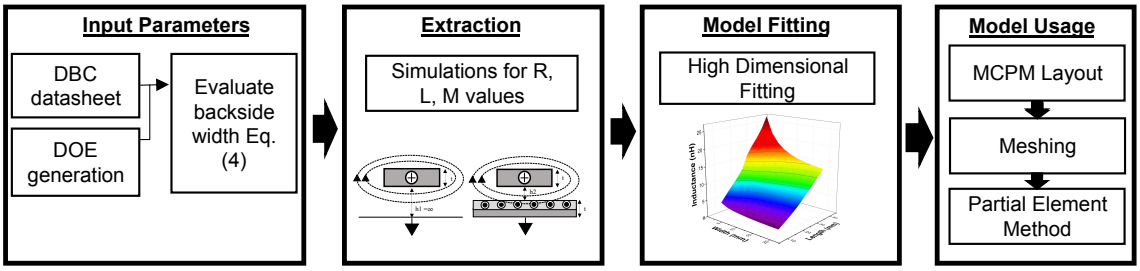


Fig. 5. Model characterization process

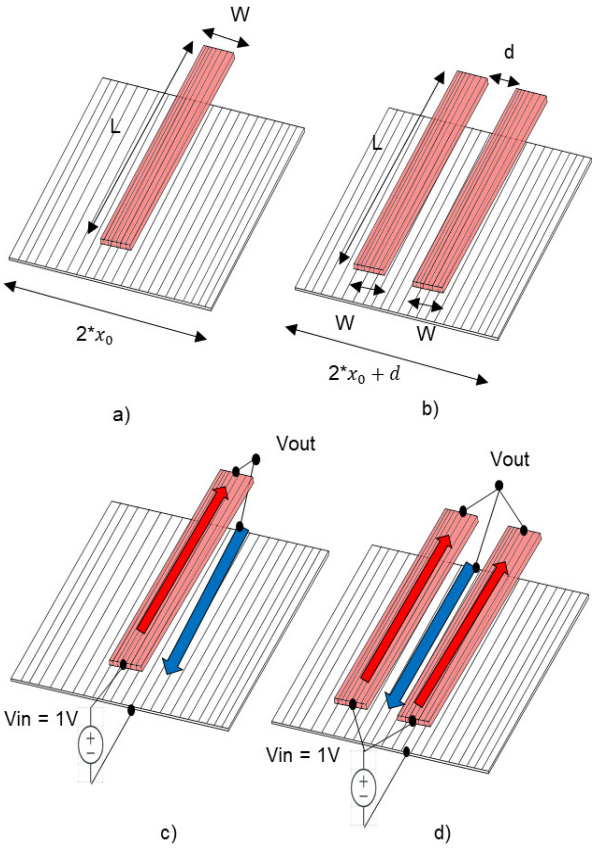


Fig. 6. Input parameters for a) a single trace b) mutual inductance between traces; Simulation setup for c) single trace impedance d) mutual inductance

of the maximum extracted frequency. Next, a set of analytical equations can be used to compute the resistance, inductance, mutual inductance for the filaments [35]. All impedance values are stored in an n-by-n matrix **P** where n is the total number of elements, **P**(i, i) is the partial self-impedance, and **P**(i, j) is the partial mutual impedance between element i and j. Then, an n-by-k mesh matrix **M** is formed where k is the number of forward current elements. In this matrix **M**, if an element i is in the forward current path, **M**(i, j) is 1, and 0 otherwise. A column vector **u** is also formed with n rows of one, this is a normalized vector for the voltage drop across each trace. Two equations are then formed and evaluated as shown below:

$$Pa = u \quad \text{and} \quad PB = M \tag{3}$$

Vector **a** is used to compute the current distribution in each element, which is unified to have a norm sum of 1. The result from matrix **B** along with this unified vector is then used to obtain the current matrix **I**, whose j-th column vector **I**(j) can be calculated using:

$$I(j) = B(j) - V_{out} \times a \quad \text{where} \quad j = 1, 2, ..., n \tag{4}$$

where:

$$B_{out} = \frac{\sum B(i,j)}{\sum a} \tag{5}$$

let k be the total number of loops forming from the top-trace and backside. The total current through each loop is computed by:

$$I_{trace} = M^T \times I \tag{6}$$

then:

$$Z_{trace} = (M^T \times I_{trace})^{-1} \tag{7}$$

The extraction is performed for all variation of parameters and the extracted frequency (f). The results for R_{trace}, L_{trace}, and M_{trace} are stored in table form for the model fitting process. Fig. 7 shows the comparisons among the extraction using different models and for some selected input parameters. The result shows error within 6% between the loop-based method versus Ansys Q3D for both self and mutual inductance extraction. The open-loop equation shows 30-40% error for both self and mutual inductance cases. Table II shows the memory and time comparisons using the loop-based method versus FEA simulation using Ansys Q3D. On the same computer, for this simple structure, the model is 7× faster and 62× more memory efficient than FEA approach.

Table II: Performance versus Ansys Q3D for L and M Characterization

	Ansys Q3D		Loop-based	
# Run	Time	Memory	Time	Memory
1	70 s	310 MB	9 s	5 MB
100	1 h 40 m	310 MB	15 m	5 MB

3) Regression Methodology for Model Characterization: Once all extraction results are collected, regression models can be built to evaluate for trace impedance values quickly. The Python Scikit-Learn library [36] offers many different regression techniques such as linear, polynomial, support vector, artificial neural network and so on... However, among these existing methodologies, the polynomial regression method is the most suitable for fitting the impedance equations. This is because this model allows a nonlinear fitting while having a simple equation form. The general polynomial equation forms in Eq. (8) and (9) have been used here to fit the model:

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2022.3175150, IEEE Journal of Emerging and Selected Topics in Power Electronics

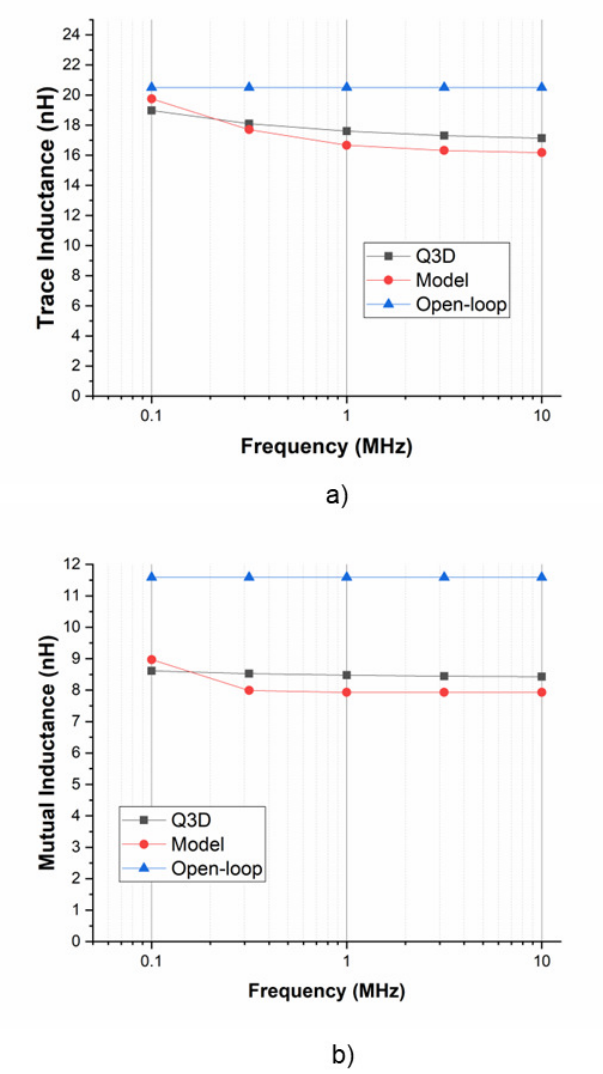


Fig. 7. L and M extraction results comparison among different approaches for a) w=1mm, l =25 mm, b) w=1mm, l =25 mm, d= 1mm

$$f_{RL}(W,L) = \sum_{0}^{K} a_k W^k + \sum_{0}^{K} a_k L^k + \ldots + \sum_{0}^{M} a_m W^m L^m \quad (8)$$

$$f_M(W,L,d) = \sum_{0}^{K} a_k W^k + \sum_{0}^{K} a_k L^k + \sum_{0}^{K} a_k d^k + \ldots + \sum_{0}^{M} a_m W^m L^m d^m \quad (9)$$

where W is width in mm, L is length in mm, d is distance in mm, a_i are coefficients to be fitted, K is the number of degrees, and M is the number of interaction features.

A third order polynomial ensures a fitting error of less than 10% for $R_t race$ and 1% for$L_t race$. As for the mutual inductance model, a fourth order polynomial equation form ensures a fitting error of less than 1%. Once the model is characterized, it can be reused many times for the same DBC structure. More importantly, the characterized model is much faster and memory efficient than the simulation. Hence it can be used in any partial element solver to evaluate the MCPM electrical parasitic parameters.

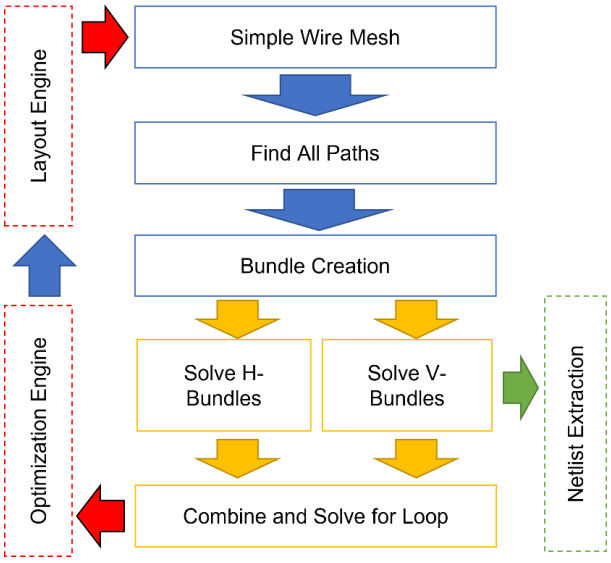


Fig. 8. Loop based method extraction flow

Algorithm 1: Digraph formation

```
Input  : Initial Wire Mesh Graph (G)
Output: Digraph from source to sink (D)
if exist_path(G,source,sink) then
    paths = depth-first-search(source,sink)
else
    raise error: no path exist
    return
for i ← 0 to len_of(paths) do
    /*Get the array of nodes on paths*/
    p = paths[i]
    /*Loop through all node to form digraph*/
    for j ← 0 to len_of(p)-1 do
        if not(exist_path(D, p[j], p[j+1]) then
            add edge(D, p[j], p[j+1])
```

To consider the broad frequency band effect, the model is characterized in both low (<1 kHz) and high frequency region (> 10 MHz). Then a ladder circuit model in [37] can be used to effectively estimate the inductance value for any frequency points. As mentioned in [37], this ladder circuit model is accurate for maximum frequency of 6 GHz well beyond the frequency range considered for MCPM applications (Fig. 2). Similar to self-inductance, the mutual inductance value is also frequency dependent. However, there is no known circuit model in the literature for the mutual inductance versus frequency. Hence, to have the best approximation value for all frequency points, the mutual inductance model is built for every first frequency point per decades between DC and 30 MHz.

4) Using the Regression Model in Loop-based Extraction Method: Fig. 8 illustrates the design flow of the loop-based method [14] to solve for MCPM lateral-loop parameter. To begin with, a layout geometry from the layout engine [26] is transformed into a wire mesh using trace-edge location, device location, and bondwire landing location. These locations are represented as nodes where edges are formed if they share the same layout traces or bondwires. A pathfinding based on

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2022.3175150, IEEE Journal of Emerging and Selected Topics in Power Electronics

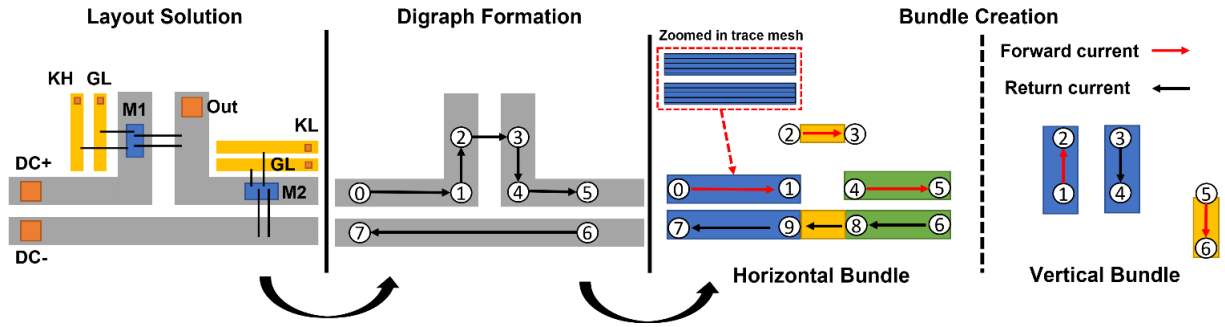


Fig. 9. The layout to bundle formation process

depth-first search algorithm [38] (shown in Algorithm 1) finds all existing paths from the source and sink and transformed the wire mesh into a directed graph (Fig. 9). The directed graph is further divided into two groups of horizontal and vertical bundle with defined forward and return current directions. Also, for each bundle, a uniform mesh (Fig. 9) is formed to consider the proximity effect among traces. While this might look similar to the current-bunch concept in [10], the key difference is using Eq. (3) to capture the current distribution among parallel traces. This gives a better frequency transition, whereas in [10], each current-bunch object is assumed to have a uniform current distribution. Finally, using Eq. (4) – (8) above, the loop impedance for all horizontal and vertical bundles can be evaluated. Here, to consider the eddy current impact, , Eq. (8) and (9) have been used in the formation of partial impedance matrix P. Once all impedance values for the bundles are updated, the impedance of each bundle is calculated, they are stored in a square matrix A with the size of N×N for N is the total number of horizontal and vertical loops. The loop impedance is then simply calculated using:

$$AI_i = V_i \tag{10}$$

where I_i is the current vector for the total current through each loop and V_i is the input voltage vector.

By dividing the layout into multiple bundles, the total complexity for this algorithm is $O(N \times E^2)$ where E is the average number of elements in each bundle. The value of E is usually very small in the case of an MCPM layout.

IV. Experimental Validation and Performance Comparison

A. Experimental Validation for a Selected Layout Case

A Device Under Test (DUT) for a 2D half-bridge layout is fabricated on an Alumina DBC substrate with a copper thickness of 0.2 mm and an isolation thickness of 0.64 mm (Fig. 10a). The layout is designed for a half-bridge circuit with two devices for each switching position on a 39.5 × 52 mm2 footprint. However, bond-wires connections are used to form shorts at the locations of the devices to form the loop between DC+ and DC-. Two SMA connectors are connected to DC+ and DC- locations on the DUT to interface with the impedance analyzer (Fig. 11d). A Keysight E4990A impedance analyzer has been used to measure many power electronics systems in the literature [39, 40] and has also been used in this work to verify the power loop inductance against the extraction results.

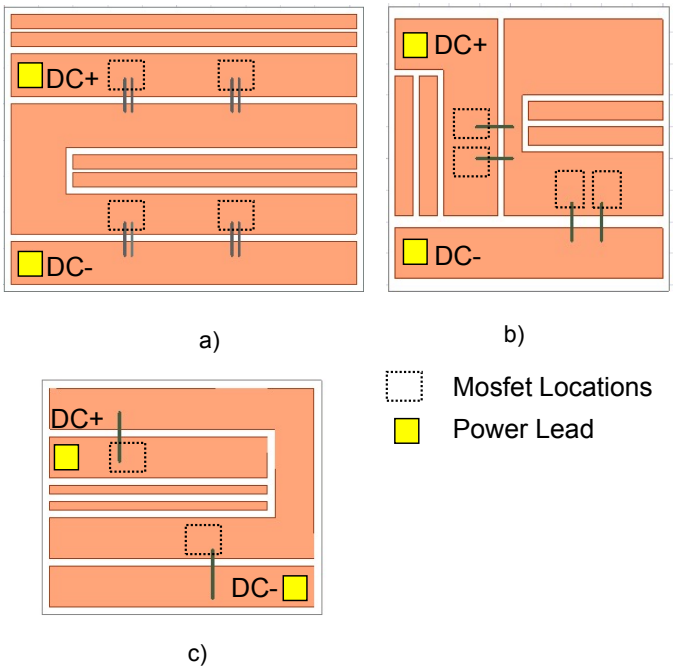


Fig. 10. a) Layout-1 (52×40 mm2) design under test (DUT) for experimental validation b) Layout-2 (50×47 mm2) c) Layout-3 (35×28 mm2)

While E4990A is capable of impedance measurement between 20 Hz and 30 MHz, there is a limit in the impedance resolution making the impedance lower than 100 kHz inaccurate. There is a very small change in inductance for the frequency range greater than 10 MHz. Therefore, the frequency range has been selected between 100 kHz to 10 MHz for this measurement.

This impedance analyzer requires 4 BNC connections for high-low currents and high-low potential ports (HCur, LCur, HPot, and LPot in Fig. 11a). Hence, for this measurement, a custom-made PCB fixture has been designed (Fig.11) to interface between the impedance analyzer BNC ports and the layout's SMA ports. Two female-female SMA interfaces have been used to connect the layout to the PCB board. A small PCB with the same SMA connector's locations (Fig. 11c) has been designed for short calibration. However, since MCPM layouts usually have inductance in the nH range, the impedance of the shorted fixture is quite significant to the MCPM loop inductance result. As seen in Fig. 11c, the ABCD loop form a shorted path for the current. In this case, the simulated value is between 9.1 to 8.4 nH for the selected frequency range. Therefore, one needs to consider both mea-

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2022.3175150, IEEE Journal of Emerging and Selected Topics in Power Electronics

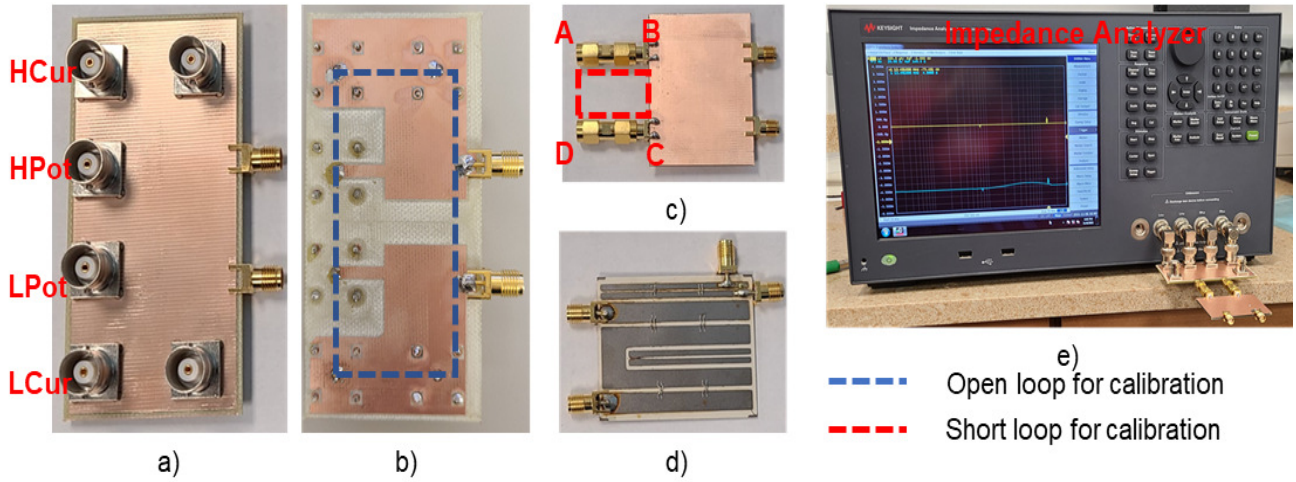


Fig. 11. a) topside of custom-made PCB fixture b) bottom side of PCB fixture c) board for short calibration d) design under test layout e) impedance analyzer

surement and simulation for the most accurate comparison and this additional inductance is extracted using Ansys Q3D for all selected frequency points (Fig. 11). This shorted inductance value can be defined during the short calibration state in the measurement. The characterized models in the previous section are used along with a partial element methodology to validate against the measurement results. Here, the loop-based method from [19] has been used to extract the total loop-inductance for the lateral conduction paths in comparison to ANSYS Q3D results. Fig. 12a illustrates the comparison among different models. The results from PE-WBS are in good agreement with Q3D-WBS and measurement results. The maximum error is only 8.5% between measurement versus PE-WBS and 9% between Q3D-WBS versus PE-WBS while the minimum error is only 1% (Fig. 12b). On the other hand, the model without backside (NBS) copper shows about 4-6 nH which is 30-40 % different in comparison to the measurement. These results have confirmed the importance of backside consideration in the extraction of trace inductance for MCPM layouts and shown that the method presented can model this effect with more than 90% accuracy.

B. Time and Memory Performance Comparison.

The meshing effort for the MCPM structure can be significantly reduced by using the regression model. This in turn increases the performance of the partial element model so the model can be used in an optimization process. In [19], it has been demonstrated that the loop-based approach is more efficient than SOTA method in terms of speed and memory. However, the previous work in [19] did not include the backside impact. Hence, to illustrate the benefits of the method in this work, the extraction is performed on two more examples (Fig. 10b and Fig. 10c) to have a comparison between this method and Ansys Q3D (Table. III). The experiment is run on an Ubuntu machine using 2.2 GHz Intel Xeon Silver 4210 CPU. This experiment shows a maximum speedup of 34.6× in run time and 16.7× more memory efficient using this method.

V. Layout Optimization and Circuit Simulation Study

An optimization study is performed using both the PE-NBS and PE-WBS approaches to show the impact of eddy current consideration in a layout optimization problem. The models are implemented in the latest PowerSynth tool [41] where the layout generation algorithm in [31] allows a parametric study of multiple different footprint sizes, which has been used to generate the layout solution. The thermal model from [42] has been used through the application interface in [43] to demonstrate the impact of the eddy current on the optimized electrothermal solution space. Each of the device heat dissipation is set to 10 W. The heat transfer coefficient is set to $150W/m^2.K$, and the ambient temperature is set to 300K. The accuracy of the thermal model has been hardware validated in [31]; thus; it is not discussed in this work.

About 1200 layouts are generated with six different floorplan sizes ranging from 500 mm^2 to 2475 mm^2. For each floorplan size, the maximum available area for randomization is calculated based on the difference between the minimum floorplan size and the given floorplan size. Then, the room is distributed following a weighted distribution to vary the trace dimensions and other components (i.e., devices, leads) locations. The time required for the 1200 layouts inductance evaluation is about 2200 s using the PE-WBS or PE-NBS models. There is almost no difference in extraction time is because of Eq. (8) and (9) are simple and as fast as the open-loop equations from [35]. Conversely, it takes about 20 hours using Ansys Q3D, which averages 35× speedups for each layout extraction. Fig. 13a shows the comparison between PE-NBS and PE-WBS models, and Fig. 13b shows the absolute difference between the two models versus maximum device temperature. As illustrated in Fig. 13b, the maximum absolute difference between the two models increases with a larger floorplan, indicating that the PE-NBS model is more inaccurate with a larger floorplan size. A larger floorplan size is usually required for a more complicated MCPM layout (e.g., more devices per switching position). Therefore, the PE-NBS model is not recommended for circuit simulation of more complicated

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2022.3175150, IEEE Journal of Emerging and Selected Topics in Power Electronics

Table III: Extraction Time and Memory Comparison for Different Layout Cases

	This model			Ansys Q3D			Comparison		
ID	Ls (nH)	Runtime (s)	Memory (MB)	Ls (nH)	Runtime (s)	Memory (MB)	Error	Speedup	Memory
1	15.6	1.85	9.4	14.8	64	157	5.5%	× 34.6	1:16.7
2	18.4	1.5	4.7	17.4	40	74.5	5.7%	× 26.7	1:15.8
3	21.4	0.6	6.2	20.6	15	73.7	3.9%	× 25	1:11.8

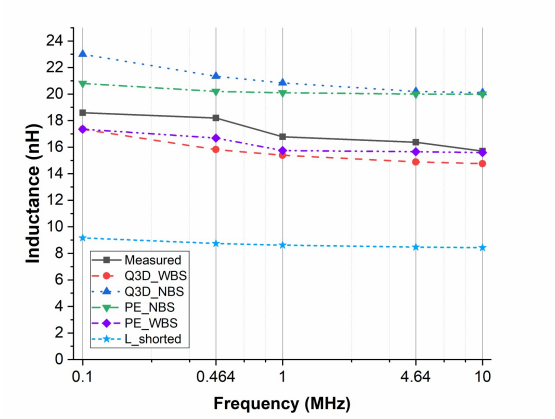


Fig. 12. a) Comparison among different methods and measurement b) Error comparison among measurement and models with backside consideration.

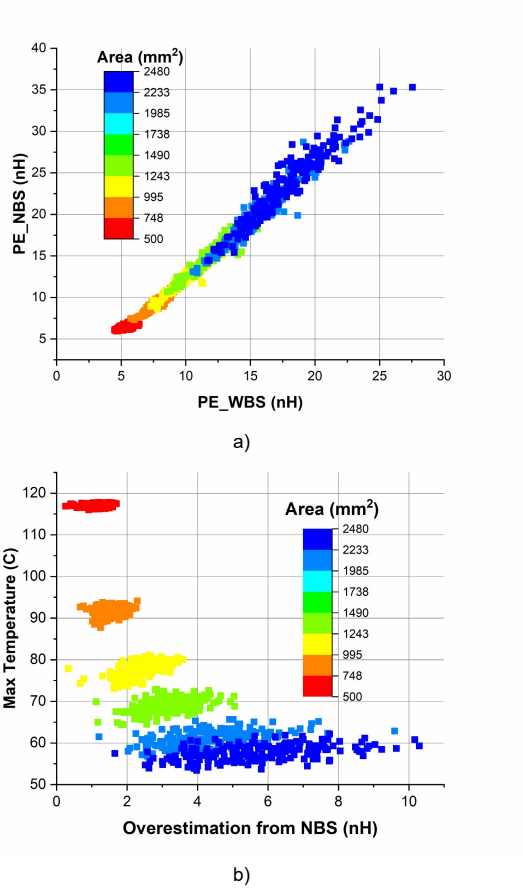


Fig. 13. a) Direct comparison between 2 approaches b) Absolute difference between 2 approaches versus maximum temperature.

MCPM layout. Additionally, due to this inaccuracy, there is a shift in the optimized pareto-front using PE-NBS and PE-WBS models (Fig. 14). Table. IV shows the error comparison of some optimized solutions (Fig. 15) selected from the PE-WBS pareto-front. The error margin expands with increased floorplan sizes. Despite the large error due to ignorance of eddy current, the PE-NBS model still shows the same trend within the same floorplan size (Fig. 13a). Therefore, one can still apply the PE-NBS to minimize the loop inductance for a fixed floorplan size problem. However, the extracted parasitic result is inaccurate for the further circuit simulation study. In this case, the characterization steps described in section III above can be applied to improve the accuracy of the extracted parasitic parameters. In addition, as shown in Table. II above, this process only takes about 15 minutes to complete for a selected DBC substrate. Therefore, this characterization process can be applied to any partial element models (e.g, [14], [16], and [19]) to improve the extraction accuracy.

A. *Impact of Eddy Current on Layout Optimization*

B. *Circuit Simulation Study*

The loop-based approach in this work also allows a distributed netlist generation, enabling a post-layout circuit simulation study and verification of a selected solution. While this process can be done using PEEC or FEA methods, it requires more effort to set up and run simulations, as discussed in [10]. A double pulse test (DPT) circuit simulation is performed in LtSpice to demonstrate the importance of the distributed netlist. Here, for the half-bridge layout on Fig. 10a, four CPM2-1200-0040B from Wolfspeed are switched with DC-DC voltage of 400V, the two pulses are shown in Fig. 16a where the rise and false time of the gate-signal is 50ns. The total load current is 40A through the load inductor of 50 uH. The LtSpice

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2022.3175150, IEEE Journal of Emerging and Selected Topics in Power Electronics

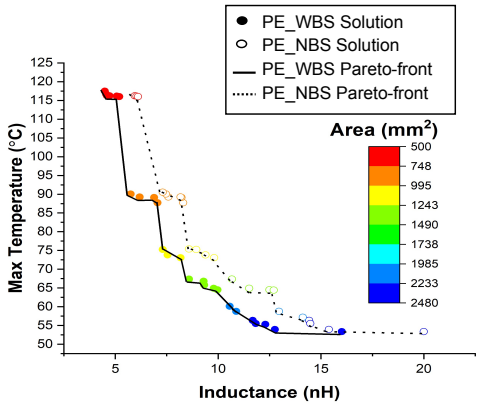


Fig. 14. Electrothermal Pareto-frontiers comparison between with and without backside consideration

device models [44] have been used to ensure most accurate simulation results. Two simulations are run to compare the distributed netlist extracted from the model using the process in Section III. D and a single lumped element for the loop inductance of 15.5 nH at 10 MHz. As shown in Fig. 16b, with the same loop-inductance, the ringing oscillation in both cases show the same resonance frequency of about 70 MHz. There is a 31 V difference in the peak overshoot voltage using the lumped versus the distributed model, which is about 75% difference if a single lumped element is used. This is because in the single lumped element simulation does not capture the switching behavior of each device correctly. On the other hand, the distributed netlist allows a more accurate analysis on the interaction between the layout parasitic parameters and device parameters (e.g., Ciss, Coss, Crss ...). More importantly, a more detailed analysis of the current sharing among devices can be done using the distributed netlist (Fig. 16c). In the future, this would help the optimization tool decide on a more optimized layout in terms of current balancing.

VI. Conclusion and Future Work

In this work, a parasitic extraction method is presented combining a regression-based characterization process with a loop-based approach to capture the eddy current impact in MCPM layout. This method is more efficient than FEA simulation while showing less than 10% error compared to simulation and measurement for a broad frequency range. This method has shown a maximum speedup of 35× while being 17× more memory efficient. While this method cannot beat the FEA approach in terms of flexibility, the method is more suitable in the design automation framework for MCPM layouts. Therefore, the method has been used in optimization tools such as PowerSynth for fast and accurate parasitic extraction. In the future, the accurate extracted parasitic results through a distributed netlist can be used to accurately predict power module dynamic performance aspects such as voltage overshoot, current sharing, or gate signal instability.

References

[1] H. A. Mantooth, T. Evans, C. Farnell *et al.*, "Emerging Trends in Silicon Carbide Power Electronics Design," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 3, pp. 161–169, 2017.

[2] M. Kanechika, T. Uesugi, and T. Kachi, "Advanced SiC and GaN Power Electronics for Automotive Systems," in *International Electron Devices Meeting*, 2010, pp. 13.5.1–13.5.4.

[3] A. B. Jorgensen, S. Munk-Nielsen, and C. Uhrenfeldt, "Overview of Digital Design and Finite-Element Analysis in Modern Power Electronic Packaging," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10 892–10 905, 2020.

[4] Z. Zeng, X. Zhang, and X. Li, "Layout-Dominated Dynamic Current Imbalance in Multichip Power Module: Mechanism Modeling and Comparative Evaluation," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 11 199–11 214, 2019.

[5] H. Lee, V. Smet, and R. Tummala, "A Review of SiC Power Module Packaging Technologies: Challenges, Advances, and Emerging Issues," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 239–255, 2020.

[6] F. Yang, Z. Liang, Z. J. Wang, and F. Wang, "Design of a Low Parasitic Inductance SiC Power Module with Double-sided Cooling," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 3057–3062.

[7] F. Yang, Z. Wang, Z. Liang, and F. Wang, "Electrical Performance Advancement in SiC Power Module Package Design With Kelvin Drain Connection and Low Parasitic Inductance," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 84–98, Mar. 2019.

[8] D.-P. Sadik, K. Kostov, J. Colmenares *et al.*, "Analysis of Parasitic Elements of SiC Power Modules With Special Emphasis on Reliability Issues," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 988–995, 2016.

[9] Y. Xiao, H. Shah, T. Chow, and R. Gutmann, "Analytical Modeling and Experimental Evaluation of Interconnect Parasitic Inductance on MOSFET Switching Characteristics," in *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC '04.*, vol. 1, 2004, pp. 516–521 Vol.1.

[10] M. Yun, K. Zhang, M. Cai *et al.*, "Extraction, Optimization and Failure Detection Application of Parasitic Inductance for High-Frequency SiC Power Devices," in *International Conference on Electronic Packaging Technology (ICEPT)*, 2021, pp. 1–5.

[11] B. Cougo, H. Schneider, and T. Meynard, "High Current Ripple for Power Density and Efficiency Improvement in Wide Bandgap Transistor-Based Buck Converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 8, pp. 4489–4504, 2015.

[12] M. R. Ahmed, R. Todd, and A. J. Forsyth, "Predicting SiC MOSFET Behavior Under Hard-Switching, Soft-Switching, and False Turn-On Conditions," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9001–9011, 2017.

[13] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Instability in Half-Bridge Circuits Switched With Wide Band-Gap Transistors," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2380–2392, 2014.

[14] L. Wang, Z. Zeng, Y. Yu *et al.*, "Current-Bunch: A Fast and Accurate Tool to Extract and Optimize Parasitics of Power Packaging," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 3171–3177.

[15] K. Wang, L. Wang, X. Yang *et al.*, "A Multiloop Method for Minimization of Parasitic Inductance in GaN-Based High-Frequency DC–DC Converter," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4728–4740, 2017.

[16] L. Horowitz, N. Pallo, S. Coday, and R. C. Pilawa-Podgurski, "A Method of Partial Inductances to Evaluate and Optimize Switching Cells," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 1549–1554.

[17] Y. Zhou, Y. Chen, H. Gao *et al.*, "A Layout Optimization Method to Reduce Commutation Inductance of Multi-Chip Power Module Based on Genetic Algorithm," in *IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, 2021, pp. 247–252.

[18] P. Ning, F. Wang, and K. D. T. Ngo, "Automatic Layout Design for Power Module," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 481–487, Jan. 2013.

[19] Q. Le, I. Al Razi, Y. Peng, and H. A. Mantooth, "Fast and Accurate Inductance Extraction for Power Module Layout Optimization Using Loop-Based Method," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 1358–1365.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2022.3175150, IEEE Journal of Emerging and Selected Topics in Power Electronics

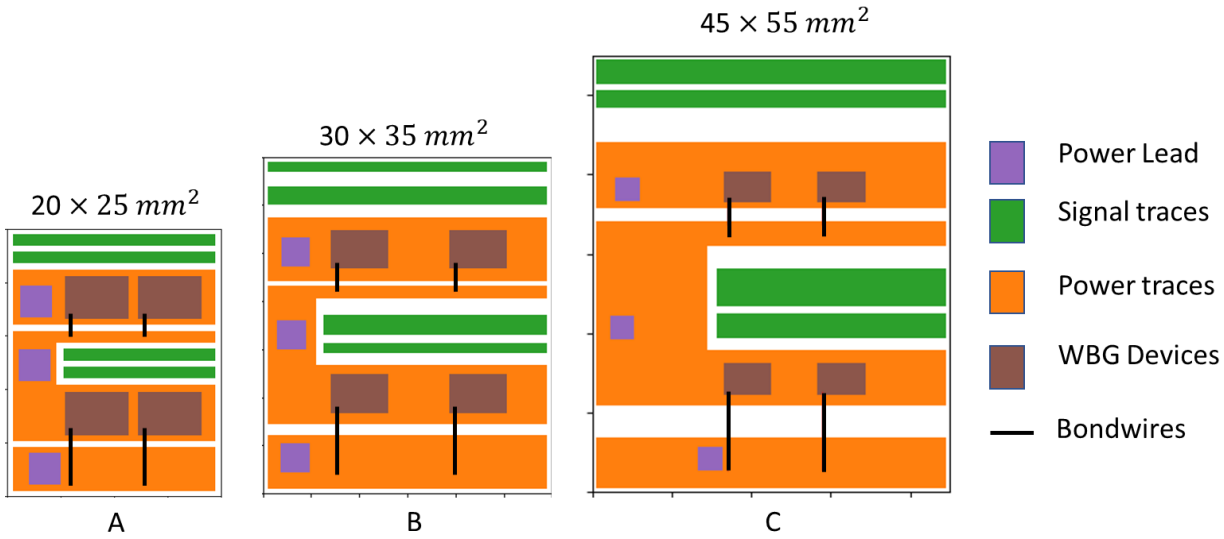


Fig. 15. Selected optimized layouts with various floorplan sizes

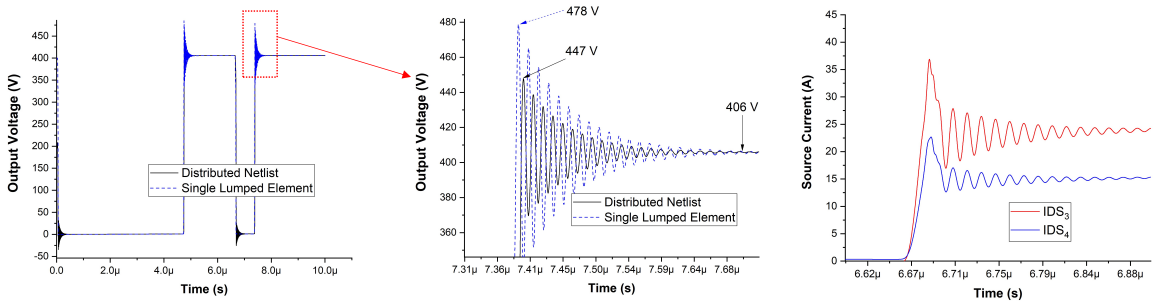


Fig. 16. a) DPT VDS waveform b) Zoomed in of VDS c) Source current comparison on lower side devices

[20] B. Gutsmann, P. Mourick, and D. Silber, "Exact Inductive Parasitic Extraction for Analysis of IGBT Pparallel Switching Including DCB-backside Eddy Currents," in *IEEE Annual Power Electronics Specialists Conference. Conference Proceedings (Cat. No.00CH37018)*, vol. 3, 2000, pp. 1291–1295 vol.3.

[21] A. Djordjevic and T. Sarkar, "Closed-form Formulas for Frequency-dependent Resistance and Inductance per Unit Length of Microstrip and Strip Transmission Lines," *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, no. 2, pp. 241–248, 1994.

[22] H. Wheeler, "Transmission-Line Properties of a Strip on a Dielectric Sheet on a Plane," *IEEE Transactions on Microwave Theory and Techniques*, vol. 25, no. 8, pp. 631–647, 1977.

[23] C. Holloway and E. Kuester, "Net and Partial Inductance of a Microstrip Ground Plane," *IEEE Transactions on Electromagnetic Compatibility*, vol. 40, no. 1, pp. 33–46, 1998.

[24] A. Niknejad and R. Meyer, "Analysis of Eddy-current Losses over Conductive Substrates with Applications to Monolithic Inductors and Transformers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 1, pp. 166–176, 2001.

[25] A. Dutta and S. S. Ang, "Electromagnetic Interference Simulations for Wide-Bandgap Power Electronic Modules," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 757–766, 2016.

[26] I. Kovacevic-Badstuebner, D. Romano, G. Antonini *et al.*, "Broadband Circuit-Oriented Electromagnetic Modeling for Power Electronics: 3-D PEEC Solver vs. RLCG-Solver," *Energies*, vol. 14, no. 10, 2021. [Online]. Available: https://www.mdpi.com/1996-1073/14/10/2835

[27] M. Kamon, M. Tsuk, and J. White, "FASTHENRY: a Multipole-accelerated 3-D Inductance Extraction Program," *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, no. 9, pp. 1750–1758, 1994.

[28] T. M. Evans, Q. Le, S. Mukherjee *et al.*, "PowerSynth: A Power Module Layout Generation Tool," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5063–5078, Jun. 2019.

[29] Q. Le *et al.*, "Response Surface Modeling for Parasitic Extraction for Multi-Objective Optimization of Multi-Chip Power Modules (MCPMs)," in *IEEE Workshop on Wide Bandgap Power Devices and Applications*, Oct. 2017, pp. 327–334.

[30] Q. Le, T. Evans, Y. Peng, and H. A. Mantooth, "PEEC Method and Hierarchical Approach Towards 3D Multichip Power Module (MCPM) Layout Optimization," in *IEEE International Workshop on Integrated Power Packaging*, Apr. 2019, pp. 131–136.

[31] I. Al Razi, Q. Le, T. M. Evans *et al.*, "PowerSynth Design Automation Flow for Hierarchical and Heterogeneous 2.5-D Multichip Power Modules," *IEEE Transactions on Power Electronics*, vol. 36, no. 8, pp. 8919–8933, 2021.

[32] R. Escovar, S. Ortiz, and R. Suaya, "An Improved Long Distance Treatment for Mutual Inductance," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 5, pp. 783–793, 2005.

[33] X. Huang, P. Restle, T. Bucelot *et al.*, "Loop-based Interconnect Modeling and Optimization Approach for Multigigahertz Clock Network Design," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 457–463, 2003.

[34] Y. Peng, D. Petranovic, and S. K. Lim, "Chip/package Co-analysis and Inductance Extraction for Fan-out Wafer-level-packaging," in *IEEE Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)*, 2017, pp. 1–3.

[35] C. Hoer and C. Love, "Exact Inductance Equations for Rectangular Conductors with Applications to More Complicated Geometries," *JOURNAL OF RESEARCH of the National Bureau of Standards-C. Engineering and Instrumentation*, vol. 69C, p. 127, Jan. 1965.

[36] F. Pedregosa, G. Varoquaux, A. Gramfort *et al.*, "Scikit-learn: Machine learning in Python," *Journal of Machine Learning Research*, vol. 12, pp. 2825–2830, 2011.

[37] B. Krauter and S. Mehrotra, "Layout Based Frequency Dependent Inductance and Resistance Extraction for on-chip Interconnect Timing

Analysis," in *Design and Automation Conference. 35th DAC*, 1998, pp. 303–308.
[38] T. H. Cormen, C. E. Leiserson, R. L. Rivest, and C. Stein, *Introduction to Algorithms*, 2nd ed. The MIT Press, 2001.
[39] Z. Wang, Z. Yuan, Z. Ma *et al.*, "Fixtures Design Considerations for Impedance Measurement," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 1555–1559.
[40] B. Nelson, A. Lemmon, B. DeBoi *et al.*, "Measurement-Based Modeling of Power Module Parasitics with Increased Accuracy," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 1430–1437.
[41] "PowerSynth Releases." [Online]. Available: https://e3da.csce.uark.edu/release/PowerSynth/
[42] "ARL ParaPower." [Online]. Available: https://github.com/USArmyResearchLab/ParaPower
[43] T. M. Evans, S. Mukherjee, Y. Peng, and H. A. Mantooth, "Electronic Design Automation (EDA) Tools and Considerations for Electro-Thermo-Mechanical Co-Design of High Voltage Power Modules," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 5046–5052.
[44] M. M. Hossain, L. Ceccarelli, A. U. Rashid *et al.*, "An Improved Physics-based LTSpice Compact Electro-Thermal Model for a SiC Power MOSFET with Experimental Validation," in *IECON Annual Conference of the IEEE Industrial Electronics Society*, 2018, pp. 1011–1016.

Quang Le Research Assistant at the University of Arkansas. Mr. Le (IEEE S'16) received the B.S. (summa cum laude) degree in electrical engineering in December 2015 from the University of Arkansas, Fayetteville, where he is currently working towards a Ph.D. degree in electrical engineering. He is currently working at Dr. Alan Mantooth's Mixed-Signal Computer-Aided Design (MSCAD) lab.

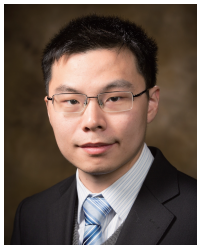
His current research focuses on design automation and optimization tools for power electronics modules. He also completed an internship at Cadence Design Systems - Analog Mixed Signal (AMS) group in 2019. In 2019, He served as a student leader in the National Science Foundation's multi-university, multi-disciplinary Engineering Research Center for Power Optimization of Electro-Thermal Systems (POETS). In 2021, He receives 1st place in ECCE 2021 Software Demonstration Competition.

Imam Al Razi received his B.Sc. in electrical and electronic engineering (EEE) from Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh in 2016. Currently, he is a Ph.D. student in Computer Science and Computer Engineering department at the University of Arkansas.

His research interest is in Computer Aided Design (CAD) tool development for power electronics and VLSI. He is working as a National Science Foundation's Engineering Research Center for Power Optimization of Electro-Thermal Systems (POETS) student on automated layout synthesis and optimization tool for multi-chip power modules (MCPMs).

Tristan M. Evans Research Assistant at the University of Arkansas. Mr. Evans received his B.S. and M.S. degrees in electrical engineering from the University of Arkansas, Fayetteville in 2009 and 2011, respectively. Afterwards, he joined the R&D department of ROHM Semiconductor at their headquarters in Kyoto, Japan as an assistant researcher focusing on new die attach technology for silicon carbide (SiC) power devices, prototyping and management of low-volume power module production, and electro-thermal modeling of SiC power modules. In 2016 he was awarded the Distinguished Doctoral Fellowship at the University of Arkansas and returned there to pursue a Ph.D. in electrical engineering focusing on design automation tools for power electronics.

Shilpi Mukherjee (S'07-M'20) received her Bachelor of Engineering degree in electrical and electronics engineering from the National Institute of Engineering in India (2010). She worked in the field of information technology for two years at Pune, India. After completing her M.S. degree in Microelectronics and Photonics from the University of Arkansas, Fayetteville (2014), she was awarded the Doctoral Academy Fellowship to continue her studies at the University of Arkansas. She is currently a Ph.D. candidate working with Prof. Alan Mantooth on the prevention of partial discharges in power modules. Shilpi has worked on inter-university and inter-disciplinary collaborative projects within National Science Foundation's POETS (Power Optimization of Electro-Thermal Systems) grant and has served as a student leader for the organization. Her work has been funded by POETS and the U.S. Army Research Lab. She completed an internship with ANSYS, Inc. in 2017.



Yarui Peng (S'12-M'17) received the B.S. degree from Tsinghua University, Beijing, China in 2012. He earned his M.S. and Ph.D. degrees in Electrical and Computer Engineering from Georgia Institute of Technology, Atlanta, USA in 2014 and 2016, respectively. He is currently an Assistant Professor in Computer Science and Computer Engineering Department at University of Arkansas.

His research interests are computer-aided design, analysis, and optimization for emerging technologies and multi-chip packages, such as 2.5D/3D ICs and wide band-gap power electronics. He studies design methodologies and optimization algorithms for parasitic extraction, signal integrity, power integrity, and thermal reliability. He also develops design automation tools for power electronics to improve performance, reliability, and productivity. He receives best paper awards in SRC TECHCON 14, ICPT 16, and EDAPS 17. In 2021, he also received NSF CAREER Award to Study Design Automation Tools for Heterogeneous Multi-Chiplet Systems.

H. Alan Mantooth (IEEE S'83 - M'90 - SM'97 – F'09) received the B.S.E.E. and M.S.E.E. degrees from the University of Arkansas in 1985 and 1986, and the Ph.D. degree from Georgia Tech in 1990. He then joined Analogy, a startup company in Oregon. In 1998, he joined the faculty of the Department of Electrical Engineering at the University of Arkansas, Fayetteville, where he currently holds the rank of Distinguished Professor. His research interests now include analog and mixed-signal IC design & CAD, semiconductor device modeling, power electronics, power electronic packaging, and cybersecurity. Dr. Mantooth helped establish the National Center for Reliable Electric Power Transmission (NCREPT) at the UA in 2005. Professor Mantooth serves as the Executive Director both the NSF Industry/University Cooperative Research Center on GRid-connected Advanced Power Electronic Systems (GRAPES) and the Cybersecurity Center on Secure, Evolvable Energy Delivery Systems (SEEDS) funded by the U.S. Department of Energy. Dr. Mantooth holds the 21st Century Research Leadership Chair in Engineering. He currently serves as Senior Past-President for the IEEE Power Electronics Society and Editor-in-Chief of the IEEE Open Journal of Power Electronics. Dr. Mantooth is a Fellow of IEEE, a member of Tau Beta Pi, Sigma Xi, and Eta Kappa Nu, and registered professional engineer in Arkansas.