PowerSynth 2: Physical Design Automation for High-Density 3-D Multichip Power Modules

Imam Al Razi, *Student Member, IEEE*, Quang Le, *Student Member, IEEE*, Tristan M. Evans, *Student Member, IEEE*, H. Alan Mantooth, *Fellow, IEEE*, and Yarui Peng, *Member, IEEE*

***Abstract*—Moving toward an electrified world requires ultrahigh-density power converters. With the adoption of wide-bandgap semiconductors (e.g., SiC and GaN), the next-generation power converters are on the horizon. However, the complexity of compact and high-speed converters is beyond the current industry-standard design flow based on manual and iterative steps. Therefore, research on design automation and optimization has been identified as an emerging topic in the power electronics society. Among different components of the converter, the physical design of power modules has proven critical for achieving high power density and energy efficiency. We present the latest design automation flow for high-density (2-D/2.5-D/3-D) and heterogeneous multichip power modules (MCPM) through PowerSynth 2 framework. In this article, we further demonstrate electro-thermal optimization for state-of-the-art (SOTA) 3-D packaging technologies. Using the latest PowerSynth 2 framework, electro-thermal design optimization is carried out on a sample 3-D MCPM layout using both exhaustive and evolutionary search methods. The optimized design is hardware-validated against physical measurements. The measurement result has shown an order of magnitude productivity improvement within 10% accuracy compared to the SOTA industry design flow.**

***Index Terms*—3-D power module, layout optimization, physical design automation, PowerSynth 2.**

I. Introduction

POWER conversion is an essential part of the modern world, where power electronic systems are found everywhere, from electricity generation to the application (e.g., electric vehicles, data centers, home appliances, and aerospace). The demand for a more-electric world has initiated a call for high-density and reliable power converters. Wide-bandgap (WBG) material-based switching devices like gallium nitride (GaN) and silicon carbide (SiC) are considered rising stars for higher switching efficiency [1]. Achieving high-power density is possible by integrating heterogeneous components [e.g., gate drivers, sensors, and electromagnetic interference (EMI) filters] and compacting module size through vertical stacking, creating challenges for thermal management as well as reliable lifetime [2]. To unleash the full potential of these latest packaging technologies, design automation is getting attention in both component and system-level design approaches.

To increase efficiency and overcome the challenges associated with advanced packaging technologies, researchers are focusing on developing methodologies to automate the design optimization of different components and converter systems. For example, design optimization tools are developed for the heat sink [3], EMI filter, and *LLC* resonant converter [4] focusing on various applications.

Power modules are fundamental elements of a power converter. Electric vehicles and electrified aerospace are emerging fields, where custom power modules are very critical to achieve high power-density with reduced volume and weight. The traditional approach is not capable of satisfying these custom module design requirements in an efficient way as this is a manual-and-repetitive design process, which requires multiple finite-element analysis (FEA) simulations to generate a single solution that is not guaranteed to be optimum [5]. Therefore, this tedious process cannot optimize the latest packaging technologies invented for ultrahigh-density module designs [6]. Among various innovative packaging approaches, the generic concepts include 2-D/3-D flip-chip [7], 2.5-D packaging [8], 3-D wire-bonded, hybrid, wire-bondless packaging [9], [10]. Existing commercial computer-aided design (CAD) tools from the power electronics industry parameterize the design variables to perform decoupled electro-thermo-mechanical analyses. However, they are limited by manually selected parameters. As a result, they cannot perform an intelligent search for the optimum solution, and each iteration requires multiple FEA runs, which results in a long runtime. The automated approach can export a distributed parasitic netlist using the built-in electrical model, whereas the FEA tool can generate a single lumped parasitic value (*R*/*L*/*C*), which cannot be used for detailed simulation. A significant speedup can be achieved in the automated design flow due to the electro-thermo-mechanical and reliability co-optimization. Also, considering the technology constraints in the manufacturer design kit (MDK) guarantees DRC-clean solutions in the automated approach, whereas the design rule checking (DRC) needs to be performed manually in the traditional approach.

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Imam Al Razi and Yarui Peng are with the Department of Computer Science and Computer Engineering, University of Arkansas, Fayetteville, AR 72701 USA (e-mail: ialrazi@uark.edu; yrpeng@uark.edu).

Quang Le, Tristan M. Evans, and H. Alan Mantooth are with the Department of Electrical Engineering, University of Arkansas, Fayetteville, AR 72701 USA (e-mail: qmle@uark.edu; tmevans@uark.edu; mantooth@uark.edu).

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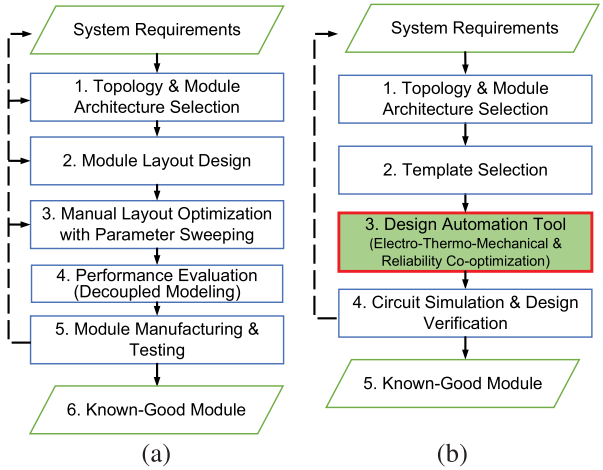

Fig. 1. Power module design flow. (a) Traditional versus (b) automated.

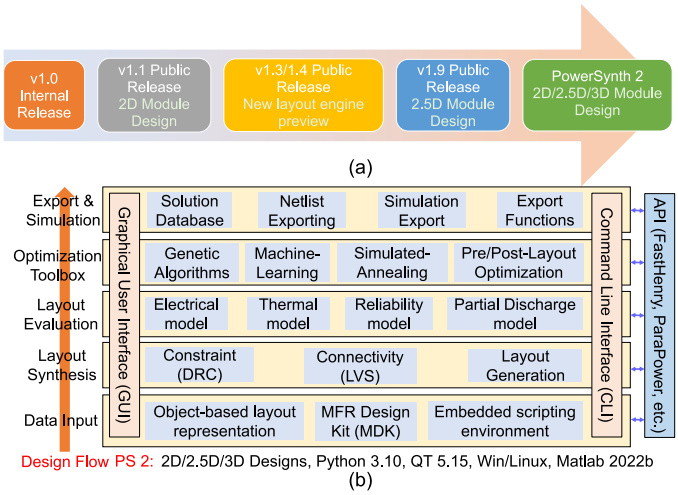

Fig. 2. (a) PowerSynth timeline summary. (b) PowerSynth 2 architecture.

The traditional, manual design flow versus the electronic design automation (EDA) flow comparison is summarized in Fig. 1.

Some researchers have come up with design automation methodologies for 2-D layout optimization. For example, authors from [11] developed an MCPM layout optimization method that uses a graph model to describe heterogeneous layouts with all interconnectivity and design constraints. Integer programming is introduced to generate layout templates with variable geometric topologies from the initial graph model. This methodology does not require a complete initial input layout from the user as it generates the initial layout based on the user's choice from the template library. However, the methodology is very application-specific with a limited number of components handling capability. The integer programming method is nondeterministic polynomial complete, which is not scalable, as with the number of increasing components, the runtime exponentially increases and it may face convergence issues in some cases. On the other hand, PowerSynth 2 uses corner stitching data structure, which is linear to the number of components and the constraint graph (CG) uses the longest path algorithm that has a time complexity of $O(E)$, where E is the number of edges in the graph. Finally, the hierarchy consideration has imposed a $O(E\log V)$ complexity for the overall methodology, where V is the number of nodes in the tree, which is scalable with the design variables. Moreover, the proposed methodology is applied and verified through a 2-D design. Any 2.5-D/3-D module is not optimized and verified with the methodology. In [12], researchers have developed a genetic algorithm-based multiobjective optimization framework, where the device placement varies with a fixed routing of the traces. FEA tools are used for electro-thermal performance evaluation. Although the proposed methodology can optimize the device placement, the trace routing impact is not considered, resulting in a smaller solution space. Moreover, the time-consuming FEA is unsuitable for rapid design space exploration of the high-density and heterogeneous layouts. Another research [13] adapts the sequence pair methodology for power module layout representation, and a 1-D binary string is used for optimization using the genetic algorithm. However, this methodology cannot optimize the advanced packaging technologies due to the limitation of simplified layout representation using design strings.

The current leading framework for MCPM layout optimization is PowerSynth [14]. After about a decade of research and development effort, PowerSynth v1.1 [14] introduced the layout abstraction technique called symbolic layout. The symbolic layout representation technique works for some simple 2-D geometries. Hardware-validated, reduced-order electrical and thermal models are presented, which can predict electro-thermal performance values within 10% accuracy with orders of magnitude speedup compared to the FEA tools. However, a matrix-based methodology is used to generate layout solutions, which leads to iterative DRC, limited solution space, and long run time on complicated layouts. To address these, the hierarchical corner stitching data structure with a CG evaluation technique is used to optimize and validate the 2.5-D CAD flow in PowerSynth v1.9 [15]. PowerSynth v1.9 has built up the fundamentals for hierarchical optimizations and can efficiently synthesize 2-D/2.5-D modules. This work introduces PowerSynth 2, which has added capability of optimizing 3-D MCPM layouts and is released in [16] for the public. Also, PowerSynth v1.1 and v2.0 source code will be gradually published on github webpage [17]. The PowerSynth roadmap is shown in Fig. 2(a).

II. Overview of PowerSynth 2

A. New Features and Contributions

This article demonstrates PowerSynth v2.0 CAD flow for high-density (2-D/2.5-D/3-D) and heterogeneous power module layout optimization. Our new contributions over earlier published works on PowerSynth are as follows.

1) New Software Architecture: PowerSynth 2 architecture [shown in Fig. 2(b)] is a modular and hierarchical one. This architecture is more flexible compared to previous versions

that can interact with external tools through application programming interfaces (APIs). The design flow is generic and extendable toward cabinet-level optimization. More detail about the architecture is described in Section III.

2) Layout Engine Updates: PowerSynth v1.1 has a very limited, simple 2-D geometry handling capability, whereas v1.9 can handle all 2-D/2.5-D Manhattan geometries. However, PowerSynth 2 layout engine can handle all 2-D/2.5-D/3-D Manhattan layouts. The baseline algorithms from v1.9 have been updated to handle interlayer connections (i.e., via). The methodology updates are described in detail in Section IV. These updates have enabled PowerSynth 2 to optimize most of the SOTA packaging technologies. Details are provided in Section V.

3) Improved User Experience: In PowerSynth 2, both graphical user interface (GUI) and command-line interface (CLI) are available for the user's flexibility. Also, PowerSynth v2.0 is released on the website [16] along with the user manual and test designs.

4) Updated Modeling Efforts: The partial element equivalent circuit (PEEC)-based electrical model from v1.9 is limited to handling 2-D MCPM layouts. To support 3-D layout's electrical parasitic extraction capability, an in-house, loop-based electrical model is under development, while the FastHenry [18] electrical model has been interfaced for v2.0. Also, the 1-D thermal model used in previous versions has been replaced with a more generic ParaPower [19] thermal model to incorporate 3-D layout thermal evaluation capability. This integration has enabled both static, transient thermal simulation, and stress evaluation for 2-D/2.5-D/3-D MCPM designs. Besides, electro-thermal performance models, reliability modeling efforts are also initiated. For example, an electromigration-aware reliability model is proposed in [20]. Section IV-C has a detailed description about the modeling efforts in PowerSynth 2.

5) Hardware-Validation of 3-D MCPM Design: Finally, the 3-D MCPM design optimization capability has been hardware-validated through a novel 3-D MCPM module design. The brand-new 3-D module has been optimized for electrical and thermal performances, and an optimized design has been manufactured in-house. Electrical and thermal testing has been performed on the manufactured module to verify the optimization result. The custom 3-D MCPM layout optimization result is described in Section V. Fabrication details and the experimental verification results are presented in Section VI.

6) Design Flow Demonstration: PowerSynth 2 CAD flow [shown in Fig. 2(b)] is validated for a wire-bonded 3-D MCPM layout case. The flow starts with an initial layout, a layer stack, and design constraints, which is referred to as "Data Input" step in the architecture. Then, the solution layouts are generated using the constraint-aware, hierarchical layout generation methodology. These layouts are evaluated using the performance evaluation models, and an optimizer can be used to reach toward the Pareto-optimal solution set. Finally, from the solution space, the balanced solution is chosen and exported for postlayout optimization, which is referred to as "Export and Simulation" in the design flow. Upon exporting the balanced solution, postlayout optimization can be performed manually. Then, the layout is fabricated and tested for performance validation. The experimental results prove the PowerSynth 2 CAD flow efficiency. Each step is described in the rest of this article.

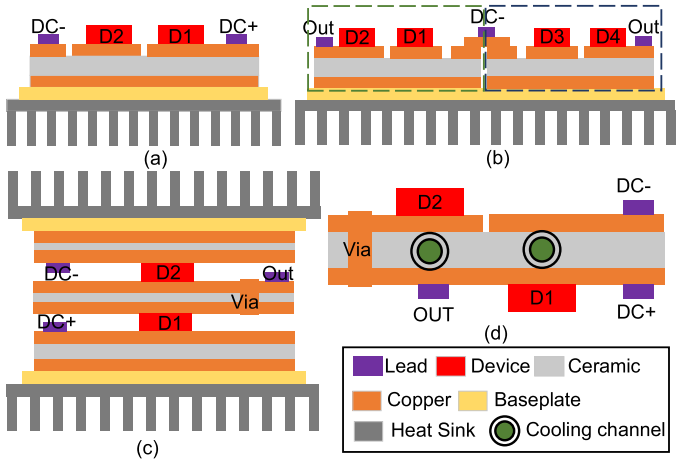

Fig. 3. MCPM layout structures. (a) 2-D half-bridge, (b) 2.5-D full-bridge, and 3-D half-bridge with (c) double-sided cooling or (d) embedded cooling.

B. MCPM Design Variations

To categorize the existing MCPM designs, the number of routing and device layers present in a design is considered. Based on these criteria, the MCPM designs are classified into three types: 2-D, 2.5-D, and 3-D. These different types of layouts are defined under PowerSynth 2 scope for better clarification. Fig. 3 shows cross sections of three types of layouts. Here, a 2-D layout refers to a single device layer, whereas 2.5-D layouts refer to multiple device-supporting substrates horizontally connected with additional routing resources. A 3-D half-bridge module consists of multiple device layers stacked vertically. Double-sided cooling is one solution for face-to-face stacking of the devices and flip-chip designs. However, for face-to-back stacking [shown in Fig. 3(c)], it requires at least four layers to form a half-bridge module with double-sided cooling, which increases the fabrication cost and complexity. To reduce the fabrication complexity and cost, back-to-back stacking can be performed to create a half-bridge module with an embedded heat sink/microcooler [21] between two copper layers [shown in Fig. 3(d)].

III. Architecture and Design Automation Flow

PowerSynth 2 architecture is shown in Fig. 2(b). Compared to PowerSynth 1, the new architecture is a module-based one. It has multiple design layers, and each layer has a flexible API to communicate within or outside the tool. The tool has two fundamental parts: a core that contains the built-in algorithms, methodologies, and modeling techniques; external tools that include commercial tools or models developed by other research groups, which are linked through APIs developed by the authors.

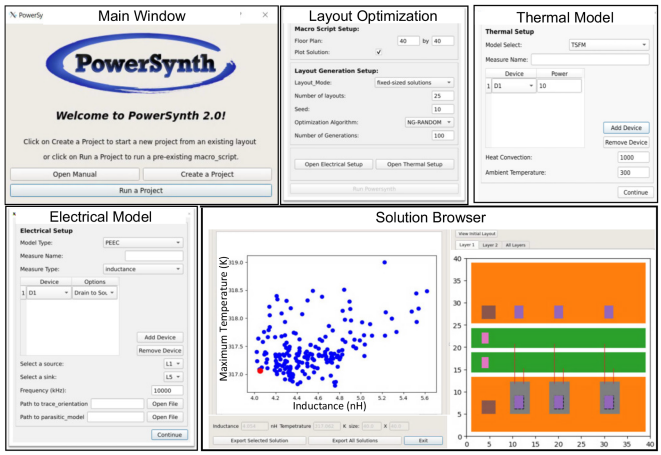

Fig. 4. PowerSynth 2 graphical user interface (GUI).

This architecture is scalable and can be extended toward cabinet-level optimization.

A. User Interfaces and Design Input

PowerSynth v2.0 has both a graphical user interface (GUI) for the interactive mode and a command-line interface (CLI) for the unattended mode and is compatible with both Windows and Linux. The CLI works on user input through the terminal, which uses a macro script describing the necessary parameters to perform the optimization flow. It is designed for high-performance and cloud computing. Besides, there is an interactive GUI for regular users. Some of the windows of the GUI are shown in Fig. 4. The main window of the user interface provides the following two main flows:

1) creating a new project from an existing layout;
2) running a project using the macro script already prepared.

Users can modify the material library, layer stack, and design constraints through the GUI. Then, the layout generation/optimization setup window can run PowerSynth 2 in three different modes: performing performance evaluation of the initial layout, generating layout solutions only, and optimizing layout solutions based on the performance models. For optimization/evaluation mode, the user needs to set up necessary files and parameters through different model setup windows. Once the necessary parameters are defined, the layout optimization process begins, and results are shown in the solution browser. Finally, the user can choose an individual solution from the solution space and export both individual and complete solution space for further processing.

PowerSynth 2 requires an initial description of the technology that contains the layer stack, power devices, substrates, connectors, heat spreaders, wire bonds, and via information. As an umbrella module, the built-in manufacturer design kit (MDK) contains a library of materials and other technology information similar to the process design kit in very large-scale integration (VLSI). An interface is built to interact with MDK so that users can update the libraries. Besides, the initial placement of the devices, leads, and routing of the traces information is taken through a hierarchical geometry description script, which is represented through an object-based data structure. An embedded scripting environment can be used to accelerate the layout geometry processing.

B. Layout Generation and Evaluation

The initial input layout is stored using two hierarchical corner-stitched tree structures: One for horizontal and another for vertical corner-stitched planes. From this data structure, two sets of CGs are created for layout solution generation using the values of the minimum constraints as edge weights provided by the manufacturer or user. Several efficient algorithms are used to generate different types of layout solutions by randomizing the edge weights of the CGs. Constraint graph creation and evaluation ensure the DRC-clean solution generation. The basic algorithms of corner stitching data structure and CG are described in our previous work [15].

As WBG devices can switch faster at higher voltage and current, electrical parasitics in the MCPM layout must be minimized to achieve the target circuit performance. With the increased density in a 3-D MCPM layout design, the parasitic loop inductance is significantly reduced compared to its 2-D counterparts. However, as the 3-D layout solution is more compact, ensuring thermal and mechanical reliability becomes challenging. Therefore, electro-thermo-mechanical performance and reliability optimization are required before fabricating a module. Available multiphysics or FEA-based analysis tools can be used for capturing these performances. However, these methods are not efficient to be used in the optimization loop due to long runtime. To address these issues, PowerSynth 2 is equipped with reduced-order electrical, thermal, and reliability models, which are fast and quite accurate compared to FEA tools. The electrical model performs resistance, capacitance, and inductance evaluation. Research is ongoing to extend electrical models to 3-D layouts. Thermal metrics include static and transient junction temperature evaluation. Reliability optimization refers to transient thermal cycling impact minimization and electromigration risk assessment. Maximum, average, and peak-to-peak temperatures of different components due to the transient thermal cycling input are considered, which is proportional to the thermal stress endured by the devices. Multilevel APIs have been developed inside the tool to leverage the existing electrical, thermal, and mechanical models from other research groups or companies. In this work, FastHenry [18] from FastFieldSolvers is used for loop parasitics extraction, and ParaPower [19] from Army Research Lab for thermal evaluation.

C. Design Optimization and Solution Export

For providing optimization options, PowerSynth 2 has a genetic algorithm and built-in randomization algorithm framework with other optimization algorithms such as simulated annealing and the neural network under investigation. Currently, PowerSynth 2 flow users can choose any available options for performing electrical, thermal, and reliability optimization. A comparison study between randomization and genetic algorithm

shows that genetic algorithm can converge faster to the Pareto-optimal solution set for a given number of generations. Although randomization provides little guidance toward optimization objectives, it can explore a larger solution space and potentially find better solutions with an acceptable runtime overhead [22]. Once the optimizer generates the solution space, a nondominated sorting is applied to get the Pareto-optimal solutions. After choosing an optimized solution for fabrication, postlayout optimization features like filleting the sharp corners to reduce current crowding and field focusing can be performed. From the solution browser, the user can choose a solution to export. APIs have been developed to export the solution in commercial 3-D CAD tools like ANSYS Q3D, SolidWorks, etc. Exporting a complete distributed parasitic netlist with *RLC* elements is one of the killer features. The exported netlist can back-annotate the circuit schematic to perform resimulation, completing the round-trip engineering design loop before fabrication. Finally, the optimized solution can be fabricated to validate and fine-tune models through physical measurements.

IV. 3-D Layout Generation Algorithms and Models

To help the designers to design custom, sophisticated, and critical MCPMs, EDA tools like PowerSynth can be helpful to find the global optimum solution by performing multiobjective optimization thus reducing the engineering time and cost. Aiming at such applications, PowerSynth 2 physical design automation methodology has been developed in a generic, scalable, and efficient way so that it can be extended toward cabinet-level optimization. For scalability and efficiency, a hierarchical methodology has been chosen. Hierarchy consideration helps apply a divide-and-conquer strategy, which is efficient for solving complex problems like physical design automation and optimization. Design constraint violation has been a bottleneck for design automation methodologies found in the literature. To address this problem, constraint-aware methodology has been developed in PowerSynth 2. Horizontal and vertical CGs are maintained to respect the minimum design constraints. To analyze the design constraints efficiently, the corner-stitching data structure has been chosen. To construct the hierarchical corner-stitch trees, a hierarchical layout geometry script format is introduced, with the initial layout taken as the input. Constraint graphs are created from the corner-stitched planes for the initial layout, and then, the graph edge weights are randomized to generate the solutions. Therefore, corner-stitching is a one-time effort for each MCPM design case. While randomizing the edge weights, to ensure no constraint violations, several algorithms are developed. All these algorithms have a linear time complexity so that the methodology is scalable with the number of components in the MCPM layout. Another important part of the flow is finding optimized designs based on the performances and power density. The optimization requires those performance evaluation models to be fast and accurate. PowerSynth 2 has either built-in models or APIs to interact with external models, which are fast and accurate enough to be used in the optimization loop so that the solution space generation can be performed within a few hours. Finally, the solutions need to be validated through hardware prototyping and measurements so that the models can be trusted and reused for different modules. This validation part is a manual task and out of PowerSynth 2 workflow scope. So, the layout optimization process using PowerSynth 2 starts with a user-provided initial layout geometry script and ends with generating a manufacturable optimized layout solution set. Major steps include layout representation, layout synthesis (solution generation), performance evaluation/optimization, and solution export. Each of these steps is briefly described below. Since PowerSynth 2 layout optimization is dependent on the initial input layout, the user can generate better optimization results if the initial layout is designed carefully. Therefore, these data structures and algorithm details can help power electronics designers to understand the underlying hierarchical optimization capability of the tool and help them designing the initial layout more effectively.

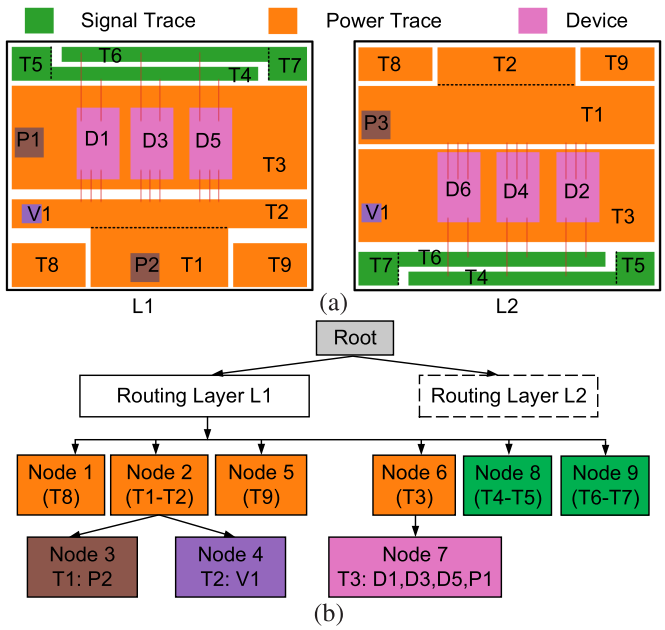

Fig. 5. Input layout structure of a 3-D MCPM. (a) 2-D view of each routing layer. (b) L1 layer hierarchical tree.

A. Layout Representation and Data Structures

PowerSynth 2 takes a layer stack, a set of constraints, and a hierarchical layout geometry script along with the via connectivity information as input. A sample 3-D layout (shown in Fig. 10) consisting of two routing layers (L1 and L2) connected through a via (V1) is considered for describing the layout representation in PowerSynth 2. The planar view of each routing layer of the 3-D layout is shown in Fig. 5(a). The hierarchical tree structure for the sample 3-D layout is shown in Fig. 5(b). Both routing layers have six groups of traces. Each group can have single or multiple connected traces. L1 has dc+ (P1) and OUT (P2) power leads along with three SiC devices (D1, D3, D5). L2 has dc- (P3) and three SiC devices (D2, D4, D6). Both layers' have via (V1) connected OUT trace. Since both routing layers have a very similar structure, only the L1 layer subtree is shown. From the

```
# Via Connectivity Information
L1 L2: V1 Through
# Layout Geometry
L1 Z-                                  L2 Z+
+ T8 power 7 7 7.5 4.5                 + T8 power 7 28 7.5 3.5
+ T9 power 29.5 7 7.5 4.5              + T9 power 29.5 28 7.5 3.5
+ T1 power 15 7 14 6                   + T1 power 7 21.5 30 6
- T2 power 7 13 30 3 BG1               - T2 power 15 27.5 14 4 BG7
   + P2 power_lead 19 7.5                 + P3 power_lead 7.25 22
   + V1 Via 8 13.5                     + T4 signal 12 7 21 1.5 BG8
+ T4 signal 11 28 21 1.5 BG2           - T5 signal 33 7 4 3.5
- T5 signal 7 28 4 3.5                 + T6 signal 12 30 21 1.5 BG9
+ T6 signal 12 30 21 1.5 BG3           - T7 signal 33 28 4 3.5
- T7 signal 33 28 4 3.5                + T3 power 7 11.5 30 9.5
+ T3 power 7 17 30 10.5                   + V1 Via 8 13.5
   + P1 power_lead 7.5 21                + D2 MOS 15 13.5 R180 BG10
   + D1 MOS 13.5 18 BG4                  + D4 MOS 21 13.5 R180 BG11
   + D3 MOS 19 18 BG5                    + D6 MOS 27 13.5 R180 BG12
   + D5 MOS 25 18 BG6

BG1: BW3, 6, 9          BG2: BW1, 4, 7          BG3: BW2, 5, 8
BG4: BW1, 2, 3          BG5: BW4, 5, 6          BG6: BW7, 8, 9
BG7: BW12, 15, 18       BG8: BW11, 14, 17       BG9: BW10, 13, 16
BG10: BW10, 11, 12      BG11: BW13, 14, 15      BG12:BW16, 17, 18
```

Fig. 6. Input geometry script of routing layers (L1 and L2).

tree structure, it is clear that six trace islands are mapped into six nodes in the L1 subtree. Since Node 2 and Node 6 traces contain additional components, they have child nodes (Nodes 3, 4, and 7). To provide such an initial layout as input in PowerSynth 2, the user needs to generate the text script shown in Fig. 6. Here, the bonding groups (BG) are used for simplifying the bonding wire description. The layout geometry script needs to be created based on the same hierarchical placement concept as shown in Fig. 5(b). This script has two parts: *Via Connectivity Information* and *Layout Geometry*. The *Via Connectivity* section is required for 3-D MCPM layouts, which is a new section on top of the v1.9 script as 3-D layout handling is not possible with previous versions. In the *Via Connectivity* section, each line has two fields separated by a colon. The fields are names of the via-connected layers separated by a space, names of the vias separated by a space, and the via type (Through or Connector). "Through" type vias connect two routing layers of the same substrate, whereas the "Connector" type vias connect two routing layers of different substrates. In this example, there are six different types of components: power and signal trace (T), wire bond (BW), power lead (P), via (V), and device (D). The layer names are mapped from the layer stack information. In the *Layout Geometry* section, for each layer, the first line represents the layer name and corresponding routing direction. In 3-D layouts, the routing of a layer can be either in "Z+" or "Z−." For this example, L1 has components on the bottom side with a routing direction as "Z−," whereas the L2 layer has components facing upward, which refers to the "Z+" direction. All 2-D layouts have a single layer, and hence, they have only "Z+" direction. The following lines represent each component in the layout. Each new group starts with a plus sign, and a dash represents the continuation of the same group. Traces have six fields, and other components have 4 or 5. Each component has four basic fields: ID, type, and bottom-left corner's x and y coordinates. The geometry is described using a global coordinate system. Since the trace dimensions can be varied, two extra fields are required for the initial layout description: width and length. Other components' except bonding wire width and length are constant and read from the corresponding component description files available in the MDK. Sometimes, the devices can have a rotation field to describe the orientation. Three different orientations (R90, R180, and R270) are considered that represent device rotation of 90°, 180°, and 270°. In PowerSynth 2 another update is considered compared to previous versions, which is wire bond connectivity representation. Previously, wire bond pad locations needed to be defined by the user, and those locations needed to be calculated carefully so that the horizontal or vertical wire bonds' landing pads can be aligned. In the updated script, the user needs to declare the start and end points of a wire bond group by mentioning the "BW" keyword in the corresponding parent component geometry description line. For example, the kelvin source connection from D1 to T6 in Fig. 5(a) is represented by mentioning BW2 in both T6 and D1 declaration lines in the script. The landing point locations are automatically calculated based on the relative locations of the parent components. Since the devices can have multiple wire bonds, a specific order needs to be followed while declaring them. If any device has gate, kelvin source, and source (for power loop) type connections, then the wire bond pads need to be declared in that order. However, for some cases, if the device does not have a kelvin source connection, then the order should be gate, and then, power loop source type connections. For a successful connection, it is assumed that each device will have at least two wire bond connections: gate and power loop source.

The initial layout description script is parsed and stored in horizontal corner stitch (HCS) and vertical corner stitch (VCS) tree structures combining information from the layer stack. The basic corner stitch data structure [23] is modified to allow overlapping of tiles by implementing a hierarchical tile insertion algorithm. To identify the design constraints properly, two types of hierarchical tile are considered in each corner-stitched nodes: background and foreground tile. Since new component is inserted on top of an existing one, the parent node tile is the background tile, and the new tile considered as the foreground tile. The background tiles are used to find both minimum enclosure and spacing constraints. And the foreground tiles are used to get the minimum width and length constraints. Besides these design constraints, user-defined reliability constraints can be considered as well. For example, current-dependent minimum width (2-D) and voltage-dependent minimum spacing (2-D) are required for reliable operation at a high voltage-current rating. For 3-D layouts, the minimum clearance and creepage distance among multiple layers also need to be considered for safe operation. In PowerSynth 2, 2-D reliability constraints can be applied while generating the CGs. For each node in the tree, two CGs are created by mapping the coordinates into vertices and corresponding constraint values as edge weights. These CGs are used to generate layout solutions by edge weight manipulation through randomization. The horizontal constraint graph (HCG)

Algorithm 1 Layout Generation Workflow.

```
Parse the input geometry script
Read layer stack and design constraints
Create a root node of the structure
Create group of routing layers connected with a same via
for each connected group do
    Create an interfacing layer
    for each routing layer in the group do
        Create HCS and VCS
        Create HCG and VCG
        Evaluate HCG and VCG
for each ancestor from leaf to root do
    Perform bottom-up constraint propagation
Evaluate root node and compute available space
for each sub-tree from root to leaf do
    Perform top-down location propagation
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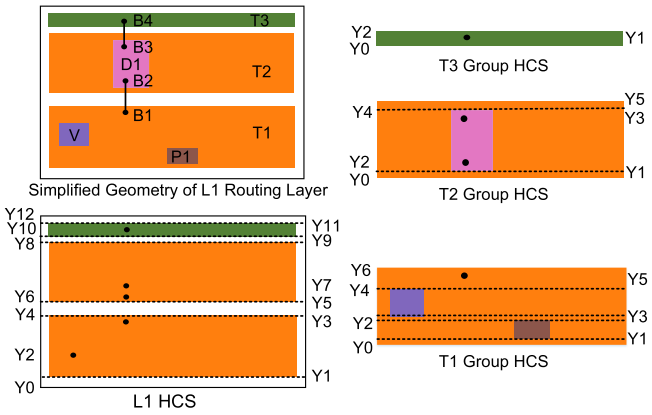


Fig. 7. Constraint propagation using a simplified example from Fig. 5(a).

maintains the horizontal relative location among the components, and the vertical constraint graph (VCG) maintains the vertical relative locations. The layout solutions can be generated by computing the vertices' locations from both graphs after the edge weight manipulation.

B. Constraint-Aware Layout Synthesis Algorithms

A high-level workflow of layout solution generation is shown in Algorithm 1. For the multilayered 3-D structure, abstract nodes (interfacing layers) are maintained to ensure the alignment of the via coordinates. After creating the HCG and VCG for each node in the tree, bottom-up constraint propagation is performed to ensure the minimum required room for the child node in the parent node. Each CG is evaluated using the longest path algorithm. Starting from leaf nodes, the longest shared subgraph between the child and parent is propagated towards the parent nodes. This bottom-up constraint propagation continues until the root node receives all necessary constraints. To demonstrate the bottom-up constraint propagation, a simplified structure of the L1 routing layer from Fig. 5(a) has been considered and shown in Fig. 7. Here, the HCS view of the L1 subtree is demonstrated. In each child's HCS (T1, T2, T3), the bonding wire landing point coordinates are represented as dots. However, in the parent HCS (L1), all propagated coordinates are shown as dots. For this simplified structure, the corresponding bottom-up constraint propagation is illustrated in Fig. 8. Each coordinate from HCS is mapped into a vertex in the VCG. Each edge in the VCG represents a design constraint. In this simple geometry, three types of constraints are considered: minimum width (W) of each component, minimum enclosure between two components (E), and minimum spacing between two components (S). In the child VCGs, there is no propagated edge, whereas, in the parent VCG, most of the edges are propagated (solid green). The weights of the propagated edges are computed at the child node's CG. The other two types of edges are: flexible (solid black) and rigid (dashed black). A rigid edge has a fixed weight having the destination as a dependent vertex. On the other hand, a flexible edge with both origin and destination as independent vertices can vary its weight. The notations of the constraint values considered in the example are: E1 through E7 represent minimum enclosure rules while S1 through S5 represent minimum spacing rules between different components. From the child nodes, the minimum necessary subgraph is propagated to their parent node. For example, in the L1 VCG, the subgraph of Y1–Y4, Y5–Y8, and Y9–Y11 contains propagated edges from T1, T2, and T3 VCG, respectively. Here, P1 through P9 are edge weights propagated from child VCGs. The detailed algorithms for solving constraints and evaluating locations are based on the previous work [22].

The root node can be evaluated in the following three modes using the top-down location propagation algorithms [22], [24].

1) *Minimum-Sized Solution:* In this mode, the root node is evaluated using the propagated minimum constraints only. This mode generates the minimum floorplan-sized solution, i.e., the most compact one with the highest power density. However, performance-wise, this solution is not optimum. It has lower loop inductance due to a smaller power loop, but the highest temperature rise due to the smallest floorplan size and compact device placement.

2) *Variable-Sized Solutions:* If the user does not have a preselected floorplan size, this mode can be used to search for an optimized floorplan size. In this mode, the floorplan size is varied arbitrarily, with the minimum constraint value as a lower bound but no upper bound. So, if the number of layouts is large enough, the methodology can explore a large solution space and find an optimum floorplan size. In this mode, the performance values have a broader range and variation.

3) *Fixed-Sized Solutions:* This mode is used after an optimum floorplan size is determined. The user can generate an arbitrary number of solutions as well. However, the randomization range is restricted with the room calculated from the difference between the given floorplan size and the minimum size. This extra room is distributed into the edge weights in two ways: uniform and weighted. This is the most-used case for the power electronic module designers as the converters generally have a specific size requirement for standardized modules.

Once the root node evaluation is performed, the locations of the shared vertices are propagated in a top-down fashion until

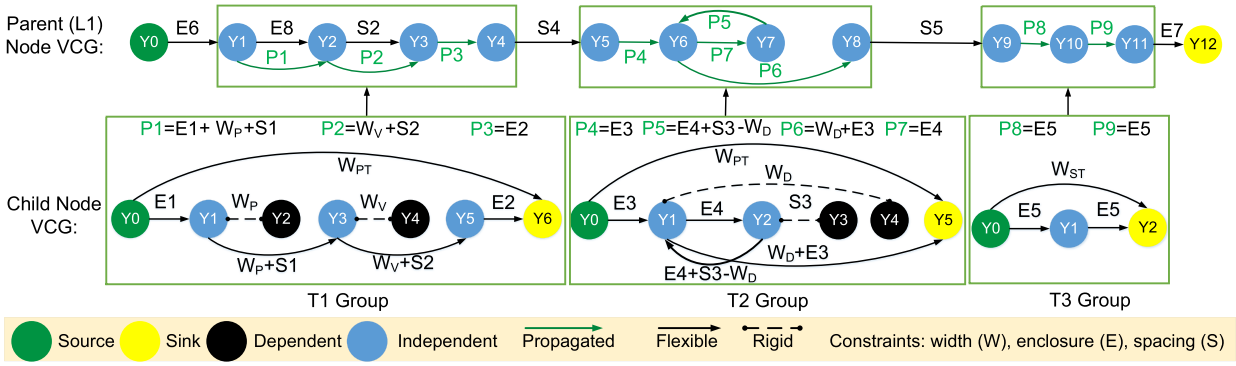
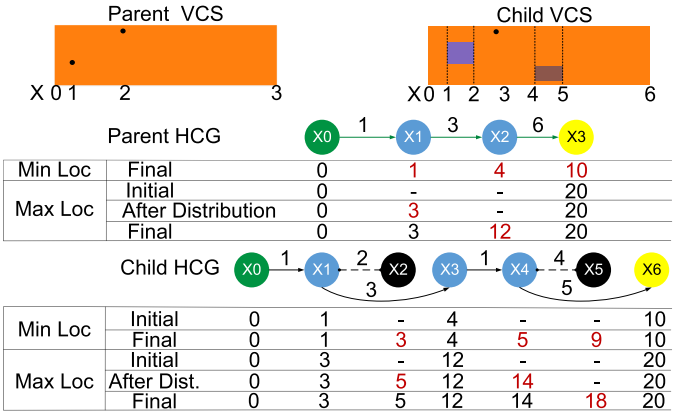


Fig. 8. Bottom-up constraint propagation illustration for HCS shown in Fig. 7. Here, subscripts P, V, D, PT, and ST represents power lead, via, device, power trace, and signal trace, respectively.



Min Loc	Final	0	1	4	10		
Max Loc	Initial	0	-	-	20		
	After Distribution	0	3	-	20		
	Final	0	3	12	20		

Min Loc	Initial	0	1	-	4	-	-	10
	Final	0	1	3	4	5	9	10
Max Loc	Initial	0	3	-	12	-	-	20
	After Dist.	0	3	5	12	14	-	20
	Final	0	3	5	12	14	18	20

Fig. 9. Top-down location propagation illustration for T1 in Fig. 7.

all leaf nodes are evaluated. This process is called top-down location propagation, where each node is allocated with some space for expansion, which creates more design variants in the solution space. A sample illustration of the top-down location propagation for minimum-sized and fixed-sized solution generation is shown in Fig. 9. Here, to simplify the illustration, a partial HCG (only the T1 group region) from the complete L1 layer (shown in Fig. 7) is considered the parent HCG. For minimum-sized solution generation, minimum edge weights are assumed as shown in the figure. The source is always considered a reference vertex, and the location is set to 0. The rest of the vertices are calculated based on the longest path. In the child HCG, shared vertices (X0, X1, X3, X6) are propagated from the parent. Therefore, these vertices' locations are evaluated in the parent node and propagated to the child node. The rest of the vertices are calculated based on the longest path from the source to that vertex. In the case of the fixed-sized solution generation, both min and max locations are necessary. Max location computation is an iterative process. In each iteration, one flexible vertex location is determined after distributing the weight from randomization. For example, in the parent node case, if the user sets the X3 vertex location at 20, the X1 vertex has room for randomization between 1 (0+1) and 11 (20–6–3). So, after distribution, if the value is set to 3, X2 must be between 6 (3+3) and 14 (20–6). Any value in that range ensures a DRC-clean solution. The child node's maximum locations are also determined similarly. The detailed algorithm is described in [22].

C. Multiobjective Modeling and Optimization

Since PowerSynth 2 can perform multi-objective optimization, fast and accurate models are required for performance evaluation to explore a large solution space within an acceptable runtime. PowerSynth 2 performs an area sweep to find the optimum solution with a higher power density. Therefore, apart from electro-thermal optimization, PowerSynth 2 can guide the user towards high-power density design without compromising other objectives. The electrical and thermal models used in this work are described as follows.

1) Electrical Modeling: To extract electrical parasitics (i.e., loop inductance, resistance, and capacitance), PowerSynth 2 has two options: an API for evaluating through FastHenry and a built-in electrical model. The loop-based method from VLSI has been adapted to capture the mutual coupling among conduction paths in the power module. This method has several advantages for high-density 3-D MCPM layouts, including more efficient mutual inductance extraction, a significantly smaller netlist size, and compatibility for parallelization [25]. First, a path-finding algorithm is applied to each layout solution to determine the current direction through each trace. These current directions are then stored in a directed graph, where they are later partitioned and grouped into two different sets, namely horizontal and vertical bundles. Each set only contains trace segments of equal length. Next, an iterative algorithm runs through each bundle to evaluate the parasitics of all segments. A lumped-elements netlist is formed during this iterative process to store all parasitic results. Finally, a current source is applied between the source and sink nets to evaluate the overall voltage drop in the loop. The loop impedance value can be calculated based on the voltage drop and input current. A significant improvement in speed and memory has been achieved while maintaining the same extraction accuracy for the loop-based method compared to FEM and PEEC models. For a 2-D case, the model has shown 56 times speedup with 6% accuracy compared to ANSYS Q3D results. There are two key reasons for the speedup using this method compared to FEM. First, this method applies the divide

and conquer programming strategy and divides the layout into multiple vertical and horizontal bundles. The loop impedance for each bundle is calculated separately and combined later. Second, to capture the backside eddy current impact on the extraction result, numerical simulations are run to form a regression model capturing this backside eddy current impact. The regression model is later used for the partial element's calculation during optimization. Although this method is efficient for 2-D layout cases, rigorous testing for 3-D layout evaluation is ongoing. Therefore, in this work, FastHenry [18] is used for the electro-thermal optimization case study for 3-D layouts.

2) Thermal Modeling: PowerSynth 2 has two options for thermal performance evaluation. First, ParaPower [19] developed by the Army Research Lab is linked with PowerSynth 2 for accurate thermal performance evaluation of 3-D layouts. Second, the built-in transient thermal model [26] can predict both static and transient thermal performance of 2-D layouts with a 3500 times speedup while keeping the accuracy within 10% compared to ANSYS Fluent. This transient model can report maximum, average, and peak-to-peak temperature for each layer. The key reasons behind such significant speedup without compromising the accuracy are as follows.

1) The 1-D Cauer thermal network representation for the structure due to the similarity between heat transfer and current flow.

2) The HSPICE engine for the *RC* network simulation, which is very fast compared to FEA.

However, FEA has more detailed meshing that helps with the accuracy, whereas the built-in model uses lumped *RC* values for each layer, sacrificing the accuracy. Although ParaPower can be used for transient simulation, the built-in model is 316 times faster than ParaPower, and hence, more suitable for optimization. In this work, ParaPower has been used for static thermal performance evaluation of the 3-D MCPM layout.

3) Layout Optimization and Finishing: In PowerSynth 2, two optimization algorithms are implemented: a built-in randomization method and a nondominated sorting genetic algorithm II (NSGAII) [27]. The randomization method generates the solution space and performs performance evaluation using the corresponding models. Then, a nondominated sorting is applied to generate the Pareto-front solutions. On the other hand, the genetic algorithm approach takes the number of generations as input and applies crossover and mutation to spawn a new generation of the solutions. Based on the ranking, a subset is passed to the next generation. This procedure continues until it reaches the maximum number of generations. In this process, the layout is represented by a design string that is created by concatenating the longest path weights of each node and iterating through the hierarchy tree [22]. When a solution is generated from the design string, it is evaluated by the performance models and follows the genetic algorithm steps to create a new design string. Finally, PowerSynth 2 reports the solution space and Pareto-optimal solution set in a user-interactive solution browser. PowerSynth 2 export feature can be used to perform export to commercial CAD tools and optimized design can be taped out for fabrication.

V. PowerSynth 2 Design Examples

A. High-Density Power Module Designs

A high-density MCPM layout can be achieved with four types of 2-D/2.5-D/3-D packaging technologies. The 2-D planar power loop can be converted into a vertical loop to reduce the power loop parasitics. Double-sided cooling or embedded cooling can improve the thermal performance of the high-density layouts. However, in some cases, the fabrication complexity can be significantly increased due to the compact placement and routing of components in a multilayered fashion. Each of these packaging technologies is described and PowerSynth 2 generated solutions are shown as follows.

1) Flip-Chip Module: In flip-chip designs, the devices are connected in a flipped fashion with the routing traces. Fig. 10(a) shows a half-bridge 2-D flip-chip module that has solder balls for connecting the gate, source, and drain with traces. The drain has an extended metallic connection that converts the typical vertical device into a planar one. In this configuration, no via is used, and the OUT trace has high-side devices' sources and low-side devices' drains on the same plane. Flip-chip 3-D module needs multiple direct-bonded coppers (DBCs), and the fabrication complexity of such designs is much higher compared to the wire bonding technology.

2) Hybrid 3-D Module: A hybrid 3-D module refers to the package where both wire bond and metallic posttype connections are used. Wire bonding is used for gate and kelvin source connections, whereas metallic post connectors are used for power loop connections. The initial 3-D structure and minimum-sized solution generated by PowerSynth 2 are shown in Fig. 10(b). Here, two DBCs are connected face-to-face through metallic post-type connections. The L1 layer has the OUT terminal and low-side devices' drain connections. The sources (S) are connected to the L2 layer through metallic posts. L2 layer has dc+ and dc- terminals, as well as high-side devices' drain connections. Double-sided cooling can be enabled by attaching heat sinks on both sides. However, the power loop area is increased due to the planar part. To make a vertical power loop, four routing layers are required, where there needs to be one through DBC via type connection as shown in [24]. However, the metallic post attachment to the device source pads is a challenging task as there is no established recipe for that.

3) Wire-Bonded 3-D Module: A sample 3-D structure of the wire-bonded 3-D module is shown in Fig. 10(c). The planar view of each layer of the 3-D structure is shown in Fig. 5(a). Here, the bottom layer (L1) consists of high-side power devices, gate and kelvin source connections, and dc+ and OUT terminals. The top layer (L2) has low-side power devices with gate and kelvin source connections and dc- terminal. A through ceramic via is used to connect both layers' OUT traces. Thus, a 3-D half-bridge wire-bonded layout is created using two routing layers. Since devices are on both sides of the structure, heat sink attachment is not possible for thermal management. Therefore, a DBC ceramic board with an embedded cooling channel is required for the best thermal performance. The current rating of such design is limited by the number of parallel vias and their diameter. Another wire-bonded structure is possible using two

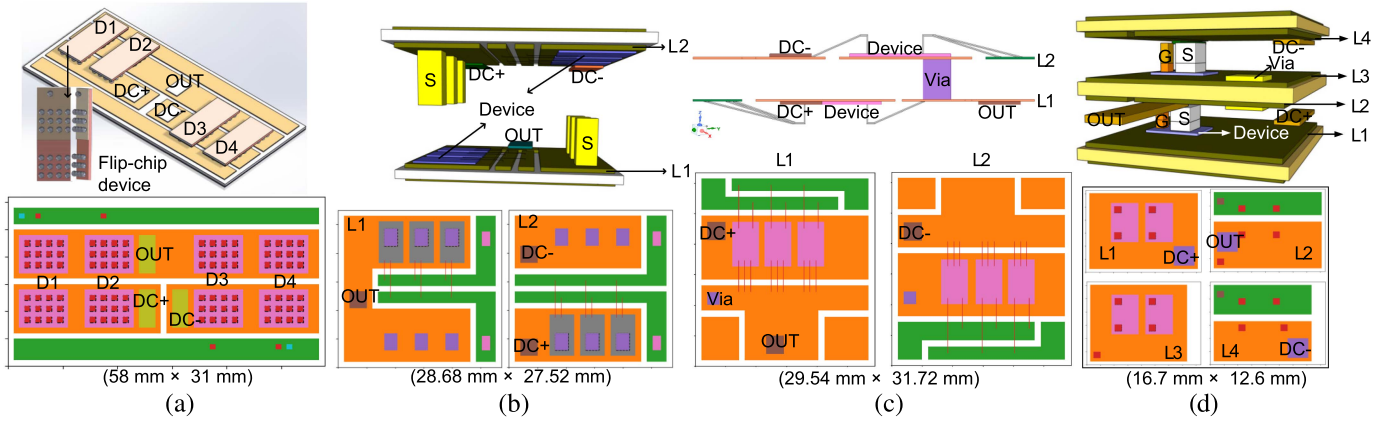


Fig. 10. CAD structure and PowerSynth 2 generated minimum-sized solution of high-density packaging layouts. (a) Flip-chip 2D module. (b) Hybrid 3D module. (c) Wire-bonded 3D module. (d) Wire-bondless 3D module.

substrates and replacing the through DBC vias with metallic posts, where the face-to-face stacking of the devices is required, as shown in [28]. In such structures, the heat sink can be attached to both DBCs, and the volume between two device layers can be filled with encapsulant gel or LTCC interposer for electrical isolation. Although this structure can have cheaper thermal management than embedded cooling, the fabrication complexity is much higher than the single substrate through ceramic via case as the metallic post connection is required between two substrates.

4) Wire-Bondless 3-D Module: From the literature, it is evident that the bonding wire in the power loop is the critical part that contributes to the loop parasitics and is more prone to failure compared to other parts in the module. Eliminating the wire bonding, wire-bondless 3-D designs are investigated. Fig. 10(d) shows a sample 3-D wire-bondless structure with per-layer layouts. Here, three DBCs have been used to form a half-bridge module. Among the four routing layers, L2 and L3 are connected through a via. L1 layer has a dc+ terminal, and high-side devices with both source (S) and gate (G) connections are ported to the L2 layer through metallic posts. The L3 layer has the low-side devices' drains, which sources (S) and gates (G) are connected to the L4 layer that contains the dc- terminal.

Each aforementioned packaging technology has its own appeal based on application. The user needs to choose the packaging architecture before designing the module layout. The aforementioned results demonstrate that PowerSynth 2 can handle most of the state-of-the-art high-density packaging layout architectures available in the literature. They can be optimized using PowerSynth 2 in the similar way as the wire-bonded 3-D case is described in Section V-B. Optimization results of flip-chip, hybrid, and wire-bondless example designs can also be found in [20], [24], and [22], respectively. Currently, PowerSynth 2 is the only tool that is the one-stop solution for the users, where all of these high-density packaging architectures are supported. Generic, hierarchical layout geometry script, and efficient and scalable algorithms in PowerSynth 2 have made it possible for these diverse high-density designs.

B. Experimental 3-D Design Optimization

Although PowerSynth 2 can optimize all the aforementioned packaging technologies, 3-D CAD-flow validation through hardware prototyping depends on complexity, cost, and equipment for module manufacturing. Considering the fabrication complexity, the wire-bonded 3-D module design has been chosen [shown in Fig. 10(c)]. This layout has a few benefits over any 2-D design: a vertical power loop, reduced footprint size, embedded cooling opportunity, etc. This module is a brand-new 3-D module with wire-bonded devices on both sides of a substrate. This module initial layout design requires several considerations like copper utilization area maximization, through-ceramic-via connectivity, signal trace orientation, and power loop area minimization. Also, an innovative cooling idea has been proposed for such a compact high-density module. Embedded microcooling has been studied in [21]. However, any previous module design having a DBC substrate with an embedded liquid cooler could not be found in literature although some DBC companies offer such substrates. This new cooling method is only partially implemented in this prototyping due to the fabrication complexity and cost. However, to prove the concept of such cooling in a high-density module, experiments have been performed. Since PowerSynth 2 has a hierarchical optimization feature, the relative location of the components can be considered from both global and local perspectives. PowerSynth 2 can change the relative location of the components across different hierarchy nodes (global). However, within the same node (local), the components are not allowed to change their relative location. This strategy is chosen as a result of tradeoff between runtime and design variation. If the locations of the components are allowed to change locally, the corner stitching data structure and CG need to be created for each solution to avoid DRC violation, which will introduce runtime overhead. Currently, the corner stitching data structure is created once and the CG is modified to generate new solutions. Due to this strategy, the initial layout of the module needs to be designed carefully to reduce coordinate correlation among components in the same trace island. Also, the fabrication steps need to be

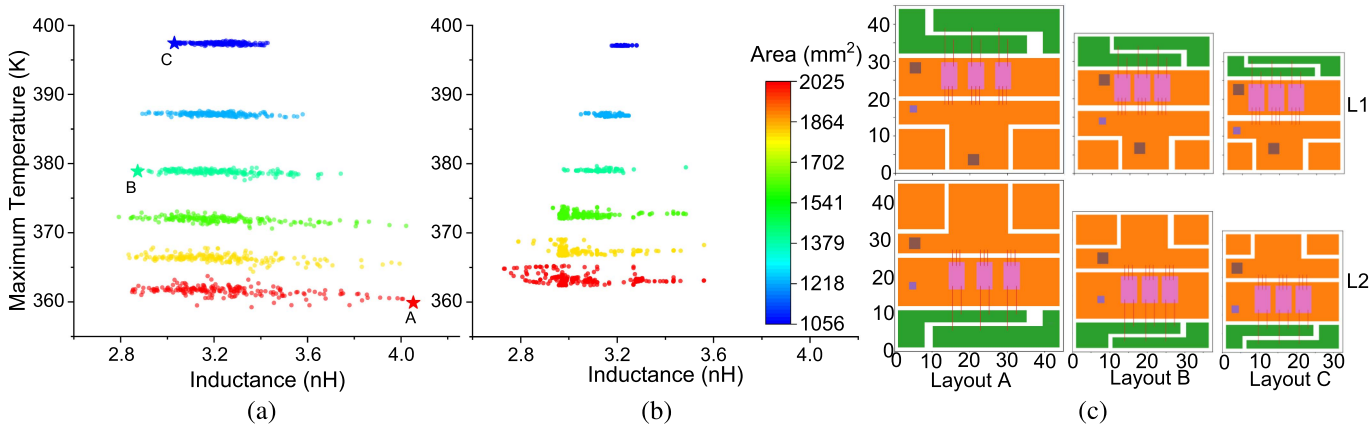


Fig. 11. Solution space generated by PowerSynth 2 using (a) randomization, (b) NSGAII, and (c) 2-D view of the three selected solutions.

planned as both sides of the single DBC have devices. In this section, the electro-thermal optimization flow of PowerSynth 2 using the 3-D wire-bonded module is demonstrated.

The optimization target is reducing power loop (from dc+ to dc-) inductance, static maximum junction temperature, and increasing power density. FastHenry [18] is used for loop inductance extraction, and ParaPower [19] from Army Research Lab is used for static thermal evaluation. Before optimizing the layout, the electro-thermal performance of the minimum-sized solution [shown in Fig. 10(c)] is evaluated. Since the 3-D structure has bare devices with wire bonding on both sides, there is no baseplate attached to this design. For thermal performance evaluation, a heat transfer coefficient on an even surface is required as an input to the ParaPower interface. To have an even surface, the 3-D structure is considered to be encapsulated with silicone gel (thermal conductivity 0.2 W/mK) with a thickness of 0.5 mm on both sides. To mimic the forced air cooling, the heat transfer coefficient of 350 W/m^{2}K is applied on both sides of the encapsulated DBC substrate (Cu/ AlN/ Cu) with filled Cu vias. The ambient temperature is set to 300 K. The power loop inductance is found 3.26 nH at 1 MHz, and the maximum junction temperature is found 381.68 K for 2.5 W heat dissipation for each device. Since the minimum-sized solution provides the most compact solution, to optimize this layout assuming the same boundary conditions, six different floorplan sizes are considered ranging from 1056 to 2025 mm^2. For each floorplan size, both randomization and NSGAII are used to generate solution spaces. The result is shown in Fig. 11. For randomization, each floorplan size has 200 solutions, and the runtime for solution generation and evaluation is 100 and 2500 s, respectively, on a server with dual Intel Xeon Silver 4210 CPUs and 384-GB memory. On the other hand, for the NSGAII, the number of generations varied from 25 to 35 with the increasing floorplan size. The average runtime for each solution is approximately 1 min. Since NSGAII generates and evaluates one solution at a time, parallelization on performance evaluation is not possible. Therefore, the runtime is higher than the randomization. From the solution space plot, NSGAII finds better solutions with larger footprints but has a narrower solution space than randomization. From both solution spaces, the balanced solution can be chosen and fabricated. In this study, the optimized layout is chosen from the randomization solution space. Because for the same footprint size (<1800 mm^2), it has a better electrical performance. However, tuning NSGAII parameters (crossover, mutation, etc.) might lead to similar results with randomization. To demonstrate design variation, three corner solutions have been chosen from the randomization solution space and labeled in Fig. 11(a). These solutions represent the tradeoff among all three objectives. The planar view of each layout is shown in Fig. 11(c). The performance metrics comparison is shown in Table I. From the layouts, it is evident that Layout A has the highest footprint with higher loop inductance and a lower temperature rise. Layout C has the smallest floorplan size with the highest temperature rise and relatively lower loop inductance. Layout B shows the tradeoff between two performance values and achieves a balanced electro-thermal performance with higher power density compared to the solutions with the same floorplan size as Layouts A and C. The initial layout of each layer of the 3-D structure is shown in Fig. 5(a). This layout is evaluated under the same boundary conditions as the optimization study. A brief comparison between the initial and optimized layout is shown in Table I. From the comparison results, it is clear that PowerSynth 2 not only synthesizes a manufacture-ready layout but also performs electro-thermal co-optimization.

TABLE I
PERFORMANCE METRICS FOR THE THREE SELECTED LAYOUTS

Layout	Inductance (nH)	Max. Temp. (K)	Size (mm^2)	DRC-Clean
Initial	3.19	498.21	34 × 28.5	No
A	4.05	359.87	45 × 45	Yes
B	2.87	378.88	37.5 × 37.5	Yes
C	3.03	397.41	32.5 × 32.5	Yes

The selected Layout B has been further tuned before taping out for fabrication. Since the optimization target was to reduce the power loop inductance, the gate loop in the L2 layer is not optimized. Therefore, the OUT trace width in the L2 layer is further reduced, and the width of the dc- trace is increased by 1.5 mm. A 3 × 3 via array is used to enhance the current rating. These postlayout optimizations helped in reducing the gate and kelvin source wire bond lengths as well as the power loop length. This modified layout has a power loop inductance of 2.77 nH at 1 MHz. The updated layout has been exported to SolidWorks for 3-D rendering. The final layout and exported 3-D model are

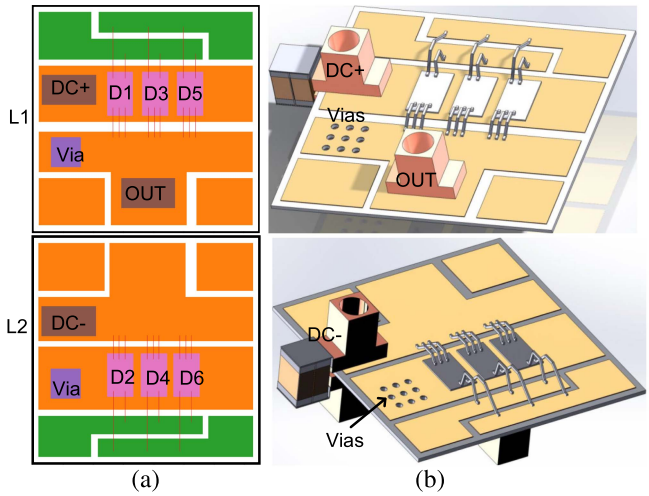


Fig. 12. (a) Modified layout of solution B. (b) Exported 3-D structure.

shown in Fig. 12. In the 3-D model, the decoupling capacitor is also shown between dc+ and dc- terminal. This postlayout tuning is a manual and optional step, which can be performed with the exported design files.

VI. Software and Hardware Validation

A. 3-D Power Module Fabrication

The CAD drawing of the optimized layout is fabricated with a gold-plated DBC substrate (0.1 mm Cu/ 0.5 mm AlN/ 0.1 mm Cu). The gate and kelvin source headers are chosen according to the gate driver interfacing pins. The power leads are machined from copper bars at the High Density Electronics Center (HiDEC). CPM3-0900-0010 A SiC devices from CREE are used for the module. All these parts are assembled at HiDEC to manufacture the module. Two sets of graphite fixtures are machined to make the die and terminal attachment process smoother. One set of fixtures is used for high-side components assembly and another for the low side. The attachment process is divided into two steps. Since the devices need to be attached on both sides of the DBC, the high-side layer components are assembled first using a Pb95/Sn5 preform solder material as it has a higher melting temperature (308 °C). The substrate is plasma cleaned priorly to remove any organic residue. Then, a vacuum furnace performs the attachment process. For low-side components, the Sn63/Pb37 eutectic solder paste with a lower melting temperature (183 °C) is used. Then, the substrate is cleaned using the flux remover solution and plasma cleaner to remove any organic residue. Finally, the substrate is placed in another custom graphite fixture, and 12-mil automatic wire bonder is used to perform the wire bonding on both sides. Then, the 1-μF capacitor is soldered between the dc+ and dc- terminal edges. The final fabricated design is shown in Fig. 13.

B. Functionality Verification

A double pulse test (DPT) is performed to validate the functionality of the assembled module. The test setup of the DPT is shown in Fig. 14. CGD1700HB3P-HM3 from CREE is used as the gate driver. The load inductor used in the setup has an inductance of 157 μH. As the module has no encapsulation, the test is performed at a 300-V/15-A rating for safety considerations. PowerSynth 2 extracted parasitic netlist (shown in Fig. 14) is used to simulate the double pulse test. The Vds and load current waveform comparison are shown in Fig. 15. The current is measured using a mini Rogowski coil around the wire, adding some noise to the collected data. The maximum voltage overshoot of Vds is approximately 27 V. The low-frequency ringing in the Vds is due to the 1 μF decoupling capacitor used in the module. This capacitor has to be used to decouple the parasitics from the external connections as there is no custom busbar is used in the test setup. Both voltage and current waveforms are within acceptable accuracy for simulation compared to the measurement results. A 200-MHz voltage probe has been used for voltage measurement. From the Vds waveform, there shows no high-frequency ringing at the turn-OFF cycle in both simulation and experiment. This is because of low parasitic inductance, high gate resistance (5 Ω from the gate driver and 2 Ω from the device), high rise (400 ns), and fall (230 ns) time of the gate driver output signal, etc. Since the turn-OFF ringing frequency could not be measured from the experiment, the loop inductance cannot be verified through DPT. However, from the switching waveforms, it is clear that the assembled optimized module is fully functional.

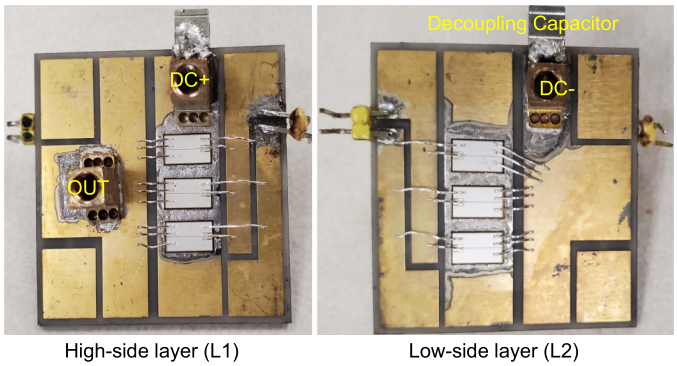


Fig. 13. Fabricated 3-D module.

C. Electrical Validation

To validate the power loop inductance, an impedance analyzer is used. For this test, another copy of the optimized via a connected DBC substrate is used. In this device under test (DUT), no SiC devices are attached. For the power loop, wire bonds are used at the device locations. For each device position, three parallel 5-mil Aluminum wires are used. The module (DUT) image is shown in Fig. 16(a). A Keysight E4990 A impedance analyzer is used to measure the loop inductance and impedance. Based on the sensitivity and frequency range of the analyzer, 1–10 MHz is selected for this test. A custom printed circuit board fixture [shown in Fig. 16(a)] is used to interface between the impedance analyzer BNC ports and the module design. An open and short calibration is performed before measuring the DUT. For short calibration, two similar connectors (DC+ and DC-) as used in the DUT are soldered at one side to nullify the terminal parasitics. The measurement results are shown in Fig. 16(b).

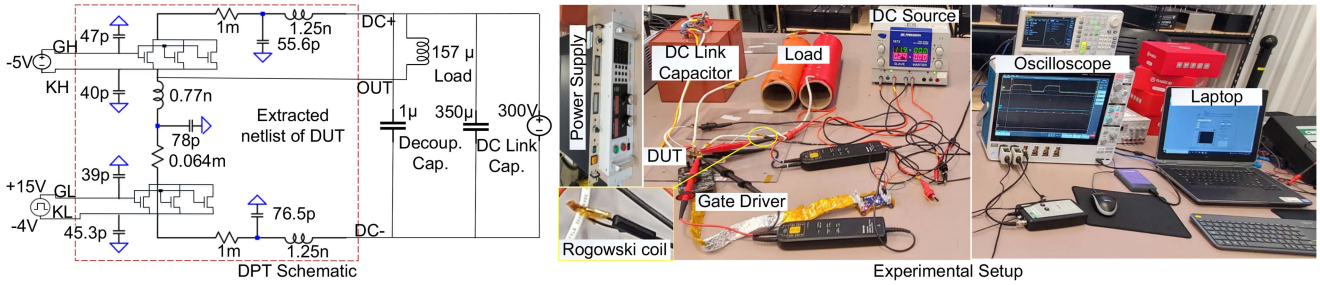


Fig. 14. Double pulse test schematic and experimental setup.

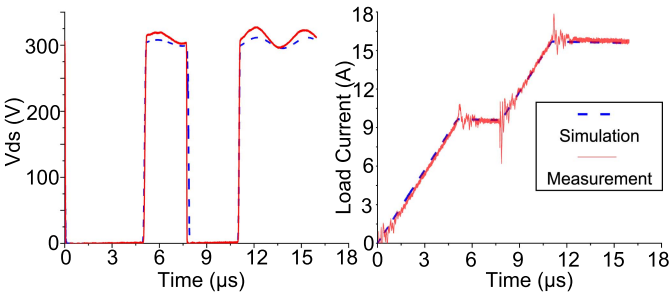


Fig. 15. Double pulse test comparison on Vds and load current.

TABLE II
COMPARISON BETWEEN THERMAL MEASUREMENT, ANSYS, AND PARAPOWER

Case	Maximum Temperature (°C)			% of Mismatch
	D1	D3	D5	
Measurement	37.00	38.80	37.90	-
ANSYS	39.76	41.54	40.23	7.06%
ParaPower	40.75	42.30	40.78	9.02%

For electrical model validation, a frequency sweep is performed within the selected frequency range, and both loop inductance and resistance data are collected. Shown in Fig. 16(b), the max inductance error is 13.4% (3.43 versus 2.97 nH at 1 MHz), while the max impedance error is 12.5% (0.20 versus 0.175 Ω at 10 MHz). There are several uncontrollable factors, which are as follows.

1) From the impedance analyzer datasheet, it is evident that for low impedance measurement case (<200 mΩ), the analyzer itself has a 10% error that decreases with the increasing frequency [Shown in Fig. 16(b)].

2) The short calibration cannot perfectly nullify the terminal impedance impact as the short terminals are not connected exactly the same way as those are in the module.

Although the absolute mismatch is around 13%, considering the very low impedance and the analyzer error, the measurement is still close to the model prediction.

D. Thermal Validation

The simplified boundary conditions used in the optimization flow are challenging to reproduce in the lab environment due to several reasons, which are as follows.

1) Encapsulant gel is not used for the fabricated module, which makes it impossible to create an even surface on both sides of the module.

2) The assumed heat transfer coefficient is for forced air cooling on both sides, which is hard to achieve in such small scale experiment setup as no direct relationship is found in the literature with low fan speed and heat transfer coefficient.

3) More complicated equipment is required to match the heat transfer coefficient of the forced air cooling.

Such a high-density power module cannot be used reliably without any active cooling. Therefore, an alternative cooling method is proposed. A custom DBC can be manufactured that has an embedded liquid cooling channel by adding some electrical impedance overhead in the power loop, as shown in Fig. 17. To demonstrate the thermal solution, a cold plate is used for active cooling, resembling the embedded cooling channel. For this test, only the high side of the half-bridge module is assembled and attached on top of the cold plate, as shown in Fig. 18, using a silicone-based interfacing material (thermal conductivity 13.9 W/mK). A dc power supply is used for providing current through the devices. A multimeter is used to measure the voltage drop across the devices. A coolant loop with water cooling (flow rate 0.5 gallons/min) is set up through the cold plate. A thermal camera from FLIR is used to record the temperature of the module. The devices are connected to operate in diode mode (higher resistance) as the purpose is heat generation only. At 15-A supply current, total heat dissipation across three parallel devices is 30.6 W. The inlet and outlet temperatures of the cold plate are 22.2 °C and 22.43 °C, respectively. The measured case temperature is 25.6 °C. The resultant IR image is shown in Fig. 18. Based on Newton's law of cooling, the effective heat transfer coefficient is approximately 7394 W/m^{2}K. This heat transfer coefficient is applied on the bottom side, and 10.2-W power is provided for each device in ParaPower evaluation. The ambient temperature is set to the same as the experiment (24 °C). The maximum junction temperature from ParaPower thermal model is 42.30 °C. For the same boundary condition and module structure, ANSYS Workbench has reported 41.54 °C as the maximum temperature. The comparison result for each device among different sources is shown in Table II . From the results, it is clear that ParaPower predicted temperature is within 10% error. A few factors in the measurement cannot be considered in simulation, such as measurement equipment (power supply, multimeters, thermocouple, and IR camera) accuracies, voids in the solder attach, and heat dissipation through radiation. Therefore, the equivalent heat transfer coefficient is not 100% accurate. However, the overall thermal result still agrees with the model prediction.

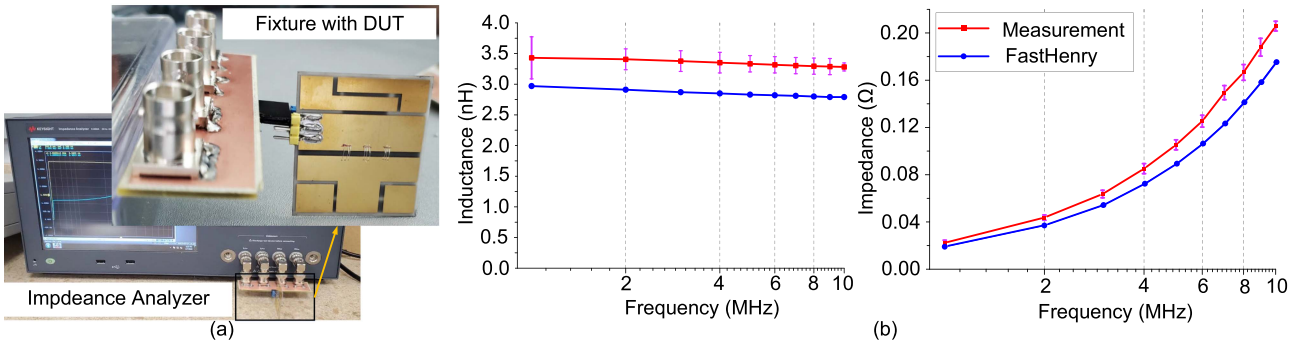


Fig. 16. (a) Impedance measurement setup. (b) Result comparison for the power loop.

TABLE III
SUMMARY OF HIGH-DENSITY PACKAGING DESIGNS

Source	Architecture	Packaging	Power Loop		Cooling	Max V (V)	Max I (A)	Dev./Pos.	Area (mm^2)	Design
			Type	L (nH)						
[12]	2D HB	Wire-Bonded	Planar	7.44	Single	1200	40	1 SiC	54.8 × 28	automated
[15]	2D HB	Wire-Bonded	Planar	8.33	Single	1200	80	2 SiC	40 × 40	automated
[11]	2D HB	Wire-Bonded	Planar	5.59	Single	1200	160	4 SiC	60 × 40	automated
[29]	2.5D HB	Hybrid	Vertical	2.60	Dual	1200	90	1 SiC	40 × 37	manual
[30]	2.5D HB	Hybrid	Vertical	3.38	Single	1200	24	1 SiC	21 × 11.5	manual
[31]	2.5D HB	Hybrid	Vertical	4.3	Single	1200	80	2 SiC	23.7 × 14.2	manual
[32]	2.5D FB	Wire Bondless	Vertical	4.5	Dual	1200	200	4 SiC	76.9 × 74.9	manual
[15]	2.5D FB	Wire-Bonded	Planar	8.33	Single	1200	80	2 SiC	80 × 40	automated
[33]	3D HB	Wire-Bondless	Vertical	0.93	Dual	650	120	2 GaN	45 × 35	manual
[34]	3D HB	Flip-chip	Vertical	4.5	Dual	900	388	2 SiC	28 × 50.5	manual
[34]	3D HB	Wire Bondless	Vertical	5.1	Dual	3300	100	2 SiC	27 × 46.4	manual
This Work	3D HB	Wire-Bonded	Vertical	3.43	Embedded	900	582	3 SiC	37.5 × 37.5	automated

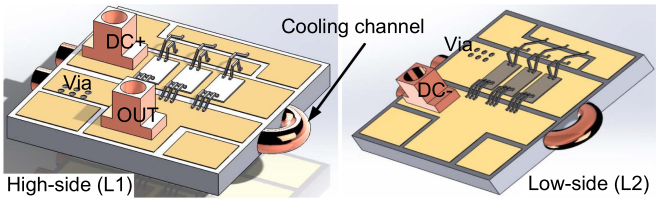


Fig. 17. Proposed embedded cooling for the 3-D power module.

E. Optimization Flow Validation and Comparison

The aforementioned experimental results have essentially validated the performance evaluation models (FastHenry for electrical and ParaPower for thermal) through module prototyping and testing of a representative case from the solution space. Since the chosen optimized design is within 10–13% accuracy of the predicted values, it is clear that the models are reliable enough to be used for 3-D MCPM layout evaluation. Therefore, the optimization flow is hardware validated, as reliable models are used to evaluate the objectives.

Since there is no design tool like PowerSynth 2 that can optimize 2.5-D/3-D high-density modules, the optimization results are compared against mostly manual designs. However, there are two 2-D half-bridge (HB) module design cases, which are optimized by the automated methodology proposed in [11], and [12]. Compared to these two optimization results, PowerSynth 2 has achieved significant speedup with comparable performance values. For example, PowerSynth v1.9 optimized module [15], which is also generated by PowerSynth 2 and took only 1288 s for 100 generations, whereas the methodology in [11] took almost 5400 s for 30 generations, and the authors in [12] took 266,343 s for ten generations of NSGAII. The optimized design from [11] has a lower power loop inductance compared to PowerSynth design as they have two parallel power loops with two snubber capacitors. Most of the commercial modules from the power electronics industry are wire-bonded 2-D designs. Therefore, high-density 2.5-D/3-D WBG power module designs are mainly found in the literature. From Table III, it is clear that PowerSynth 2 optimized 3-D design has achieved comparable or better performance compared to all other manual designs. Provided the necessary manufacturing capabilities, PowerSynth 2 optimized design (37.5 mm × 37.5 mm) can achieve 372.48 VA/mm^2 power density assuming the module has an output power with rated peak voltage (900 V) and current (194 A) of each parallel device, which is among the highest power density for bare modules compared in the table using the same power density calculation method. The power loop inductance value is not the lowest since most of the inductance comes from the wire bonds. However, the vertical power loop has a reduced loop inductance compared to most of the other 3-D designs. Therefore, it is clear that PowerSynth 2 optimized design can even outperform many manual designs with SOTA manufacturing capability. Although the embedded cooling concept is not fully implemented in the manufactured module, PowerSynth 2 can optimize design prototypes to push the power packaging industry toward higher power density.

VII. CONCLUSION

PowerSynth 2 CAD flow is demonstrated for high-density 2-D/2.5-D/3-D and heterogeneous MCPM physical designs. The capability to optimize all 2-D/2.5-D/3-D power modules has

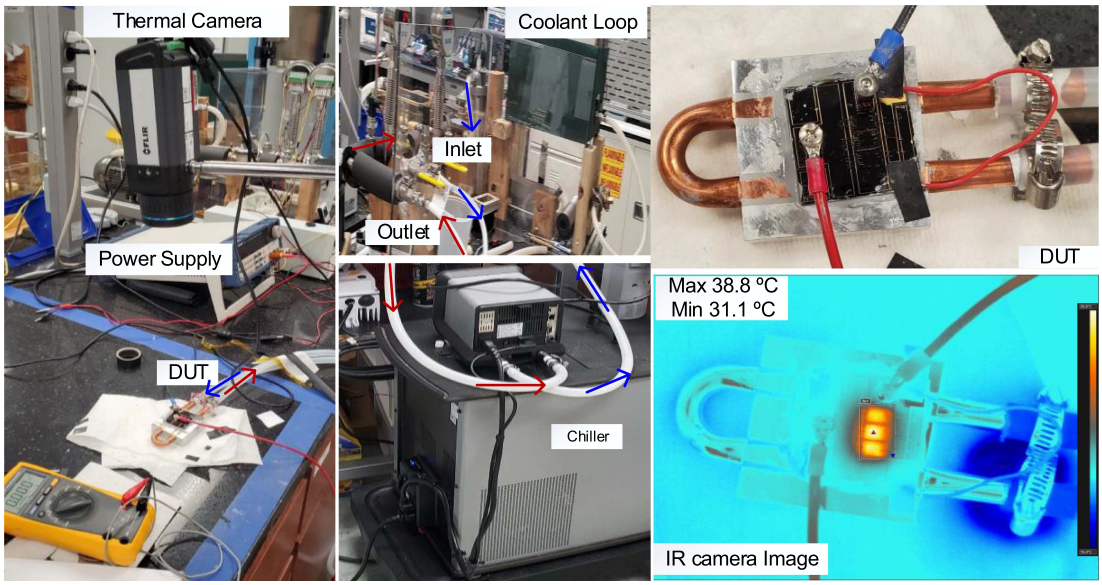


Fig. 18. Thermal test setup and temperature measurement result.

reached state-of-the-art as generic, scalable, and efficient algorithms can adapt to most existing packaging technologies in the industry. PowerSynth 2 can simulate and optimize high-density layout solutions beyond the current manufacturing capability, which provides an early testing platform for future packaging and thermal solutions. This module-level design framework can also be extended toward system-level optimization. A high-density 3-D MCPM layout is optimized and validated through a fabricated 3-D SiC power module. The measurement and FEM simulation show a close agreement with PowerSynth 2 predicted electrical (within 13%) and thermal (within 10%) results for the 3-D layout with minimum parasitics. There is room for improvement, such as automatic netlist-to-layout synthesis, changing local relative location among components by introducing optimization algorithms like simulated annealing, handling non-Manhattan routing, etc. Research and development are ongoing to overcome these limitations. In addition, our new electrical, and reliability models will be included for faster runtime and lifetime estimation. Also, PowerSynth v2.0 is released with new features and updated documentation.

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Imam Al Razi (Student Member, IEEE) received the B.Sc. degree in electrical and electronic engineering from the Bangladesh University of Engineering and Technology, Dhaka, Bangladesh, in 2016, and the Ph.D. degree in computer engineering from the University of Arkansas, Fayetteville, AR, USA, in 2022 .

During his Ph.D., he worked in computer-aided design tool development for power electronics as a National Science Foundation's Engineering Research Center for Power Optimization of Electro-Thermal Systems student. He is currently a Design Automation Engineer with Intel Corp, Oregon, USA. His research interest includes developing novel tools, flows, and methodologies to improve the performance of cutting-edge integrated circuit design technologies.

Quang Le (Student Member, IEEE) received the B.S. (summa cum laude) and Ph. D degrees in in electrical engineering from the University of Arkansas, Fayetteville, AR, USA, in 2015 and 2022, respectively.

He is currently a Software Developer with Analog Mixed Signal group, Cadence Design Systems, California. During his Ph.D., he worked with Dr. A. Mantooth's Mixed-Signal Computer-Aided Design (MSCAD) lab, where his main research focused on design automation and optimization tools for power electronics modules. In 2019, he served as a Student Leader with the National Science Foundation's multiuniversity, multidisciplinary Engineering Research Center for Power Optimization of Electro-Thermal Systems.

Dr. Le was the recipient of first place in ECCE 2021 Conference's Software Demonstration Competition, in 2021.

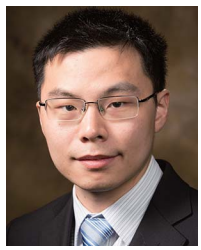
Tristan M. Evans (Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering, in 2009 and 2011, respectively, from the University of Arkansas, Fayetteville, AR, USA, where he is currently working toward the Ph.D. degree in electrical engineering.

He joined the R&D Department, ROHM Semiconductor, Kyoto, Japan, as an Assistant Researcher focusing on new die attach technology for SiC power devices and thermal modeling of SiC power modules. In 2016, he was awarded the Distinguished Doctoral Fellowship with the University of Arkansas, where he is currently a Research Assistant. His current research interests include developing design automation tools for power electronics modules.

H. Alan Mantooth (Fellow, IEEE) received the B.S.E.E. and M.S.E.E. degrees in electrical engineering from the University of Arkansas, Fayetteville, AR, USA, in 1985 and 1986, respectively, and the Ph.D. degree in electrical engineering from Georgia Tech, Atlanta, GA, USA, in 1990 .

After Ph.D., he joined Analogy, Beaverton, OR, USA, a startup company. In 1998, he joined the faculty of the Department of Electrical Engineering, University of Arkansas, where he is currently a Distinguished Professor. He helped establish the National Center for Reliable Electric Power Transmission, University of Arkansas, in 2005. He serves as the Executive Director with the NSF Industry/University Cooperative Research Center on GRid-connected Advanced Power Electronic Systems (GRAPES) and the Deputy Director with the NSF ERC on Power Optimization of Electro-Thermal Systems. His research interests include analog and mixed-signal integrated circuit design and computer-aided design, semiconductor device modeling, power electronics, power electronic packaging, and cybersecurity.

Dr. Mantooth currently serves as a Senior Past-President for the IEEE Power Electronics Society and the Editor-in-Chief for the IEEE Open Journal of Power Electronics. He holds the 21st Century Research Leadership Chair in Engineering. He is a Member of Tau Beta Pi, Sigma Xi, and Eta Kappa Nu, and a Registered Professional Engineer in Arkansas.



Yarui Peng (Member, IEEE) received the B.S. degree in microelectronic engineering from Tsinghua University, Beijing, China in 2012, and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2014 and 2016, respectively.

He is currently an Assistant Professor with Computer Science and Computer Engineering Department, University of Arkansas. His research interests include computer-aided design, analysis, and optimization for emerging technologies and heterogeneous integration with advanced packaging, such as 2.5-D/3-D integrated circuits and wide band-gap power electronics. He studies design methodologies and optimization algorithms for parasitic extraction, signal integrity, power integrity, and thermal reliability. He also develops design automation tools for power electronics to improve performance, reliability, and productivity.

Dr. Peng was the recipient of Best Paper Awards in SRC TECHCON 14, ICPT 16, and EDAPS 17 and the NSF CAREER Award in 2021.