

Factoring Interacting Stress Mechanisms in Design for Reliability of Extreme Environment Power Modules

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Abstract—As power densification demands are placing electronic packages under greater reliability risk, the consequences of complementary or interacting stresses in producing failure are becoming increasingly significant. As such, it is important that reliability methods and package designs consider how multiple-stress interactions may impact product life. Here, the coordination between a novel accelerated testing method and electronic design automation efforts has demonstrated a successful optimization approach for a wire-bonded 2D module layout combining failure mechanisms of electromigration and mechanical stressing. Utilizing custom, physics-of-failure approaches in accelerated testing, interactions can be observed in failure acceleration, which then can be incorporated into design for reliability (DfR) optimization tools. The PowerSynth 2 platform has been utilized as a DfR tool to perform a rapid reliability evaluation incorporating multistress scenarios. This work demonstrates the value added to reliability evaluation techniques when accounting for interacting failure mechanisms and suggests that next-generation power devices consider these effects in lifetime estimation.

Keywords—Accelerated testing, design automation, design for reliability, interacting failure mechanisms, layout optimization, power electronics

INTRODUCTION

Device and packaging reliability remains a significant element of delivering robust, power-dense electronics, especially where wide bandgap (WBG) semiconductor technologies enable higher operating temperatures and voltages. Issues like thermomechanical stress, materials degradation, and diffusive mobility-driven voiding are not trivial, and complexities of variegated failure mechanisms lead to difficulty in identifying accurate lifetimes. With electrification needs anticipated to exceed 1 kW/cm^2 and operating temperatures $>200^\circ\text{C}$, module packaging technology and materials impede reliable operation for mission critical systems, particularly in the form of interconnect reliability. Highly transient power needs arising from pulsed and continuous duty energized systems or rapidly changing traction demands in electrified vehicles introduce high intermittent temperatures as well as thermomechanical stresses that accumulate damage in interconnects—all concurrent with high current density operation and vibrational stresses that also

reduce operating lifetimes. These coupled and interacting failure risks must be identified early in the design cycle to ensure robust operation, for which reliability life prediction could ideally be integrated into electronic design automation (EDA), so as to produce reliability-optimized, power-dense systems.

With WBG device current capabilities soaring to hundreds of amps, temperatures arising from conduction and switching losses are lowering packaging lifetimes, with interconnect metallurgies subjected to extreme current, temperature and thermomechanical stresses that lead to reliability failure mechanisms such as electromigration (EM) [1, 2]. At its core, EM is a combinatorial failure mode that appears under the combined influence of high-temperature-enabled diffusivity and electromotive metal ion migration caused by high current density [3-5]. Yet even beyond this, coupled thermomechanical risk and other failure driving factors like humidity or strain accelerated failure can overlap in system design, leading to premature failures that would be undetected by uni-dimensional accelerated stress testing, typical of those performed in standards-based qualifications. Several instances of overlapping accelerating stress factors have been noted in literature, where thermal cycling (TC) and vibrations, humidity and TC, or voltage and temperature interact to promote accelerated failure [6-11]. For example, EM-induced voids further amplify risk from TC stress with weakened interconnections, so that when considering high current and temperature WBG device interconnects, layout and thermal schemes ought to be evaluated together. Unfortunately, these compounded reliability driving factors cannot be easily assessed in common accelerated testing, nor can they be captured using simple design rules.

Ideally, electrical, thermal, and mechanical design co-optimization need to identify and inform designers of potential failure risks that arise from interacting failure mechanisms in the context of operating conditions for a given application. To demonstrate the impact of enabling design for reliability (DfR) while accounting for multistress scenarios, this study has combined experimental and EDA efforts to examine a wire-bonded multichip power module (MCPM) architecture. Coupled EM and thermomechanical stressing experiments on aluminum wire bonds have been leveraged to integrate a multistress model into the PowerSynth 2 EDA workflow to emphasize the extended lifetimes that can be achieved through optimization for thermomechanical and electrical stress reduction. PowerSynth 2 is a 2D/2.5D/3-D MCPM layout optimization tool that can perform electro-thermal optimization to get a Pareto-optimal solution set using fast, accurate, hardware-validated models [10, 12]. The traditional 2D power module generally only uses a single substrate, such as direct bond copper (DBC) to support multiple devices connected horizontally using traces. The latest breakthroughs in 3D modules are power modules that use multiple

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device or substrate layers that are stacked and connected vertically [12]. For these high-power density MCPM designs, EM-aware reliability optimization is essential for critical missions. Therefore, an EM-aware layout optimization methodology has been incorporated into the physical design automation tool, PowerSynth 2.

MOTIVATION

Prior works have demonstrated that the development of novel accelerated testing methods for addressing specific failure mechanisms can decrease testing times while still delivering lifetime prediction accuracy [13-16]. Therefore, well-designed accelerated testing processes and results can be leveraged for reliability estimation. As WBG materials enable increases in power density, the potential for interaction between multiple failure mechanisms increases, which can significantly reduce electronics packaging lifetime. For instance, elevated operating temperatures and high current densities can work to reduce the lifetime of interconnect technologies. Previous work has demonstrated that solder interconnections show a reduced lifetime when the interacting failure mechanisms of mechanical stress and EM are present [17]. While traditional models for handling EM, such as Black's equation, have been used with relative success to determine the risks of device failure, the extreme conditions of present-day applications demand a more comprehensive multistress model that better captures the physics of combined failure [18]. The focus of this article is to demonstrate the coordination of multistress accelerated testing experiments and EDA reliability estimations in a DfR tool to reduce the impact of interacting stresses likely found in high-density power electronic packaging through the development of optimization routines.

DEMONSTRATION OF COMBINED STRESS TESTING METHOD

The ability to accurately characterize physical inputs in operation by the DfR tool integrated with rapid thermomechanical predictions provides a fantastic platform for enabling DfR optimization; however, unfortunately, most existing models treat reliability stress factors as "individual-actors," such as humidity, that do not participate in failure mechanisms that are not directly assessed against that factor. This approach leaves electronic applications subject to unforeseen failures where combined interactions capitulate premature failure in service.

To illustrate this principle, a coupled experimental and computational modeling demonstration of the combined risk of EM with thermomechanical interactions in a wire-bonded MCPM has been conducted. Since the electromigratory atomic flux itself represents a response to an internal, current-driven force, the impacts of external forces can amplify or augment the diffusive behavior, as strain and creep behaviors are coupled with EM damage. In this combo-stress and design optimization demo, coupled mechanical-EM stress-induced failure was assessed via test vehicle resistance nets driven at high current density at elevated temperature, in combination with varying mechanical stress applications. The mean time to failure (MTTF) was determined under current density, temperature, and stress conditions, using a custom accelerated test mechanism, identifying a relationship between EM stressors and externally applied mechanical loads. In concert, computational finite element modeling (FEM) activities provided context to extract localized driving stresses under complex accelerating factors in the experimental

electro-thermal system. Ultimately, these experiments elucidated layout-relevant mechanical and electro-thermal parameterized lifetime predictions for implementing in module design development, for enhanced DfR as a function of anticipated operation schemes, or mission profiles.

The experimental testing mechanism was designed to control the pitch between two, wire-bonded, DBC cards and consists of a set of machined aluminum fixtures and high-temperature micrometer translation stage which are all housed inside of a convection laboratory oven. Using this mechanism allows for the combination of temperature, current density, and mechanical stress to be imposed upon a wire bond. The wire bonds used here were 5 [mil] Heraeus ALW-49C, a 99.99% aluminum composition. The basic idea behind this method is shown in Fig. 1. As described previously, the MTTF was determined by monitoring the change in resistance of the wire bond over time, and the associated stress factors for each experimental run were characterized using the experimental conditions and electro-thermal FEM simulation results. In this set of experiments, a failure of a bond was considered to be an electrical resistance increase of 10% across a given wire, which is usually an indicator that component maintenance or replacement is necessary for maintaining expected performance.

Experimental life testing of wire bonds under constant ambient temperature and current density (100°C and $23,684\text{ A/cm}^2$) with varied mechanical stresses yielded the relationship observed in Fig. 2. This plot demonstrates a negative relationship between the time to 10% increase in wire bond resistance, meaning that as the mechanical stress level was increased, a reduction in lifetime was observed. The data scatter associated with Fig. 2 is being attributed mainly to the fact that there is some variability between the lengths of each tested bond, which in turn would have a slight impact on the maximum temperature that the bond was reaching due to joule heating. The solid line in Fig. 2 corresponds to an exponential fit to the data (see MTTF equation in Fig. 3), with the dashed lines corresponding to the 95% confidence interval of the fit [18]. These accelerated test results complement the assumption of combined stressing impacting lifetime in future devices. Based on these experiments, it is clear that considering both the electrical and thermomechanical stresses in reliability evaluation will more accurately estimate the lifetime of a wire bond, therefore requiring that optimization be done to reduce the impact of both stresses on interconnect lifetime. Certainly, increasing the diameter of bond wires will help to mitigate the effects of EM by reducing the effective current density, but increased bond wire sizes may prove to be difficult to integrate into increasingly smaller components. These results have been integrated into the optimization routines described in the following section.

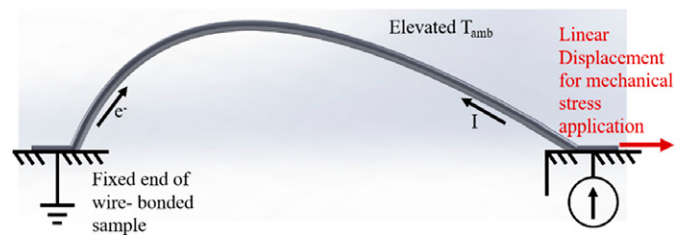


Fig. 1. Experimental accelerated testing diagram depicting a wire bond sample being stretched linearly in an elevated temperature environment while also experiencing the effects of an applied current density.

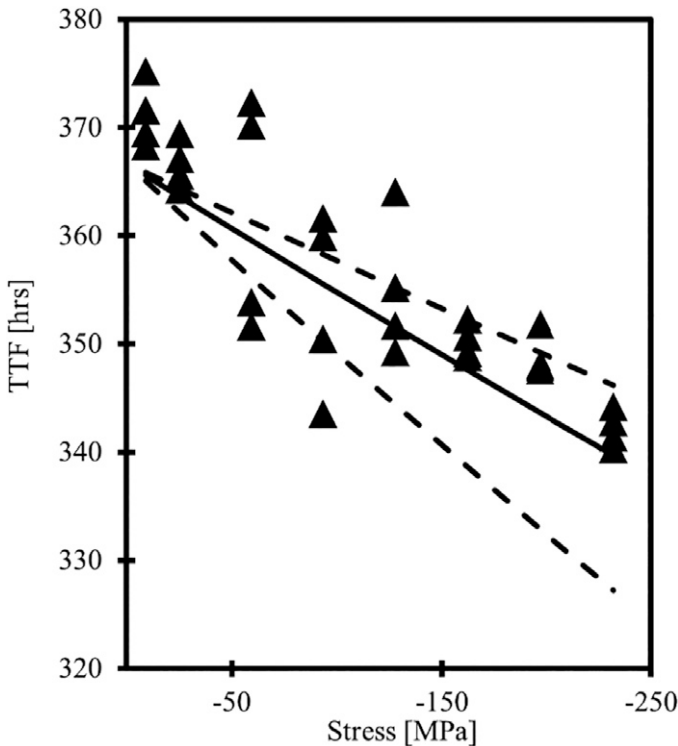


Fig. 2. Plot of wire bond multistress experimental results demonstrating a negative relationship between time to 10% increase in wire bond resistance and FEM simulated compressive stress state in wire bond samples.

DATA-DRIVEN ELECTRONIC DESIGN AUTOMATION WITH DESIGN-FOR-RELIABILITY OPTIMIZATIONS

Experimental accelerated tests can be used to add functionality to DfR tools, such as PowerSynth 2. A high-level workflow for reliability-aware MCPM layout optimization is shown in Fig. 3.

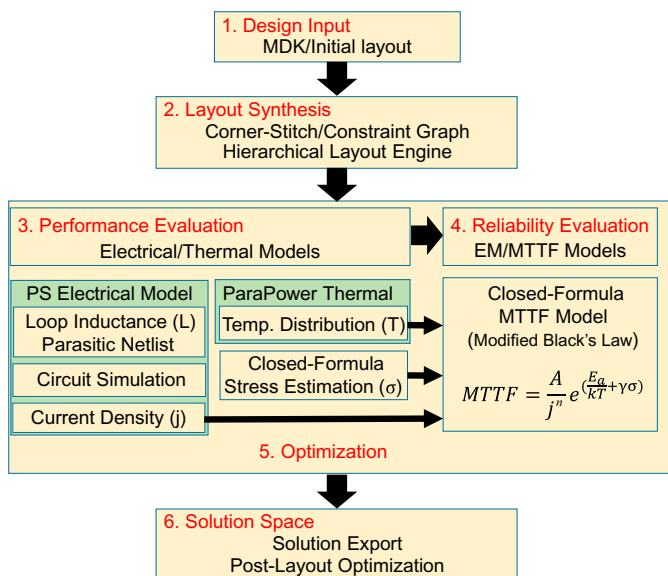


Fig. 3. Design for reliability tool workflow depicting the integration of experimental models for interacting stress mechanisms into the optimization routine (MTTF model from [18]).

PowerSynth 2 takes the user-generated initial layout (and associated layer stack), design constraints, and current-voltage ratings. The manufacturer design kit is a built-in function and contains the components and material library, which, through an interactive interface, can be edited by a user. Using constraint graph evaluation methodology, the layout engine synthesizes layouts using a hierarchical corner-stitching data structure [10].

For electrical, thermal, and mechanical reliability optimization, PowerSynth 2 provides built-in support from two aspects: design constraints and reliability modeling. Design constraints analyze both the voltage difference between any two insulated conductors and the current passing through any traces. Layout scaling on dielectric spacing and conductor width will be automatically performed to ensure dielectric E-field and conducting current are within limits. Reliability modeling, on the other hand, focuses on evaluating design solutions for stress, thermal transient, and EM impact on lifetime. The modeling result is included as a part of the cost function so that the multiobjective optimization will consider balancing different metrics when producing the final Pareto-Front.

In this study, EM impact is considered through the data-driven equations based on the experimental measurement. A built-in PowerSynth 2 partial element equivalent circuit based electrical model has been used for electrical parasitic extraction [19]. This model can provide power loop parasitics (resistance and inductance) and a distributed netlist for the layout solutions. The netlist is used for simulation, which provides the current through each device. Then, the current density for each wire bond is calculated by considering an even distribution of the current through all wire bonds connected to each device.

In addition, the ParaPower thermal model is used to simulate the temperature distribution [20]. Since ParaPower cannot represent a rounded wire-like structure, the detailed temperature distribution for the wire bonds cannot be extracted. To address this limitation, we consider the best and worst case of the bond wire lifetime expectation. Since the EM impacts are exponentially dependent on the temperature, extracting temperature variation on the bonding wire is critical for accurate analysis. For 2D layout, the devices are the hot spots on the layout, while traces are much cooler. Since most bonding wires connect between device pads and traces, we use the device temperature for worse-case analysis while using the trace temperature for the best case.

For stress-aware EM modeling, wire bond stress is evaluated using the equation derived from Young's modulus (E) and thermal expansion (α) difference based on the temperature gradient. Finally, stress-modified Black's equation is used to calculate the normalized MTTF for the interconnect [18]. Though the finite element analysis methods are capable of evaluating all the parameters required for MTTF estimation, the optimization algorithm cannot directly use their results as they significantly increase the runtime. Therefore, a fast and accurate model is required to be used in the optimization loop and compute reliability metric for different layout solutions. Based on the experiment measurement data, the following values are used in this work: $A = 9.57$, $N = 1.83$, $E_a = 0.85$, and $\gamma = 0.000445$. Since the reliability values are highly case-dependent, all MTTF metrics are normalized relative to the worst MTTF design case (defined as 1) [18]. With the above-mentioned models, PowerSynth

2 can optimize the MCPM layouts for reliability associated with EM. From the optimization solution space, a user-chosen solution can be selected and post-layout optimization can be completed for the next design iteration(s).

In this work, to demonstrate the reliability optimization feature in PowerSynth 2, power loop inductance and a quantitative reliability metric (10% increase of wire resistance) based on the experimental testing criterion are used. Based on the proposed methodology and experimental results, a 2D half-bridge module layout is optimized as an example of the DfR optimization considering the multiphysics interaction among various failure mechanisms. Seven various floorplan sizes were chosen for optimization, where 150 solutions were generated and evaluated for each size at a runtime of roughly 5.86 s per layout solution.

To include the measurement results into the DfR EDA workflow, the experimental wire bond dataset has been fit to the modified Black's equation for EM failure with the addition of a term to incorporate the application of mechanical stress [18]. Note that the constant A in the equation will affect the lifetime

expectancy of each individual design, but does not alter its relative performance among all generated layouts. The complete solution space and three selected solutions are shown in Fig. 4. As a reliability constraint, a minimum relative MTTF of four is considered to be the threshold for reliability, highlighted as a gray dotted line in Fig. 4, representing a 4X improvement in lifetime. A Pareto-Front is drawn on the solution space. Three solutions have been selected on the front to exhibit the variation between simulated layouts. Between the best and worst-case results, there is about a 20% difference in the expected lifetime due to temperature variation across the bonding wire. Based on the Pareto-Front layouts, Layout A clearly has the best reliability as it has a larger footprint as well as a smaller temperature rise and stress. However, the loop inductance of this layout is higher compared with the other two solutions. Conversely, Layout C displays the lowest loop inductance but with the lowest reliability. Since this layout has the smallest footprint size, it has the largest temperature rise, making it less reliable for operation. Among all three layouts, Layout B has the most optimized-yet-balanced metric values for both

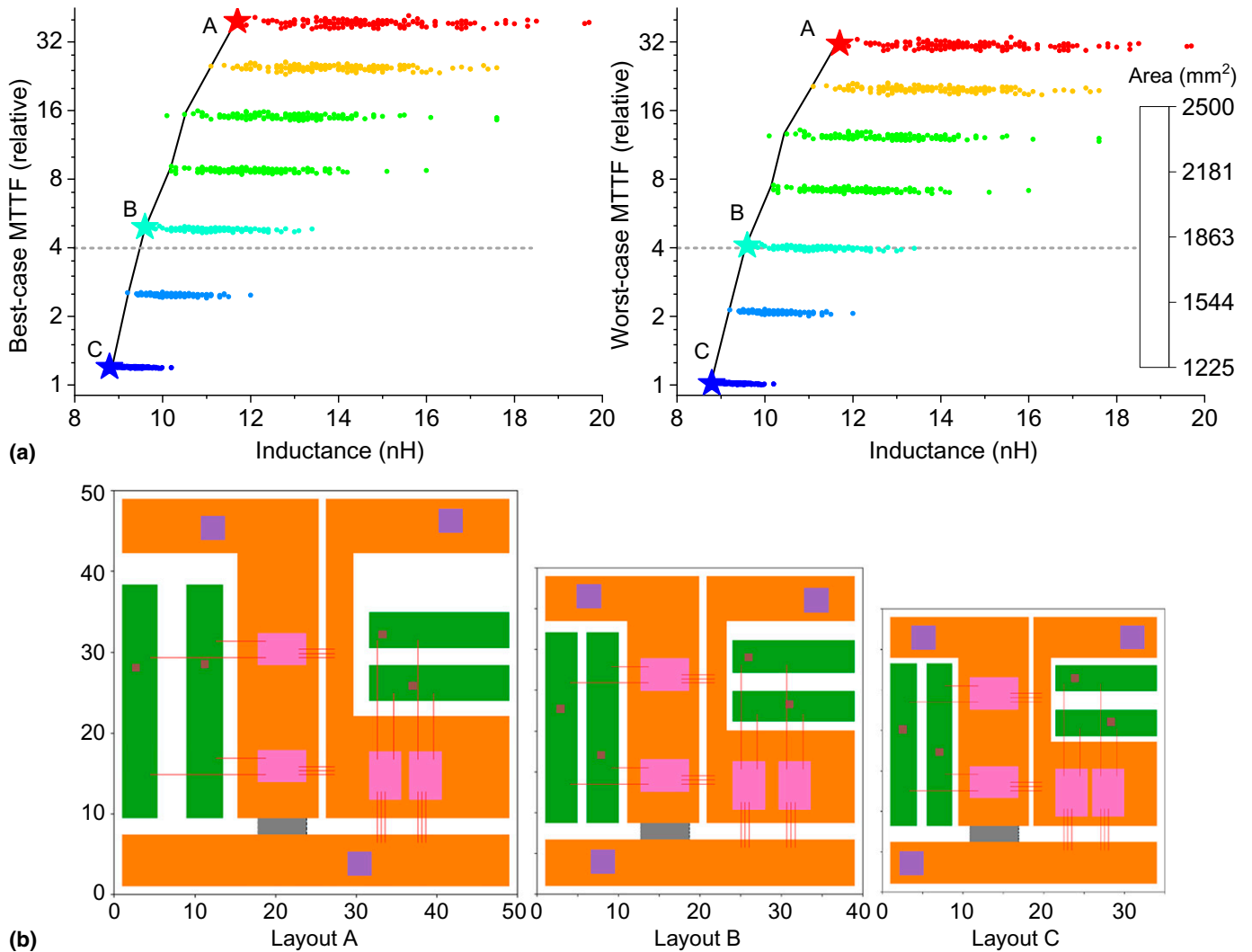


Fig. 4. (a) Optimization solution space with best-case and worst-case analysis results. (b) Three layouts selected from the Pareto-Front, demonstrating the tradeoff in multiobjective optimization.

objectives. It satisfies the threshold criteria for reliability and has a low loop inductance. Therefore, Layout B is selected as the performant-yet-reliable design by PowerSynth 2 DfR.

CONCLUSIONS AND FUTURE OUTLOOK

Designing next-generation power electronics will require the development of multimechanism failure analysis datasets that more accurately predict lifetimes compared with single failure mechanisms used today. This work demonstrates a DfR methodology which, with appropriate data and integration into an EDA space, can be applied to many different application spaces. As multistress scenarios become better understood, reliability estimates for new devices will follow suit. From this effort, it has been shown that the incorporation of multistress experimental results on wire-bonded interconnects into an EDA environment can assist in the optimization of a designed layout. This effort complements the EM-aware optimization flow with solder bump interconnects demonstrated in [21]. In this work, the effective coordination between accelerated testing and EDA efforts has demonstrated a successful optimization approach for a wire-bonded 2D module layout combining failure mechanisms of EM and mechanical loading. The PowerSynth 2 platform has been put forward as a DfR tool for performing a rapid relative reliability study which can be adapted to incorporate multistress scenarios. It can optimize device location and trace routing, considering the reliability metrics desired by the user of the tool. The stress estimation method used in this study is preliminary and experimental and needs improvement for achieving higher accuracy. Further development of statistically derived reliability models based on experimental efforts will also prove to be useful on this front, as they have the potential to surpass the simplicity of raw data sets in terms of rapid lifetime assessment and optimization.

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