

Factoring Interacting Stress Mechanisms in Design for Reliability of Extreme Environment Power Modules

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Abstract

As power densification demands are placing electronic packages under greater reliability risk, the consequence of complementary or interacting stresses in producing failure are becoming increasingly significant. As such, it is important that reliability methods and package designs consider how multiple-stress interactions may impact product life. Here, the coordination between a novel accelerated testing method and electronic design automation efforts has demonstrated a successful optimization approach for a wire-bonded 2D module layout combining failure mechanisms of electromigration and mechanical stressing. Utilizing custom, physics-of-failure approaches in accelerated testing, interactions can be observed in failure acceleration, which then can be incorporated into design for reliability (DfR) optimization tools. The PowerSynth 2 platform has been utilized as a design for reliability tool to perform a rapid relative reliability evaluation incorporating multi-stress scenarios. This work demonstrates the value added to reliability evaluation techniques when accounting for interacting failure mechanisms and suggests that next generation power devices consider these effects in lifetime estimation.

Key words

Accelerated testing, Design automation, Design for reliability, Interacting failure mechanisms, Layout optimization, Power electronics

I. Introduction

Device and packaging reliability remains a significant element of delivering robust, power dense electronics, especially where wide bandgap (WBG) semiconductor technologies enable higher operating temperatures and voltages. Issues like thermomechanical stress, materials degradation, and diffusive mobility driven voiding are not trivial, and complexities of variegated failure mechanisms lead to difficulty in identifying accurate lifetimes. With electrification needs anticipated to exceed $1\text{kW}/\text{cm}^2$ and operating temperatures $>200^\circ\text{C}$, module packaging technology and materials impede reliable operation for mission critical systems, particularly in the form of interconnect reliability. Highly transient power needs arising from pulsed and continuous duty energized systems or rapidly changing traction demands in electrified vehicles introduce high intermittent temperatures as well as thermomechanical stresses that accumulate damage in interconnects – all concurrent with high current density operation and vibrational stresses that also reduce operating lifetimes. These coupled and interacting failure risks must be

identified early in the design cycle to ensure robust operation, for which reliability life prediction could ideally be integrated into electronic design automation (EDA), so as to produce reliability-optimized, power dense systems.

With WBG device current capabilities soaring to hundreds of amps, temperatures arising from conduction and switching losses are lowering packaging lifetimes, with interconnect metallurgies subjected to extreme current, temperature and thermomechanical stresses that lead to reliability failure mechanisms such as electromigration (EM) [1], [2]. At its core, EM is a combinatorial failure mode that appears under the combined influence of high temperature enabled diffusivity and electromotive metal ion migration caused by high current density [3]-[5]. Yet even beyond this, coupled thermomechanical risk and other failure driving factors like humidity or strain accelerated failure can overlap in system design, leading to premature failures that would be undetected by uni-dimensional accelerated stress testing, typical of those performed in standards-based qualifications. Several instances of overlapping accelerating stress factors have been noted in literature, where thermal cycling (TC)

and vibrations, humidity and TC, or voltage and temperature interact to promote accelerated failure [6]-[11]. For example, EM-induced voids further amplify risk from thermal cycling stress with weakened interconnections, so that when considering high current and temperature WBG device interconnects, layout and thermal schemes ought to be evaluated together. Unfortunately, these compounded reliability driving factors cannot be easily assessed in common accelerated testing, nor can they be captured using simple design rules.

Ideally, electrical, thermal, and mechanical design co-optimization need to identify and inform designers of potential failure risks that arise from interacting failure mechanisms in the context of operating conditions for a given application. To demonstrate the impact of enabling design for reliability (DfR) while accounting for multi-stress scenarios, this study has combined experimental and EDA efforts to examine a wire-bonded multi-chip power module (MCPM) architecture. Coupled EM and thermomechanical stressing experiments on aluminum wire bonds have been leveraged to integrate a multi-stress model into the PowerSynth 2 EDA workflow to emphasize the extended lifetimes which can be achieved through optimization for thermomechanical and electrical stress reduction. PowerSynth 2 is a 2D/2.5D/3D multi-chip power module (MCPM) layout optimization tool that can perform electro-thermal optimization to get a Pareto-optimal solution set using fast, accurate, hardware-validated models [10]. For high power density MCPM designs, electromigration-aware reliability optimization is essential. Therefore, an EM-aware layout optimization methodology has been incorporated into the physical design automation tool, PowerSynth 2.

II. Motivation

Prior works have demonstrated that the development of novel accelerated testing methods for addressing specific failure mechanisms can decrease testing times while still delivering lifetime prediction accuracy [12]-[15]. Therefore, well-designed accelerated testing processes and results can be leveraged for reliability estimation. As WBG materials enable increases in power density, the potential for interaction between multiple failure mechanisms increases, which can significantly reduce electronics packaging lifetime. For instance, elevated operating temperatures and high current densities can work to reduce the lifetime of interconnect technologies. Previous work has demonstrated that solder interconnections show a reduced lifetime when the interacting failure mechanisms of mechanical stress and EM are present [16]. While traditional models for handling EM, such as Black's Equation, have been used with relative success to determine the risks of device failure, the extreme conditions of present-day applications demand a more comprehensive multi-stress model that better captures the

physics of combined failure [17]. The focus of this article is to demonstrate the coordination of multi-stress accelerated testing experiments and EDA reliability estimations in a DfR tool to reduce the impact of interacting stresses likely found in high density power electronic packaging through the development of optimization routines.

III. Demonstration of Combined Stress Testing Method

The ability to accurately characterize physical inputs in operation by the DfR tool integrated with rapid thermomechanical predictions provides a fantastic platform for enabling design-for-reliability optimization; however, unfortunately, most existing models treat reliability stress factors as "individual-actors," such as humidity, that do not participate in failure mechanisms that are not directly assessed against that factor. This approach leaves electronic applications subject to unforeseen failures where combined interactions capitulate premature failure in service.

To illustrate this principle, a coupled experimental and computational modeling demonstration of the combined risk of EM with thermomechanical interactions in a wire-bonded MCPM has been conducted. Since the electromigratory atomic flux itself represents a response to an internal, current driven force, the impacts of external forces can amplify or augment the diffusive behavior, as strain and creep behaviors are coupled with electromigration damage. In this combined stress and design optimization demo, coupled mechanical-EM stress induced failure was assessed via test vehicle resistance nets driven at high current density at elevated temperature, in combination with varying mechanical stress applications. The mean time to failure (MTTF) was determined under current density, temperature, and stress conditions, using a custom accelerated test mechanism, identifying a relationship between EM stressors and externally applied mechanical loads. In concert, computational finite element modeling (FEM) activities provided context to extract localized driving stresses under complex accelerating factors in the experimental electro-thermal system. Ultimately, these experiments elucidated layout-relevant mechanical and electro-thermal parameterized lifetime predictions for implementing in module design development, for enhanced DfR as a function of anticipated operation schemes, or mission profiles.

The experimental testing mechanism was designed to control the pitch between two, wire-bonded, DBC cards and consists of a set of machined aluminum fixtures and high-temperature micrometer translation stage which are all housed inside of a convection lab oven. Using this mechanism allows for the combination of temperature, current density, and mechanical stress to be imposed upon a wire bond. The basic idea behind this method is shown in Fig. 1. As described previously, the MTTF was determined

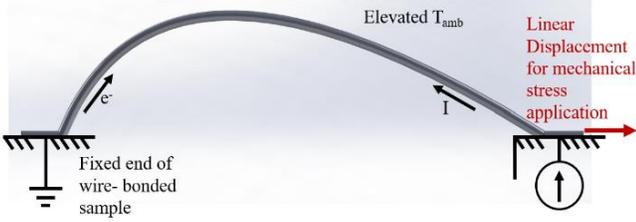


Fig. 1. Experimental accelerated testing diagram depicting a wire bond sample being stretched linearly in an elevated temperature environment while also experiencing the effects of an applied current density.

by monitoring the change in resistance of the wire bond over time, and the associated stress factors for each experimental run were characterized using the experimental conditions and electro-thermal FEM simulation results. In this set of experiments, a failure of a bond was considered to be an increase in electrical resistance of 10% across the wire bond.

Experimental life testing of wire bonds under constant current density and temperature with varied mechanical stresses yielded the relationship observed in Fig. 2. This plot demonstrates a negative relationship between the time to 10% increase in wire bond resistance, meaning that as mechanical stress level was increased, a reduction in lifetime was observed. These accelerated test results complement the assumption of combined stressing impacting lifetime in future devices. Based on these experiments, it is clear that considering both the electrical and thermomechanical stresses in reliability evaluation will more accurately estimate the lifetime of a wire bond, therefore requiring that optimization be done to reduce the impact of both stresses on interconnect lifetime. These results have been integrated into the optimization routines described in the following section.

IV. Utilizing Interacting Stress Factors for Reliability-Aware EDA

Experimental accelerated tests can be used to add functionality to DfR tools, such as PowerSynth 2. A high-level workflow for reliability-aware MCPM layout optimization is shown in Fig. 3. PowerSynth 2 takes the initial layout from the user along with layer stack, design constraints, and current-voltage ratings. The built-in manufacturer design kit (MDK) contains the material and component library, which is editable by the user through an interactive interface. The constraint-aware layout engine synthesizes layouts using a hierarchical corner-stitching data structure with constraint graph evaluation methodology [10]. For reliability optimization, the solutions are evaluated using electrical, thermal, and reliability models.

In this study, the PowerSynth 2 built-in partial element equivalent circuit (PEEC) based electrical model has been used for electrical parasitic extraction [18]. This model can provide power loop parasitics (resistance, inductance) and a

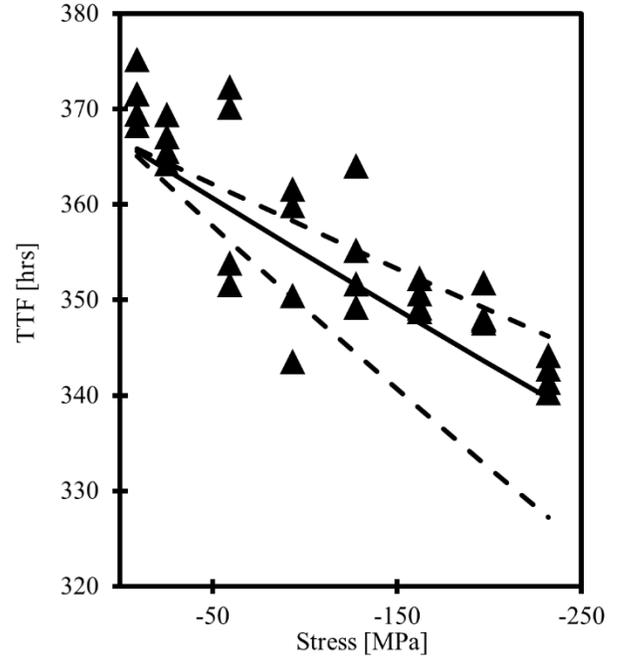


Fig. 2. Plot of wire bond multi-stress experimental results demonstrating a negative relationship between time to 10% increase in wire bond resistance and FEM simulated compressive stress state in wire bond samples.

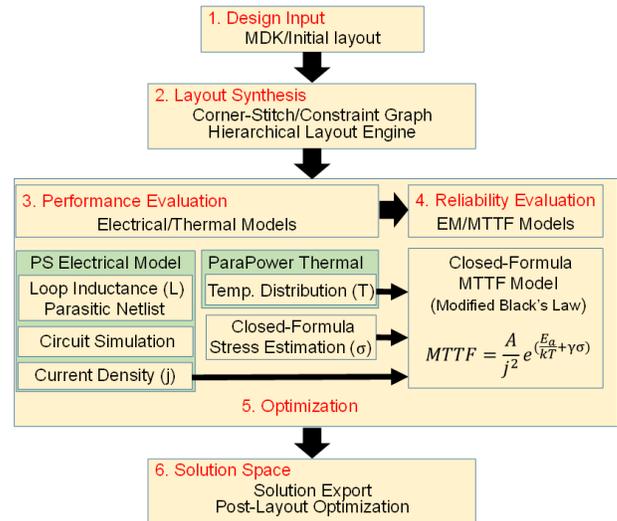


Fig. 3. Design for Reliability tool workflow depicting the integration of experimental models for interacting stress mechanisms into the optimization routine (MTTF model from [17]).

distributed netlist for the layout solutions. The netlist is used for simulation, which provides the current through each device. Then, the current density for each wire bond is calculated by considering an even distribution of the current through all wire bonds connected to each device. The ParaPower thermal model is used to get the temperature

distribution [19]. Since ParaPower cannot represent a wire bond, the temperature distribution for the wire bonds cannot be extracted. Therefore, the device temperature is used for wire bond temperature estimation. ParaPower has a stress evaluation feature, which can estimate for the devices only. Therefore, in PowerSynth 2, wire bond stress is evaluated using the equation derived from Young’s modulus (E) and thermal expansion (α) difference based on the temperature gradient. Finally, the current density (j), temperature (T), stress (σ) are fit to the experimental dataset and stress-modified Black’s Equation to calculate the normalized MTTF for the interconnects [17]. Though the finite element analysis (FEA) methods are capable of evaluating all the parameters required for MTTF estimation, these methods cannot be used in the optimization loop due to their long runtime. Therefore, a fast modeling approach is considered that can be used in the optimization loop and give a relative reliability metric for different layout solutions. With the above-mentioned models, PowerSynth 2 can optimize the MCPM layouts for reliability associated with the electromigration. From the optimization solution space, the user can choose the satisfactory solution and perform post-layout optimization for the next design iteration(s).

In this work, to demonstrate the reliability optimization feature in PowerSynth 2, power loop inductance and a quantitative reliability metric (10% increase of wire resistance), based on the experimental testing criterion, have been used. Using the proposed methodology and experimental results, a 2D half-bridge module layout is optimized as an example of the multi-stress optimization activities which can be done to address the interaction between failure mechanisms. Seven various floorplan sizes were chosen for optimization, where 150 solutions are generated and evaluated for each size at a runtime of roughly 5.86s per layout solution. The complete solution space and three selected solutions are shown in Fig. 4. To enable the inclusion of the experimental results into the DfR tool workflow, the experimental wire bond dataset has been fit to the modified Black’s equation for EM failure with the addition of a term to incorporate the application of mechanical stress [17]. While evaluating the reliability metric, the constant A , as typically seen in Black’s equation for EM, is ignored as the values are normalized for relative comparisons. From these values, 3.5 is considered to be the threshold for reliability (highlighted as a red dotted line in Fig. 4). A Pareto-front is drawn on the solution space (the black line winding along the left portion of Fig. 4), and three solutions are chosen on the front to demonstrate the layout variation. From the layouts, it is clear that layout A has the highest reliability as it has a larger footprint as well as a smaller temperature rise and stress. However, the loop inductance of this layout is higher compared to the other two solutions. On the other hand, layout C has the lowest loop inductance with the lowest reliability. Since this layout has the smallest footprint size, it has the largest temperature rise,

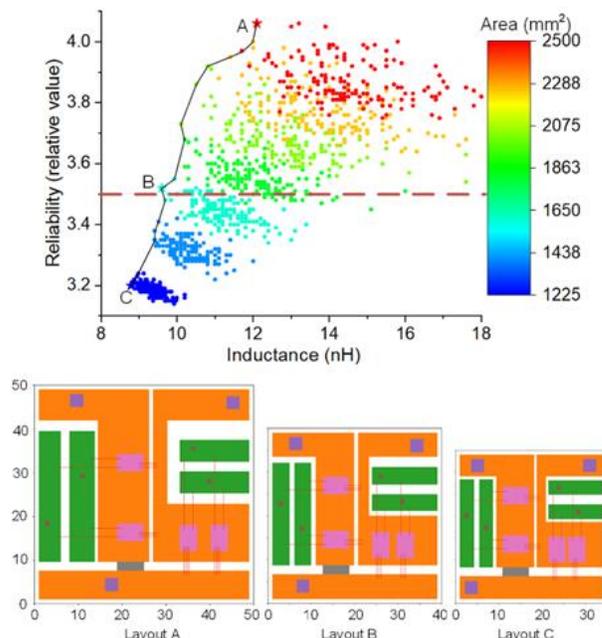


Fig. 4. Optimization solution space (top) with three selected layouts, where layouts A, B, & C (bottom) correspond to their respective labels on the Pareto-front of the solution space.

making it less reliable for operation. Among all three layouts, layout B has the most optimized-yet-balanced metric values for both objectives. It satisfies the threshold criteria for reliability and has a low loop inductance. So, layout B is selected as the reliability-optimized design in PowerSynth 2.

V. Conclusions and Future Outlook

Designing next-generation power electronics will require the development of multi-mechanism failure analysis datasets which more accurately predict lifetimes compared to single failure mechanisms used today. As multi-stress scenarios become better understood, reliability estimates for new devices will follow suit. From this effort, it has been shown that incorporation of multi-stress experimental results on wire-bonded interconnects into an EDA environment can assist in the optimization of a designed layout. This effort complements the EM-aware optimization flow with solder bump interconnects demonstrated in [20]. In this work, the effective coordination between accelerated testing and EDA efforts has demonstrated a successful optimization approach for a wire-bonded 2D module layout combining failure mechanisms of EM and mechanical loading. The PowerSynth 2 platform has been put forward as a DfR tool for performing a rapid relative reliability study which can be adapted to incorporate multi-stress scenarios. It can optimize the placement of the devices and routing of the traces, considering the reliability metrics desired by the user of the tool. The stress estimation method used in this study is

preliminary and experimental and needs improvement for achieving higher accuracy. Further development of statistically derived reliability models based on experimental efforts will also prove to be useful on this front, as they have the potential to surpass the simplicity of raw data sets in terms of rapid lifetime assessment and optimization.

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