Electromigration-Aware Reliability Optimization of MCPM Layouts Using PowerSynth

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***Abstract*—Modern power electronics are experiencing significant demand for ultra-high-power density in the grid, data center, automotive industries, and aerospace applications. To satisfy the increasing demand, innovative packaging technologies for multi-chip power modules (MCPMs) are proposed by leveraging the advantages from wide bandgap (WBG) devices (i.e., SiC, GaN). Since higher density modules are more vulnerable to electromigration (EM) risk, the MCPM layout optimization requires EM consideration along with electro-thermal aspects. In this paper, an EM-aware reliability optimization methodology is proposed and implemented in PowerSynth. Mean time to failure (MTTF) is used as the reliability metric for EM risk assessment. MTTF estimation needs a detailed current density and temperature distribution in a relatively fast method that can be used in an optimization loop. Our approach has shown 1,100 times speedup in current density extraction compared to the FEM simulation. MCPM with wire bonding and solder bump arrays are optimized using the proposed workflow. Experimental results are used to predict MTTF for wire-bonded module case.**

***Keywords*—ElectroMigration (EM), PowerSynth 2, Reliability Optimization, Layout Optimization**

I. Introduction

Recent movement toward a more-electric world is pushing the power-density requirements daily. To avail the full advantage of the WBG devices, more compact MCPM packages are proposed by the researchers [1]. Benefiting from the WBG devices, power density can be improved but maintaining reliable performance becomes challenging. Among different parts of the module, interconnects (i.e., wire bonds, solder bumps) are more prone to failure due to electro-thermo-mechanical stress as the switching frequency and power levels increase [2]. Among different failure mechanisms, EM is one of the prevalent ones, especially at high-current density. EM is a material migration based on the flow of current through it, which is a diffusion-controlled process. Though high current density drives the migration process, high temperature also plays an important role in increasing the diffusion rate. Therefore, the combination of high current density and high temperature in the interconnect/solder material can cause very severe EM-induced failures that can affect the long-term reliability of the component.

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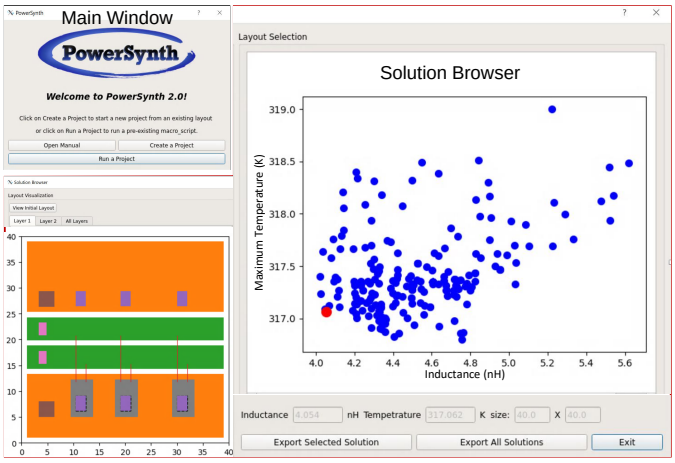

Fig. 1. PowerSynth 2 graphical user interface

EM is a well-known issue in industries like high-frequency integrated circuits (HFIC), ultra/very-large-scale ICs (U/VLSI), communication appliances, etc [3]. Since these applications include very high-frequency operations, the EM-model should be capable of capturing both DC and high-frequency AC current density impacts properly. Researchers have tried to predict the mean time to failure (MTTF) due to EM for different types of interconnects through finite element analysis (FEA) and experimental testing. Though flip-chip modules [4, 5] with SiC and GaN devices are very recent attractions to the power electronics due to their low parasitics, this technology has been widely used in U/VLSI for a while. In [6], authors have studied the combined effect of high current and high temperature on Ag, Cu, and Au wire bonds through experiments. Authors of [7] performed an electrical-thermal-mechanical coupled analysis of electromigration in a bonding wire of a power module. A test method is developed for studying the current effect on the aging process of a wire-bonded Silicon Carbide (SiC) MOSFET module under a power cycling test in [8]. The experimental and analysis results showed that different current densities have different impacts on both the bond wire resistance and die-attach solder layer. This methodology is also an experimental case study whose results can be used in validating the modeling effort for EM risk assessment. In [9], authors have tried to optimize the packaging structure of a flip-chip device by studying a few variations in solder material, solder bump diameter as well as

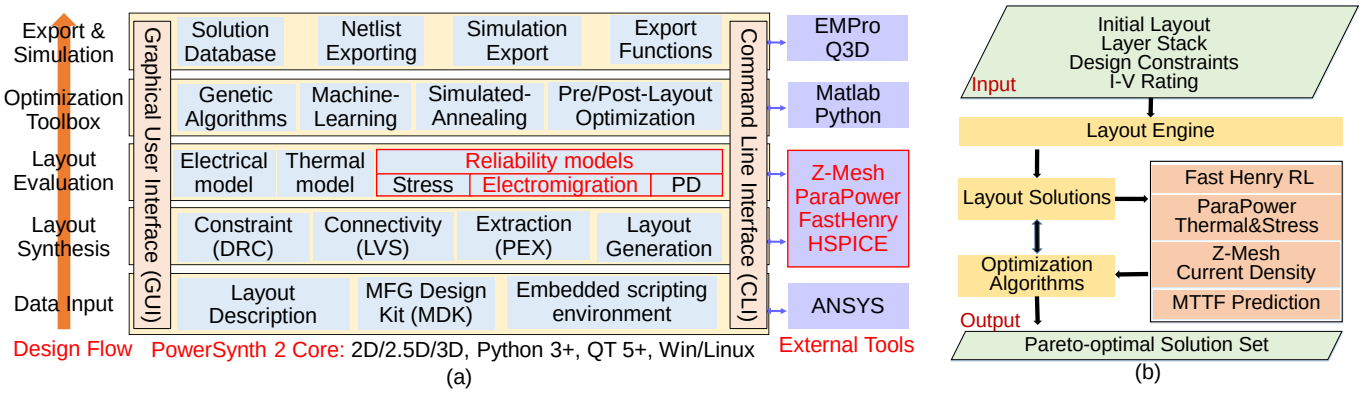

Fig. 2. (a) PowerSynth 2 architecture, (b) EM-aware reliability optimization workflow

pitch, and the drain connector geometry. All these variations are manually designed by the authors, and the module layout variation impact has not been studied. Therefore, the solution space is limited. Authors have studied a few solder bump distribution orientations in [10] to optimize the electromigration reliability by applying a more balanced current distribution among solder bumps. This trial is also a manual one and is limited by the designer's choice.

All of the above-mentioned efforts are manual and case-specific studies. The commercial CAD tools can be used for EM modeling without any intellectual optimization capability. PowerSynth [11] has been proven to be efficient in electro-thermal optimization of 2D/2.5D MCPM layouts. PowerSynth-guided reliability optimization flow has been reported in [12], where both the layer stack and the layout are optimized simultaneously considering phase change material (PCM). However, the reliability optimization objective in that work was to reduce the stress due to thermal cycling. PowerSynth 2 [13] has demonstrated the capability of handling state-of-the-art interconnect packaging technologies like wire bonds and solder bumps with 2D/2.5D/3D high-density module designs. The latest updates of the tool have enabled EM-aware electro-thermal optimization study. The graphical user interface (GUI) of PowerSynth 2 is shown in Fig. 1.

In this work, our contribution includes: 1. Capturing detailed and accurate current density distribution at both DC and AC through our in-house tool called Z-Mesh; 2. Developing a generic EM-associated risk assessment workflow; 3. Demonstrating the effectiveness of the flow through case studies of both wire bonding and solder bump technology; 4. Performing EM-aware electro-thermal performance optimization using PowerSynth 2. For MTTF evaluation, the well-known Black's law has been considered in this version, which can be replaced easily with other empirical or analytical models from different research groups. The rest of the paper is organized as follows: Section II describes an overview of the PowerSynth reliability optimization workflow. Section III presents the methodology and a brief description of associated design tools. The reliability optimization results for modules with a 2D array of bumps (flip-chip module [4]), and wire bonds with accelerated EM testing are demonstrated in Section IV. The testing results are used to evaluate the failure time of wire bonds of a half-bridge module. Finally, Section V concludes the paper with a plan for future work.

II. PowerSynth 2 Architecture

PowerSynth 2 architecture is shown in Fig. 2(a), which has two fundamental parts: 1. A core engine with the built-in algorithms, methodologies, and modeling techniques; 2. External tools linked through application programming interfaces (APIs). Moreover, both GUI and command-line interfaces are implemented to support both Windows and Linux compatibility. A brief description of the architecture is provided below.

A. Design Input and Layout Engine

PowerSynth 2 requires the technology specification that contains information on the layer stack, power devices, substrates, connectors, wire bonds, and vias. The built-in manufacturer design kit (MDK) contains a library of materials and necessary design constraints for manufacturing the module. MDK library can be modified through the interactive interface. The initial layout is taken through a hierarchical geometry description script. PowerSynth 2 supports both solder bump arrays and wire bond groups connectivity, which was impossible with PowerSynth v1.x. The EM-aware optimization flow requires a current-voltage rating of the operating condition for current-density distribution extraction, and thermal boundary conditions like ambient temperature and heat transfer coefficient.

A constraint-aware, hierarchical layout engine has been developed to generate design rule check (DRC) clean solutions that are manufacturable. The initial layout is stored as a tree of horizontal and vertical corner-stitched planes. For each node in the tree, two constraint graphs are created. Horizontal constraint graphs (HCGs), and vertical constraint graphs (VCGs) ensure horizontal and vertical relative locations, respectively. Hierarchical constraint propagation methodology [13] ensures minimum room for child nodes in the corresponding parent node. These constraint graphs are used to generate solution layouts by randomizing the edge weights. The randomization

methodology is dependent on the mode of layout generation. PowerSynth layout engine has three modes of operation: Minimum-sized, variable-sized, and fixed-sized. The minimum-sized solution demonstrates the maximum possible power density. Variable floorplan-sized solution generation mode can be used to pick an optimized floorplan size. Once the floorplan size is decided, the fixed-sized solution generation mode can be used to further optimize the placement and routing of the components within the fixed dimensions.

B. Design Models and Layout Evaluation

Electrical parasitics and thermal optimization are essential for the reliable operation of the WBG power modules. Moving from 2D toward 3D MCPM layouts, the parasitic loop inductance can be reduced significantly. However, as the 3D layout solution is more compact, ensuring electro-thermo-mechanical reliability becomes challenging. Moreover, the major interconnects, such as wire bonds and solder bumps, are more vulnerable to electromigration risk at high current density. Therefore, electro-thermo-mechanical performance and EM-aware reliability optimization are required before fabricating a module. Though FEA-based tools can be used for capturing these performances, those tools are not efficient to be used in the optimization loop due to long runtime. Also, several iterations are required to achieve acceptable performance in all aspects. To address these issues, PowerSynth 2 is equipped with reduced-order electrical, thermal, and reliability models, which are fast and quite accurate compared to FEA tools. The built-in electrical model performs resistance, capacitance, inductance evaluation, and parasitic netlist extraction for 2D/2.5D MCPM layouts. Also, there is an API for leveraging FastHenry [14] electrical models for R, L evaluation of 2D/2.5D/3D MCPM layouts. Reliability models include static and transient junction temperature, stress, EM-associated risk evaluation, and partial discharge (PD) impact reduction. Maximum, average, and peak-to-peak temperatures of 2D layouts due to the transient thermal cycling input are considered, which is proportional to the thermal stress endured by the devices. APIs are developed to accommodate available modeling approaches in collaboration with other research groups. For example, ParaPower [15] has been interfaced to evaluate static, transient thermal performance, and mechanical stress of 2D/3D MCPM layouts. Besides, our Z-Mesh tool and Synopsys HSPICE engine are linked through API with PowerSynth 2 for evaluating current density distribution efficiently.

C. Physical Design and Post-Layout Optimization

PowerSynth 2 has a genetic algorithm and built-in optimization framework based on reduced-order modeling. Both electro-thermal and reliability optimization can be performed within the framework. More details are provided in Section III. Once the optimizer generates the solution space, a non-dominated sorting is applied to get the Pareto-optimal solutions. After choosing an optimized solution for fabrication, post-layout optimization features like filleting the sharp corners to reduce current crowding and field focusing can be performed. The user can select an optimized design from the solution browser to export in commercial 3D CAD tools like ANSYS Q3D, SolidWorks, etc. Exporting a distributed full parasitic netlist with RLC elements is another attractive feature. The exported netlist can be used to perform re-simulation, completing the roundtrip engineering design loop before fabrication. Finally, the optimized solution can be fabricated to validate the performance predictions through measurements.

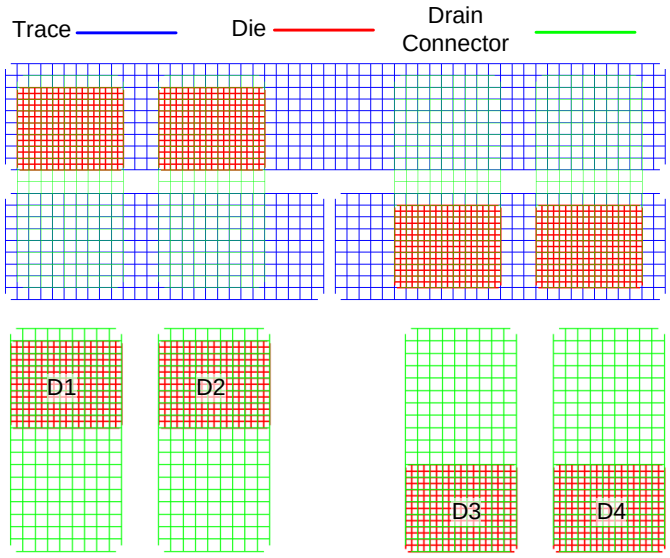

Fig. 3. Sample mesh from our Z-Mesh tool

III. Methodology and Design Tools

EM-aware electro-thermal and reliability optimization workflow is shown in Fig. 2(b). The flow involves PowerSynth, Z-Mesh tool, HSPICE, FastHenry, and ParaPower to perform different steps. PowerSynth takes the input information from the user, and the layout engine generates layout solutions. Each solution is evaluated for each performance metric by the corresponding model or tool.

A. Z-Mesh Tool

Since parasitic inductance has a significant impact at higher switching frequencies of the WBG devices, the impedance distribution of the power loop of a module needs to be considered for current density distribution evaluation. A quick and accurate resistive mesh modeling (R-Mesh) tool is reported in [16], which has shown a 517$\times$ speed up against Cadence Encounter Power System (a commercial power integrity analysis and optimization tool for VLSI) with only 1.3% error for a 2D memory die design. This tool has been modified to consider the inductance impact for each mesh element and is named as the Z-Mesh tool. Z-mesh tool takes the layer stack, layout geometry, material, supply voltage, current, and mesh size information from the user through PowerSynth API. Each layer material's resistivity is updated to reflect the equivalent inductive impedance of the material. FastHenry evaluated loop inductance is used to calibrate the modeling

TABLE I
EFFICIENCY COMPARISON OF CURRENT DENSITY EXTRACTION

Model	Runtime (s)	Speedup	Memory (MB)	Memory Reduction
ANSYS	310	×1	10329	×1
Z-Mesh	0.28	×1107	513	×20

of resistivity to capture the inductance impact properly. This calibration needs to be performed at each frequency case, thanks to the PowerSynth API that makes the evaluation very fast. Then, it creates a Z-mesh network modeling the impedance distribution of each layer for a given mesh size. The resultant impedance network is stored as a SPICE netlist, where DC+ and DC- terminals are mapped as current sources, and sink, respectively. The rated current provided by the user is considered during HSPICE simulation, and current through each element is extracted. Since this tool uses an impedance circuit model, and SPICE engine for solving the circuit, it is much faster than the FEA simulation.

A flip-chip half-bridge module is considered for the demonstration of the Z-Mesh tool meshing results. The module structure is shown in Fig. 4. This half-bridge module has two SiC MOSFETs per switching position on a direct-bonded copper (DBC) substrate. Both source and drain sides have a 4×3 array of solder bumps. For this case, the Z-Mesh tool creates three layers of meshes, where the bottom layer contains all traces, the middle layer has the SiC die, and the top layer has the drain connectors. To improve the impedance model accuracy, a finer mesh is used on device layers compared to trace and connector layers. The solder bumps are modeled as copper vias to complete the loop. The corresponding meshing is shown in Fig. 3, where the top one shows the combined meshing for all three layers, and the bottom one shows the die and connector layer's combined meshing. To calculate the current density for each solder bump, the current through each via is obtained from SPICE simulation results. This current value is divided by the cross-sectional area (1 mm^2 for this example), to achieve the current density distribution. The extraction efficiency comparison between our Z-Mesh tool and ANSYS Workbench is shown in Table I. From the table, it is clear that the Z-Mesh tool has orders of magnitude speedup and 20 times memory reduction compared to the FEA tool and hence make this tool suitable to be used in the optimization loop.

B. EM-Aware Reliability Evaluation

1) EM Modeling: EM-associated reliability metrics include MTTF for the solder bumps and resistance increment for the wire bonds. These metric values can be calculated based on a closed-form model, which can be used for relative performance measurement by excluding the experimental result-dependent parameters. Also, the lifetime can be estimated based on a data-driven model developed by purely experimental results. EM-associated risk assessment for both wire-bonded and flip-chip module can be performed by both of these models. Both of the modeling techniques are described below.

- **Closed Formula Model:** In this model, the well-known Black's equation is used for the lifetime estimation of each interconnect. The equation is as follows.

$$MTTF = \frac{A}{J^n} e^{(E_a/kT)}$$

Here, A is a constant based on the cross-sectional area of the interconnect, J is the current density, E_a is the activation energy (0.9 eV), T is the temperature of the interconnect, n is a scaling factor (set to 2), and k is the Boltzmann's constant [17]. The current density and the maximum temperature are extracted for each interconnect. Then, Black's equation is used to measure the relative value of MTTF for each interconnect, considering the A as the same constant for all the bumps. Thus, a relative number can be used for comparing the interconnects' reliability in the same layout.

- **Data-Driven Model:** To develop a data-driven model, experiments need to be designed very carefully to capture the parameters that initiate EM-associated failure. The experiments need to be customized based on the interconnect type. A parameter sweep is required to collect data at different current and temperature ranges. The temperature range needs to be planned carefully based on the solder materials used in the module. Once the data are collected, a look-up table can be generated to develop the model. Also, the data can be used to tune the constant parameters of the closed formula model to predict the absolute lifetime rather than the relative one.

2) Implementation Methodology: In this work, a Black's-law-based model has been used for the flip-chip module with solder bump interconnects, and a data-driven model has been used for the wire-bonded module.

Solder Bump: Since solder bumps are emerging interconnects with low electrical parasitics [4, 9] and the PowerSynth 2 layout engine can optimize flip-chip designs with solder bump arrays, current density and temperature distribution across those arrays are extracted for MTTF evaluation using the closed formula model. The module structure is ported to Z-Mesh tool to get the current density for each solder bump. The maximum temperature distribution across the solder bumps is read from the ParaPower interface under the given boundary conditions. Using the closed formula model, the relative MTTF value is determined for each bump.

Wire Bond: A look-up table from the data-driven model is used for the lifetime estimation of wire bonds in a power module. Data can be collected from FEA results, which is time consuming and requires experimental validation as well. Also, it is hard to get data from power module industries due to proprietary issue. Therefore, an accelerated test is performed in-house on 5-mil aluminum wire bonds under different current and temperature conditions using a custom fixture assembly (shown in Fig. 9(a)). Details on the experimental setup and data collection are described in Section IV. PowerSynth 2 parasitic netlist extraction feature is used to set up the circuit simulation under given operating conditions. SPICE simulation is performed to get the current through each device. It is assumed that each device has an equal current distribution

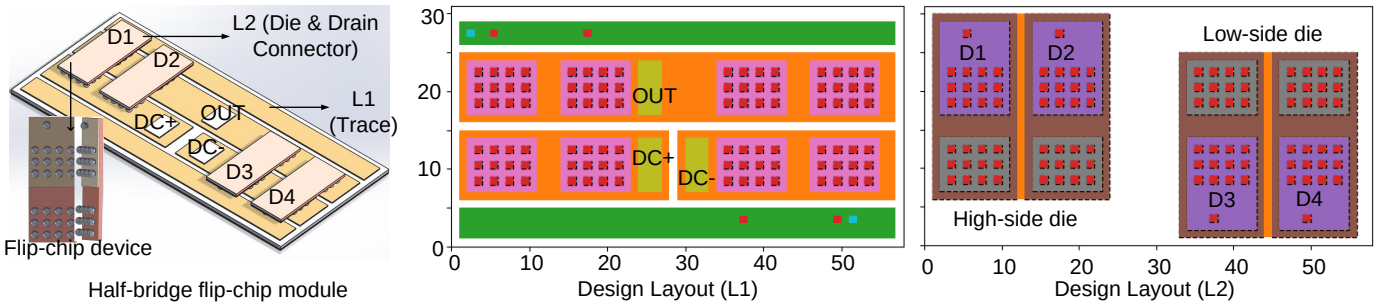

Fig. 4. Minimum-sized solution from PowerSynth

through the source-side wire bonds. Therefore, the current through each wire bond is calculated from the resultant device current. The current density of the wire bonds is found from the result of dividing the current through the wire by the cross-sectional area of each wire. ParaPower has been used to find the temperature distribution of the die and wire bond interfacing area. Then, these current density and temperature values are mapped in the experimental results to estimate the failure time.

C. Reliability Optimization

In this work, three objectives are considered: electrical parasitics (loop inductance), the static maximum junction temperature of the module, and MTTF for interconnects. The solution space is generated based on the first two objectives. The API between PowerSynth and FastHenry is leveraged for electrical loop inductance evaluation, and the ParaPower API is used for the static maximum junction temperature. Then, the MTTF value for each interconnect of the solutions is evaluated. Since each solution has multiple interconnects, the minimum value of MTTF is considered for comparison among different solutions. The built-in randomization algorithm is used to optimize the power loop inductance and maximum junction temperature. Both flip-chip and wire-bonded modules are considered for electro-thermal optimization. Before optimization, a minimum-sized solution layout is generated and evaluated to capture the maximum possible power density. To further optimize, a set of fixed floorplan-sized solutions with different floorplan sizes are generated and evaluated. For each fixed-sized solution set, the extra room is calculated from the difference between the minimum size and the given floorplan size. In randomization, the extra space is distributed by following either a uniform or multinomial distribution. However, a genetic algorithm uses mutation and crossover to generate a new set of design variables in each generation and distributes the extra room among the constraint graph edges by using those design variables as weighting factors. Finally, a Pareto-optimal solution set is reported from both algorithms by applying non-dominated sorting on the solution space.

Though static maximum temperature has been used in this flow to estimate the interconnection lifetime, the PowerSynth transient thermal model [12] can provide maximum, average, and peak-to-peak temperature under a certain thermal cycling condition. Our fast and accurate transient thermal model has been proven to be about 3,489 times faster with less than 10% error compared to ANSYS simulation for 2D cases. PowerSynth-guided reliability optimization flow can reduce the induced stress on the interconnect due to thermal cycling by optimizing the layer stack material, thickness, placement, and routing of the components. PowerSynth 2 already handles custom reliability constraints to ensure safe high power operations. Therefore, PowerSynth 2 can produce more reliable layouts upon integrating the EM-aware reliability optimization flow.

IV. Experimental Results

A flip-chip module and a wire-bonded module are considered for optimization. Results for each case are described below.

A. Flip-Chip Module Design

As a case study, the flip-chip half-bridge module shown in Fig. 4 has been considered for optimization. In the planar view of the solution layout, L1 contains the traces, power, and gate terminal footprints. On the L2 layer, the SiC MOSFETs with drain connector footprints are available. Both layers have the solder bumps footprints, which make the inter-layer connection and complete the loop.

To demonstrate both DC and AC modeling capabilities in the Z-Mesh tool, the minimum-sized solution layout case is chosen. The temperature distribution and current density distribution at DC (100 V, 1 A) are shown in Fig. 5. For the temperature distribution, a 1000 W/m^2K heat transfer coefficient is applied on both sides of the module, and 25 W heat dissipation is applied to each device. At DC, the current density results show a uniform distribution for the drain side connector bumps, whereas the SiC source side bumps have a symmetric distribution from the center towards the edges as the device has the gate region in the center. Since the resistance is dominated at DC, and trace resistance is neglected compared to the SiC and solder joint resistances, there is almost no variation in inter-die distribution. The current density is pretty small as the total current is considered only 1 A, thus each device is getting approximately 0.5 A and distributed among 12 solder bumps. For the temperature distribution, since source side solder bumps are closer to the device compared to the

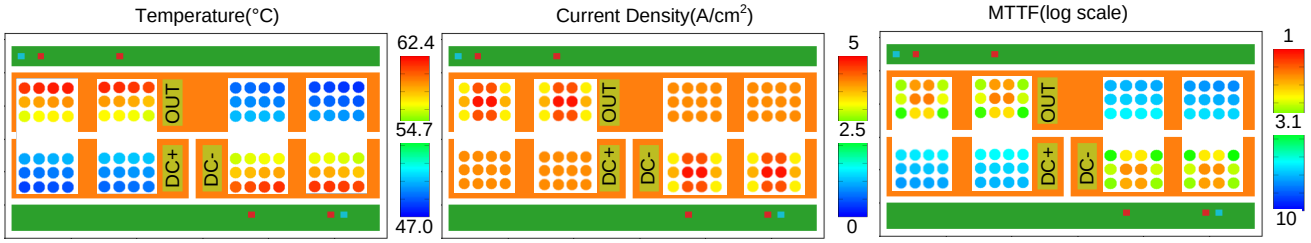

Fig. 5. Temperature, current density, and MTTF results at DC

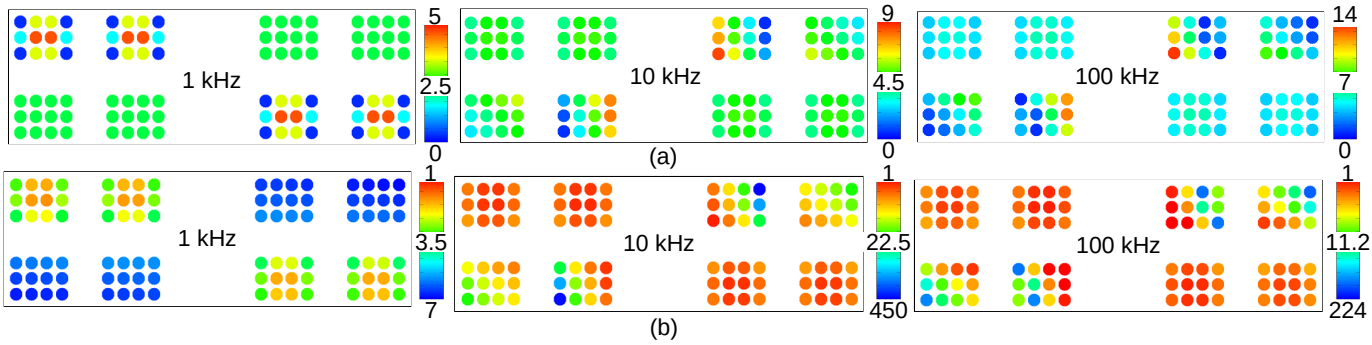

Fig. 6. AC results: (a) Current density distribution (linear scale), (b) relative MTTF values (log scale)

drain connector bumps, they have a higher temperature. Using Black's law, MTTF is evaluated for each solder bump. From the MTTF results in Fig. 5, it is evident that the MTTF is very much dependent on the temperature distribution. The source-side solder bumps are hot spots, thus they have a lower MTTF compared to the drain-side solder bumps.

Fig. 6(a) shows the current density variation at different frequencies. At low frequency, the resistance and inductance are comparable, and the variation in current density distribution is still similar to the DC case. However, with the increasing frequency, the trace inductance is dominating compared to the resistance. Therefore, variation in current density distribution depends on the distance of the device from the source or sink. The inter-die current density distribution variation is captured at AC, whereas the intra-die variation at DC. The MTTF results (shown in Fig. 6(b)) show the current density dependency of the MTTF values with the increasing frequency. At low frequency, the distribution is more temperature-dependent. Since the temperature distribution does not change with frequency, the current density distribution impact dominates. For example, 10 kHz MTTF distribution shows that the drain side solder bumps have a lower MTTF compared to many source side solder bumps due to higher current density. Therefore, both temperature and current density variations must be properly captured for reliability analyses.

To optimize the sample flip-chip half-bridge module, ten different floorplan sizes varying from 2100 mm^2 to 2992 mm^2 are considered with 15 solutions for each floorplan size at DC operating conditions. The runtime is only 135 s per layout with electrical, thermal, and reliability evaluations. The solution space is shown in Fig. 7(a). For each solution, the area is color mapped. Three layout solutions are chosen from the Pareto-front to demonstrate the layout impact on the optimization and are shown in Fig. 7(b). Fig. 7(c) shows the distribution of MTTF for each selected layout. From the layouts, it is clear that Layout A has the lowest footprint area (60 mm $\times$ 35 mm) and has the highest temperature rise, which results in a lower MTTF value (1.26). On the other hand, layout C has the largest footprint area (68 mm $\times$ 44 mm), which helps reduce temperature. This layout has achieved the highest minimum MTTF (1.92). Between two extreme solutions, layout B (66 mm $\times$ 44 mm) shows a balanced performance in all objectives with a minimum MTTF value of 1.65. Since this is the DC current distribution case, the MTTF is temperature-dominated. From the MTTF distribution, it is clear that no solder bumps from layout A have achieved an MTTF value greater than 9, whereas both B and C have a good number of solder bumps with higher MTTF values. These results can be used to filter out reliable solutions by setting up a threshold value for MTTF.

TABLE II
MTTF OPTIMIZATION WITH VARIOUS SOLDER BUMP ARRAY SIZES

Array Size	Max. Current Density (A/cm^2)	Max. Temperature (°C)	Min. MTTF	MTTF Increment
4×3	4.86	62.43	1.19	$\times 1$
5×4	3.13	62.34	2.89	$\times 2.4$

Apart from varying floorplan sizes, the solder bump array size can vary within the same floorplan size. This variation can help optimize the MTTF with more even current distribution. For example, for the same minimum-sized solution case (shown in Fig. 4), if the solder bump array is changed from 3×4 to 5×4, the minimum MTTF can be improved by 2.4 times as shown in Table II, where MTTF values are relative numbers.

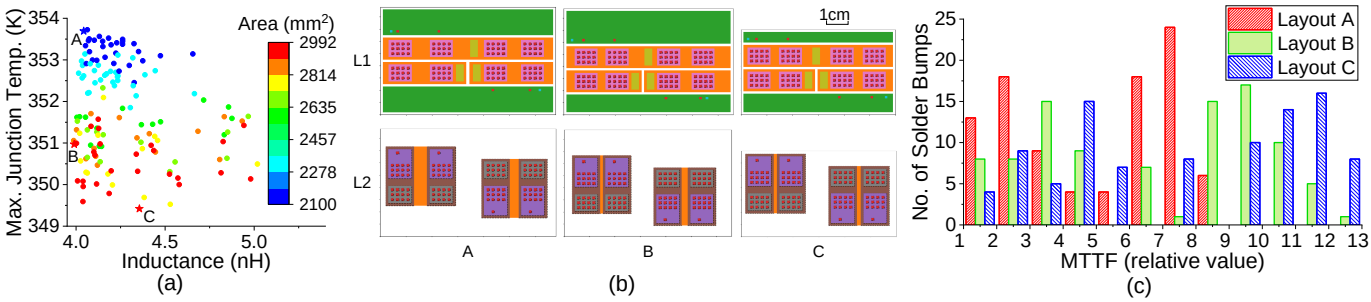

Fig. 7. (a) Optimization solution space, (b) three selected layouts, (c) MTTF distribution of three layouts.

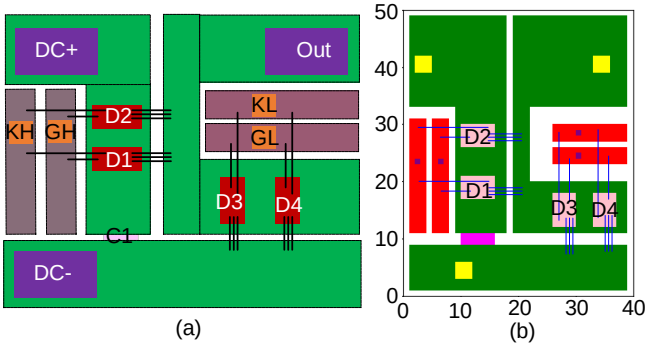

Fig. 8. Wire-bonded case: (a) initial layout, (b) balanced solution

B. Wire-Bonded Module Design

To demonstrate the EM assessment capability, a sample 2D wire-bonded module design is chosen and shown in Fig. 8(a). The module has two SiC devices per switching position and an on-module decoupling capacitor (C1). Here, KL, GL, KH, and GH represent low-side kelvin source, low-side gate, high-side kelvin source, and high-side gate pins, respectively. This initial module has been optimized for electro-thermal performances, and the solution space is reported in [11], where a balanced solution (shown in Fig. 8(b)) has been validated through manufacturing. Since this design has already been hardware-validated, we have chosen this optimized design case for EM-associated risk assessment. Failure of a wire bond in this study is a 10% increase in electrical resistance of the wire [18]. PowerSynth extracted parasitic netlist has been used for circuit simulation with 23 A current source and 131 µH load inductor between DC+ and OUT terminals. From simulation results, the current through D1, D2, D3, and D4 is found at 11.53 A, 11.26 A, 11.55 A, and 11.24 A, respectively. There are three parallel wire bonds in each device. Therefore, the current through each wire bond is calculated by dividing the corresponding device current by the number of wire bonds. Since 5-mil wire bonds are considered, the current density is extracted by dividing the current by the cross-sectional area. The current density and the temperature distribution results are mapped from the experimental results described in the following section to get the failure metric. The results are summarized in Table III.

TABLE III
RELIABILITY EVALUATION OF WIRE-BONDED 2D MODULE

Device	Current (A)	Temperature (K)	Wire Bond Current Density (A/cm2)	10% R Increment Time (Hrs)
D1	11.53	416.8	3.03×10^4	217.4
D2	11.26	416.5	2.95×10^4	229.6
D3	11.55	427.0	3.03×10^4	210.8
D4	11.24	427.7	2.95×10^4	221.9

C. Wire Bonds EM Test

The test setup is shown in Fig. 9(a). The wire-bonded samples consist of two independent DBC cards, outfitted with SAC305 soldered hex standoffs for power and voltage monitoring connection to the DBC card pads. The two cards are connected using four aluminum wire bonds, creating a series of four independently measurable bonds for each experimental run. DC power connection is supplied to the bonded samples within an oven using a low-noise power supply. This setup is used to apply ambient temperatures of 295 °C, and currents of up to 15 A to each set of wire bonds. The failure criteria for experiments is a 10% increase in electrical resistance. This change in resistance is monitored over time using a high-fidelity DATAQ voltage module. It is connected to the wire bonds with a 4-wire voltage measurement configuration. By monitoring the change in voltage over time and dividing by the constant electrical current imposed on the wire bonds during testing, the change in electrical resistance is obtained.

24 wire bonds are tested under EM conditions (elevated ambient temperatures and current densities) using the accelerated testing setup to gather failure time data. In addition to these experiments, the temperature coefficient of resistance is measured to account for wire bond joule heating. By combining the EM results with the temperature coefficient of resistance measurements, a contour plot of the results is shown in Fig. 9(b). It aggregates the current density through the wire bonds, the temperature of the wire bonds at that current density, and the corresponding failure time.

From the experimental results, it is clear that as current density and ambient temperatures are elevated, the lifetime of the wire bonds is reduced. These results are used in the data-driven model to evaluate the failure time of the 2D wire-bonded module case. As power density increases, current density and temperature impacts may be amplified on power module interconnection, emphasizing the need for a tool to

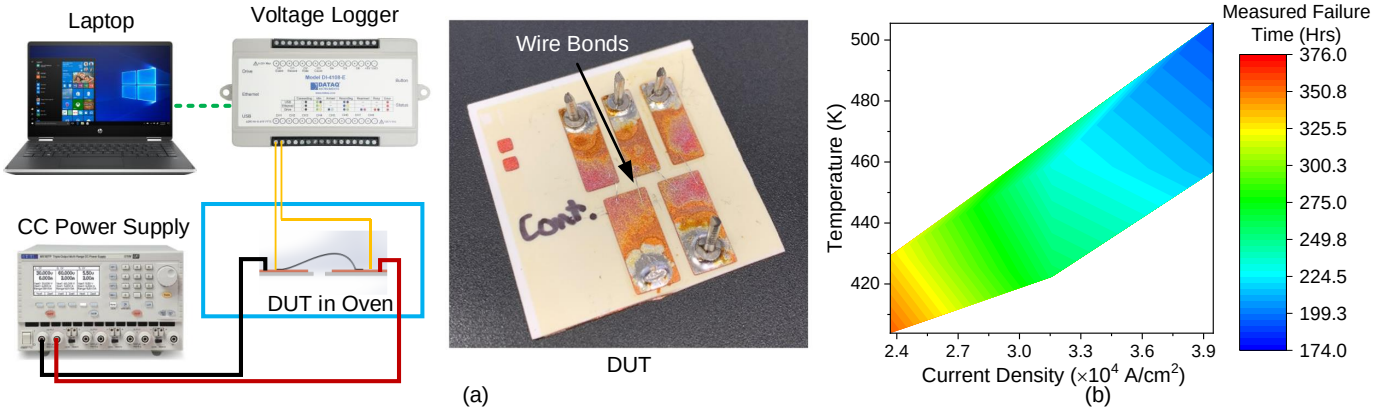

Fig. 9. (a) Test Vehicle for establishing EM experimental failure risk in Al wire bonds, (b) Reliability data library based on the experimental results

optimize a module layout for a longer lifetime.

V. Conclusion and Future Work

PowerSynth 2 is equipped with new reliability models with fast and accurate models for current density, temperature distribution, and EM-aware MTTF estimation. Both flip-chip and wire-bonded SOTA design cases can be designed with our electro-thermal-reliability co-optimization. It is promising to capture detailed current distribution impact on EM-related risk of MCPM designs. This generic and efficient methodology can be applied on both flip-chip and wire-bonded modules. Both closed-form models and data-driven models are used to evaluate the lifetime of the interconnects. However, experiments are required to more accurately tune the model parameters. A few limitations with the current tool flow include: The solder bump is modeled as a cube rather than a sphere; The device temperature is used for wire bonds; Current distribution through each wire bond is assumed to be equal, etc. In the future, some of these limitations can be addressed with updated Z-Mesh and EM models, and PowerSynth 2 can further improve the physical design process with design-for-reliability CAD flows.

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