PowerSynth Integrated CAD flow for High Density Power Modules

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***Abstract*—In the last few years, design automation for multi-chip power modules (MCPMs) has become a trending research topic in the power electronics community. Many different research efforts have demonstrated the advantages of bringing Computer-Aided Design (CAD) flow into MCPMs design and optimization. Among these works, PowerSynth has shown to have the most complete and mature CAD design flow for MCPMs. This paper will go through some of the recent research and development in PowerSynth. Modeling and layout generation algorithm will be discussed in the paper. The most recent results for 3D layout generation and optimization are also discussed and demonstrated.**

***Index Terms*—Design Automation, High Density MCPM**

I. Introduction

Development in Wide Band-Gap (WBG) technologies [1] have recently allowed power electronic circuits with faster switching speed, higher voltage and current ratings, and higher efficiency. In addition to this fast development, new module packaging technologies [2], allow a more compact circuit element arrangement into a single package. Because of this, the multi-chip power modules (MCPMs) layout design has become a more challenging task for packaging engineers. Many reliability issues have arisen and need to be considered during the design state. These include electrical parasitics, thermal management, mechanical reliability, electromagnetic interference (EMI), and partial discharge (PD). However, these design aspects are usually conflicting with each other. For example, a more thermally optimized design should have a bigger footprint for better heat dissipation. However, this, in turn, would increase the inductance due to larger current loops. Due to these conflicts among the design aspects, the MCPM layout design is a multi-objective task. In a traditional layout design process shown in Fig. 1, the designer usually needs to run various analyses on the layout using computationally intensive methods. Once some layout analyses are done, circuit analyses such as transient simulation are performed to gain more knowledge on the circuit operation. Using this information, the designer can make manual enhancements to the layout until an optimal design is achieved. With the help from these Computer-Aided Design (CAD) tools, some improvements in both electrical parasitic and thermal performance have been presented in the literature [3]–[5]. However, this design process is still a labor-intensive design approach, usually taking weeks to months for each design. Hence, there is an increasing demand for design automation in the power electronics community. This paper will go through some of the most recent and continuous research efforts on MCPM design automation and demonstrate PowerSynth 2 architecture. This paper is organized as followed: Section II gives an overview of the current research and development of MCPM design automation. Section III gives an overview of PowerSynth 2 architecture automation design flow. This section also explains the tools' layout generation and optimization engines and then goes through some of the modeling approaches being used in PowerSytnh. Section IV shows some layout automation design examples using the tool. Finally, Section V concludes the paper.

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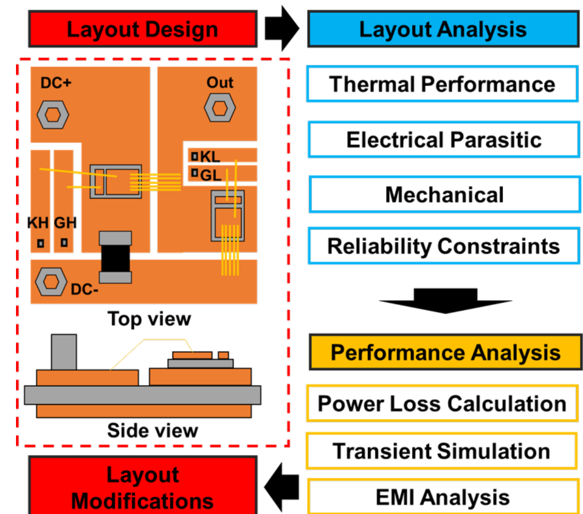

Fig. 1: The MCPMs traditional 2D layout design flow

II. Current status on MCPMs design automation

A. A review on some MCPMs design automation approaches

Many research groups have demonstrated different methodologies and approaches for the MCPMs design automation problem to overcome the traditional time-consuming design process. A sequential optimization methodology has been presented in an early attempt for layout optimization tools

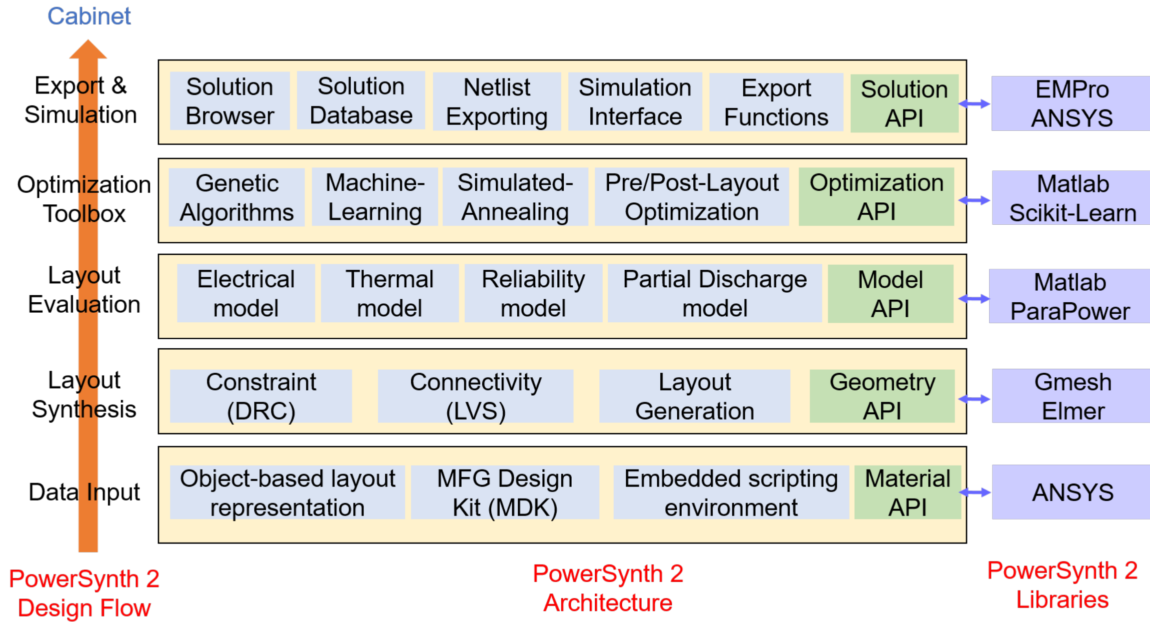

Fig. 2: PowerSynth 2 architecture design flow

[6]. Multiple computationally expensive FEA tools have been connected and controlled through scripting languages. The results of these FEA simulations are served as evaluated functions in a multi-objective optimization framework where the MCPM layout can be modified automatically. While this approach ensures high fidelity, the solution space has fewer candidates due to the computationally expensive FEA simulations. Since then, many other research groups have developed reduced-order models to reduce the complexity of the layout optimization process. The work in [7] shows an interesting approach for the lifetime optimization of IGBT MCPMs. To begin with, the author generates a design of experiment (DOE) to sample the design parameters. Then, FEA simulations are run from this DOE to build a surrogate model. This surrogate model is then used in power cycling (PC) and thermal cycling simulations to optimize the thickness values of each layer in the MCPM layout. [8] applies the sequence pair method learned from Very Large Scale Integration (VLSI) to optimize MCPM layouts. Two genetic algorithm frameworks have been used for device placements and copper routing. A Method of Moments (MoM) model has been applied to evaluate the layout resistance. Once the loop resistance is calculated and the current path is known, parasitic loop inductance is calculated using the boundary element method. Layout area, loop inductance, and loop resistance are combined into a cost function for the optimization process. One drawback of this method is the number of mesh elements would increase with the layout footprint to ensure accurate loop inductance evaluation. An interesting approach for device dynamic current balancing has been shown in [9]. In this work, the author has applied response surface modeling methodology to find the relationship between geometry information and parasitic inductance of Double Bonded Copper (DBC) traces and bonding wires. After the model formation step, a non-linear optimization package in MATLAB is used to perform layout optimization for the best bondwire landing positions. The optimized result has shown better balance among parallel device drain currents. However, the layout design parameters are quite simple and limited. More recently, [10] has shown an efficient method to extract layout parasitics parameters considering mutual inductance among conducting paths. According to this research, this model is faster, having similar accuracy, and more memory efficient than FEA simulations. However, in this work, the layout design parameters and layout generation methodology are not discussed. Among these groups, a design automation and optimization tool named PowerSynth [11], [12] has a complete design flow for MCPMs. This tool has its modeling library for various design aspects (e.g., electrical parasitic, maximum temperature), along with a generic and salable layout generation algorithm.

B. PowerSynth progression towards 3D MCPM design

The idea of PowerSynth originates from an MCPM layout optimization framework called PowerCAD [13]. In this work, the author used the fmincon optimization package in MATLAB to optimize simple MCPM layouts. To optimize for electrical parasitic, the optimization engine sent each layout's geometry information to FastHenry. The layout geometry is also used to characterize a thermal resistance model, where a circuit simulator is used to evaluate the maximum temperature. This optimization framework, while promising still is also very computationally expensive and slow. Since then, this PowerCAD idea has been evolved into a more user-friendly and capable CAD tool known as PowerSynth. Tremendous research and development efforts from the PowerSynth group

have demonstrated the tool's potential for a complete physical design flow of MCPMs. The first version of PowerSynth v1.1 [11] has demonstrated the tool capabilities for automation design and optimization of the simple 2D layout structures. This version has been applied in some co-design attempt to optimize, design, and fabricate MCPM layouts [11], [14]. However, the layout generation algorithm in this work only supports simple 2D layout structures. The post layout design rule check (DRC) requires for each generated solution, limiting the number of solutions in the solution space. The new generic, scalable and efficient methodology with constraint-aware layout engine has been demonstrated in [12] to overcome these limitations. This new algorithm allows layout generation and optimization for most of 2D-2.5 D layouts. With the v1.9 release, a complete PowerSynth enabled CAD-flow has been hardware-validated against 2D-2.5D MCPMs design. A few co-design examples using PowerSynth v1.9 design flow have shown the tool capabilities in improving MCPMs layout performance while maintaining accurate design constraints for layout fabrication [11], [12], [15] The layout generation methodology has been further enhanced in [16] through a hierarchical approach to push the power density. This hierarchical approach has also been proven to be beneficial to handle 3D power module layouts.

Along with the advancements in layout generation and optimization algorithm, a library of reduced-order models have been developed for fast and accurate assessment of various physical design aspects such as electrical parasitic, thermal performance, mechanical stress and strain [17], [18] or reliability aspects such as electromagnetic interference and partial discharge [19], [20]. Using these models with the layout optimization in [16], it is evident that the 3D power module can be both electrically and thermally better optimized than the 2D counterpart. More recently, researches and studies on 3D MCPM packaging further improve the circuit efficiency and power density [2]. These new packaging technologies allow MCPMs designs with multi-layers, multi-substrate structure connection, elimination of bonding wires, and heterogeneous components integration. While these design approaches result in electrically and thermally optimized MCPMs layouts with reduced packaging parasitics and efficient thermal management, the layout design process becomes an even more challenging task for packaging engineers. Hence, the latest development for PowerSynth version 2.0 now incorporates these updated 3D structures, design constraints, and inclusion of heterogeneous components. Upgraded modeling techniques and application programming interface (APIs) also allow evaluation for these layouts. Some early results have shown the benefits of 3D MCPMs layouts versus the 2D ones.

III. An overview on PowerSynth 2 architecture

The recent development of PowerSynth 2 architecture has combined layout generation algorithms, modeling methodologies, and other functionalities into a single package Fig. 2. This new version allows layout optimization of both prevalent high-power density packaging technologies (i.e., wire-bondless, hybrid, flip-chip 3D) and relatively new packaging efforts (i.e., embedded micro-channel heatsink). In the **Data Input** state, the tool takes input layout script, manufacturer design kits (MDK), material information, and command-line instructions from the user to perform layout synthesis. The layout engine generates hundreds to thousands of layout solutions in the **Layout Synthesis** state while ensuring DRC and LVS (Layout versus Schematic) verification. These layouts are then sent to the **Layout Evaluation** state, where the reduced-order models evaluate all design targets. These evaluated values are fed into the **Optimization Toolbox** where different optimization algorithms can be selected. These optimization algorithms modify the layout design and generate a layout solution space. Due to the multi-objective nature of MCPM design, this solution space usually has more than two dimensions, where each dimension represents a design aspect (i.e., electrical parasitic, maximum temperature). In the **Export & Simulation** step, these layout solutions are stored in a database where users can access through a solution browser. The user can select each layout solution to perform further analysis and verification through the tools' external Application Programming Interfaces (APIs). Some APIs include Ansys Q3D, EMPro, and Solidworks. Finally, necessary output files can be generated for the layout fabrication.

A. Layout Engine and Optimization Engine

A constraint-aware, hierarchical layout engine has been developed for MCPM layout generation. A hierarchical corner stitch tree with the constraint graph methodology [12] has been extended to optimize 2D/2.5D/3D MCPM layouts in a generic, salable, and efficient way [16]. The engine can handle layouts with heterogeneous components and any 2D/2.5D/3D Manhattan geometry. The algorithms to consider both design and reliability constraints are shown to be efficient for MCPM design optimization [21]. To provide flexibility, the layout engine can generate solutions in different modes: minimum-sized, variable-sized, and fixed-sized. Minimum-sized solution gives the maximum power-density for a certain layout. Variable-sized solutions can generate arbitrary number of solutions with varying floorplan sizes. This mode can help user to come up with an optimum floorplan size for a certain packaging technology. Finally, the fixed-floorplan size solutions can be useful to optimize a layout with pre-defined floorplan size. These options are necessary to generate DRC-clean, reliable solutions. The latest version of the layout engine has overcome most of the limitations associated with the previous matrix-based approach [11] and can explore a larger solution space efficiently. Research is ongoing to support most of the available latest 3D packaging technologies like wire-bondless, flip-chip, hybrid, etc.

B. Reduced order modeling library

Along with the development in layout generation algorithm, research and development on the modeling side allow evaluation and analysis for 3D layout structure. The PowerSynth layout engine generates hundreds to thousands of layouts and

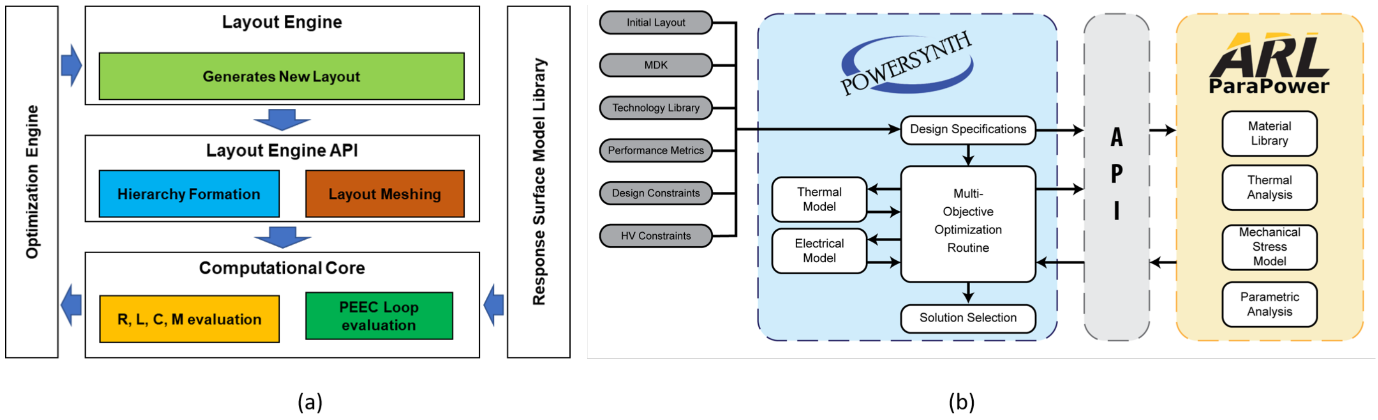

Fig. 3: (a) Electrical Model API (b) PowerSynth-ParaPower API [18]

evaluates their electrical parasitic and thermal performance to optimize the layout. This information is then fed to the optimization engine to make modifications to the layout. This section briefly describes some of the latest modeling efforts in PowerSynth.

a) Electrical Parasitic: Electrical parasitic, mainly parasitic inductance, is one of the key design aspects in MCPMs. This is because a high loop parasitic inductance could lead to voltage overshoot and increased power losses, reducing the devices' lifetime and circuit performance. Generally, to extract loop inductance, the designer often runs computationally expensive FEA simulations to extract the layout parasitics parameters. However, these FEA simulations are not suitable for evaluating hundreds to thousands of solutions from the PowerSynth layout engine. Therefore, a new electrical parasitic extraction method has been developed for layout optimization purposes.

A partial element equivalent circuit (PEEC) based electrical model has been developed in [17] to improve the evaluation performance while maintaining similar extraction accuracy. This model considers mutual coupling between different current-conducting paths in both 2D and 3D modules. As seen in, Fig.3 (a), an API has been developed to convert the layout information from the layout engine to geometrical data structure used in the electrical model computational core. Thanks to the hierarchical information from the Corner-Stitch data structure, the layout is divided into multiple connected partial elements. A characterized reduced-order model for MCPM traces is used to evaluate for partial R, L, and M values of each mesh element. These values are then fed into a Modified Nodal Analysis (MNA) calculator to extract the loop parasitics parameters. This method has been found to be a few orders of magnitude faster than FEA simulations while maintaining similar accuracy.

b) Thermal and mechanical models: Mechanical stress and strain, along with maximum device temperature, are also crucial design targets for high-density MCPM design. Although WBG devices such as SiC and GaN are known to have much better thermal conductivity than their Si counterparts, high-temperature condition can also limit their performance. Similarly, high stress and strain values can lead to reliability issues and reduce the lifetime of the design. On this end, an application interface between PowerSynth [18] and the Army Research Lab (ARL) ParaPower [22] has been developed. This API (Fig.3(b)) provides a bidirectional data flow between ParaPower and PowerSynth, which takes input layout, material, and MDK information and return evaluated thermomechanical value. ParaPower first converts the PowerSynth layout solution into a 3D thermal resistance network. This network is then used in a finite difference calculator to evaluate various design targets: static and transient thermal performance or stress induced due to the coefficient of thermal expansion mismatch (CTE).

C. Reliability and DRC rules library

In the high voltage and high current design of a compact MCPM layout structure, electrical phenomena like partial discharge are significant reliability concerns. Partial discharge is a localized electrical breakdown in an insulating material that potentially bridges the gap between the conductors. Because PD deteriorates the insulation material, it increases the chance for electrical breakdown, which makes the insulation material no longer insulating. Unlike electrical or thermomechanical design aspects, PD issues are too complex to be evaluated during the layout optimization state. Hence, to consider this effect in a layout, a systematic method [20] has been developed to formulate general equations through FEA simulations and experimental measurements. These equations allow the tool to quickly evaluate different trace-to-trace gap which can be used to update the DRC rules. The layout engine can use these new DRC rules to mitigate PD issues. At the moment, this method is applicable for 2D MCPM layout only. However, it can be extended to apply for 3D MCPM layout in the future.

IV. Results

A. 2D vs. 3D layout performace

Since 3D layouts are more compact compared to a 2D one, it can achieve higher power-density. To performa a electro-thermal performance comparison between 2D and 3D layout,

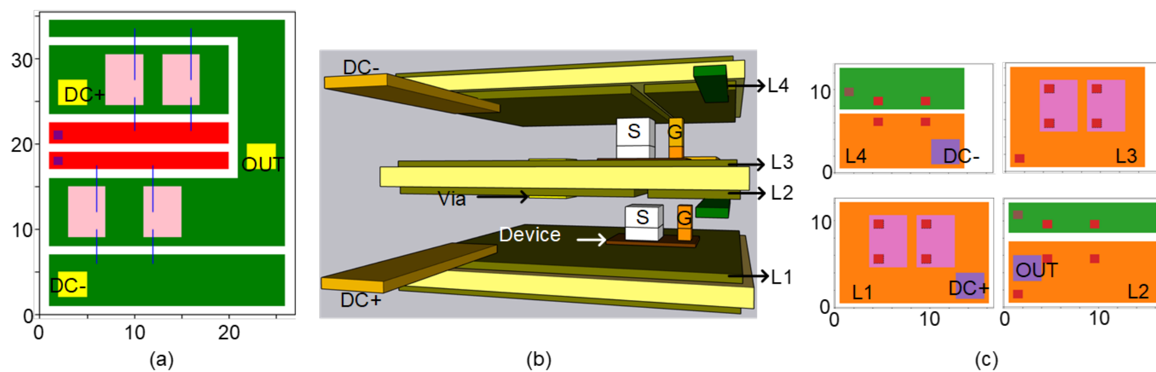

Fig. 4: Minimum-sized solution of half-bridge module: (a) 2D wire-bonded half-bridge module (25.3 mm × 35.2 mm), (b) 3D wire bondless structure, and (c) 2D view of each layer (16.7 mm × 13.1 mm)

two sample half-bridge layouts are chosen and minimum-sized solution is generated for each layout (shown in Fig. 4). 2D layout is a wire-bonded one, whereas the 3D structure is wire bondless (shown in Fig. 4(b)).Here, four layers are used to make a half-bridge module. The gate and source connections are performed through via-type connection with the consecutive upper layer. The minimum-sized solution layout shows that the 3D layout has a vertical power loop and double-sided cooling feature. For this minimum-sized solution, the power loop inductance of 2D, 3D layout is 20.23 nH, 1.52 nH, respectively. The via type connections have been considered as perfect connections and so no parasitics have been considered for those. The ambient temperature is set to 300 K, and for each die, heat generation is assumed 10 W. The thermal result (332.64 K vs 354.94 K) shows the 3D layout has more junction temperature compared to the 2D one.This is because the floorplan area of 3D layout is 4.1 times smaller compared to the 2D one. So, though double-sided cooling is used with 1000 W/m^2K heat transfer coefficient, the 3D layout cannot achieve better thermal performance. However, if the layout size is increased, the 3D layout can overcome the thermal limitation as well [16].

B. 3D layout optimization

PowerSynth 3D layout optimization capability is demonstrated using a wire-bonded 3D half-bridge module (shown in Fig. 5). The layout has been considered for electro-thermal optimization. Here, two DBCs are stacked face-to-face, and the layout of each layer is shown in Fig. 5(b). A via-type metallic post connection is acting as interconnect between two OUT traces. A set of minimum design rules is applied to generate the minimum sized solution (shown in Fig 5(c)). The layout is evaluated using PowerSynth electrical model and ParaPower thermal model. For this case, the heat transfer coefficient on both sides baseplate is set to 1000 W/m^2K, and ambient temperature is 300 K. For each die, heat generation is assumed 10 W. At 100 kHz, the loop inductance is about 6.40 nH and the maximum junction temperature is 328.24 K.This case has been used for further optimization with the same boundary conditions as the minimum-sized solution case. To have a better electro-thermal tradeoff, about 5000 solutions with variable floorplan sizes are generated and evaluated. The solution space and three sample solution layouts are shown in Fig 6(a), (b), respectively. From the results, it is evident that layout A (22 mm × 22 mm) has a lower inductance (5.99 nH) with a higher temperature (327.11 K). In contrast, Layout C (32 mm × 36.5 mm) has a lower temperature (318.24 K) with larger power loop inductance (11.39 nH). Among all the solutions, layout B (30 mm × 31.5 mm) has the optimum electrical (6.71 nH) and thermal performance (319.99 K) values with a reasonable floorplan size. So, layout B can be exported to 3D modeling tools and eventually fabricated.

V. Conclusion and Future Work

To conclude, in this paper, some of the latest works on MCPM layout design automation have been reviewed. The latest architecture of PowerSynth 2 architecture has been demonstrated. The layout engine algorithm, along with modeling approaches, has been explained. Upon implementing the architecture, the tool will not only be able to optimize 2D/2.5D/3D MCPM layouts but also allow exploration towards cabinet-level optimization. The initial results are promising towards high-density MCPM layout optimization. In the future, research and development on PowerSynth would support layout synthesis and optimization of most 3D MCPM layouts. Furthermore, the team will develop new models to reduce the computational efforts further.

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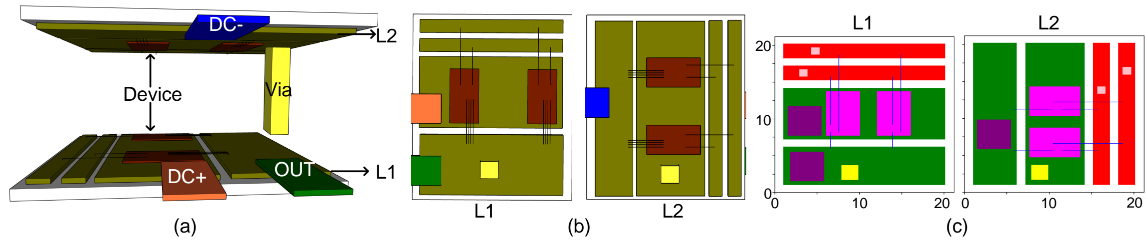

Fig. 5: (a) 3D structure of a wire-bonded MCPM, (b) planar view of each layer, (c) minimum-sized solution (21.2 mm × 21.2 mm)

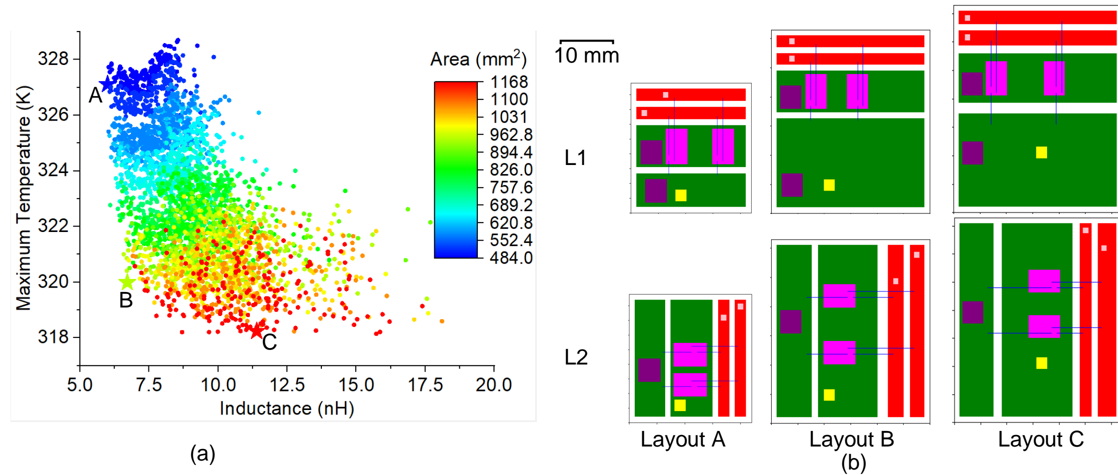

Fig. 6: (a) Complete solution space with three selected solutions, (b) planar layout of each layer for the selected solutions

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