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# PowerSynth progression on layout optimization for reliability and signal integrity

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**Abstract:** PowerSynth has been developed to significantly accelerate power module design through a multi-objective layout synthesis and optimization process. It uses a series of layout generation and optimization algorithms and various electrical and thermal models to automatically synthesize power module layouts and create a Pareto surface of solutions with optimum electrical and thermal performance. Recent advanced power modules are designed with various types of components integrated on multiple device layers to minimize the parasitics and increase power density. With more compact layouts and tighter design constraints, power module design becomes increasingly challenging because of reliability and signal integrity issues, such as partial discharge, electromagnetic interference (EMI), electro migration, and noise-induced false turn-on. This paper summarizes the latest PowerSynth layout engine and model improvements with an emphasis on the new reliability and signal integrity features. A generic and scalable constraint-aware layout engine is developed to process generic types of devices, traces, and connectors in power modules. Electrical models are improved from a 1D wire model to a 2D mesh model with enhanced feature sets to better capture the intrinsic layout structures and extract coupling between power and gate loops. EMI models are built on top of it to further reduce the noise analysis and qualification requirement posted on designers. Finally, a new post-layout optimization step is included in the flow as an improvement of design for manufacturability and reliability. The software development along with the hardware testing results demonstrates the latest advances in design automation for power electronics.



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**Key Words:** PowerSynth, design automation, reliability, power module, layout optimization

## 1. Introduction

The power module design process is a tedious task today. Engineers spend days and weeks on designing and validating power modules with FEM tools through trial-and-error methods to finalize the layout. Feedback from the power electronics industry has suggested about six to seven design-manufacturing-testing iterations before an optimized design is achieved and ready for the market. PowerSynth [9] is a software tool designed to allow engineers with very little packaging expertise to create power electronic module layouts from a draft design. It can be used to prototype layouts without the need for highly-experienced experts in power module design. Further, with its built-in models for electrical and thermal evaluation, PowerSynth can also be used to quickly analyze the layout quality without the need to run FEM tools that are highly expensive both price-wise and time-wise. However, existing electrical and thermal models are designed for 2D layouts, in which a single device and routing layer are allowed.

Recent research demonstrated working prototypes integrating multiple Direct Bonded Copper (DBC) [5, 12, 30] and Low-Temperature Co-fired Ceramics (LTCC) [8] substrates into a single stack with 3D layouts. In addition, double-sided sintering technology or metal bump interconnects are introduced to eliminate wire bonds. It not only reduces undesirable parasitic inductances, controls voltage overshoot, and allows a higher surge current, but also enables the ability for double-sided cooling for better thermal management. Undoubtedly, adding the third dimension to the layout has shown great potential for increasing power density with compact layouts and improving parasitics without any thermal limitations. This calls for an update on design tools to analyze and optimize heterogeneous design with a 3D structure with reliability and signal integrity considered.

Another growing trend to lower the overall cost of power modules is the integration of components other than just the power semiconductors. This includes passive elements such as decoupling capacitors and active elements such as gate drivers. Thermal sensors and switches can also be integrated to allow dynamic monitoring and fine-grain control. The proximity of these components to the power devices will increase in the quest for higher power density and advanced control. Consequently, during the physical design phase, the models that reflect the behavior of these items need to ensure that these components do not exceed their temperature range. However, it is still challenging to formulate a suitable layout synthesis strategy since new applicable models must be created.

The first version of PowerSynth (v1.0) is successful at creating layouts of limited complexity with improvements over hand-generated designs. However, it is restricted to planar DBC substrates with limited design rules. Signal integrity and noise are not considered in the physical design, since the electrical model ignores coupling capacitance and mutual inductance. Only thermal reliability is considered as the optimization algorithm attempts to reduce maximum temperature while electrical reliability issues induced by high voltage, large current density, and E-field focusing are not covered. Since then, PowerSynth research has focused on addressing some of the limitations that are discovered by both developers and end-users, and progress has been made on several fronts (see Fig. 1):

- First, improved electrical and thermal models are verified against hardware measurements [9]. An investigation into the mutual inductive coupling impact between power and gate loops has shown observable signal integrity concerns under various operating conditions. The model further leads to an auto-generated simulation test bench for analyzing switching transients and conducted Electromagnetic Interference (EMI) emissions from power modules.

- Second, previous efforts concerning design reliability involved current crowding studies, high E-field density and the need to fillet 90-degree corners. To further validate this observation, through the design of experiments and analyses of leakage current, models will be developed to predict partial discharge impacts, determine optimum filleting sizes and prevent potential failures through layout constraints and post-layout optimization.

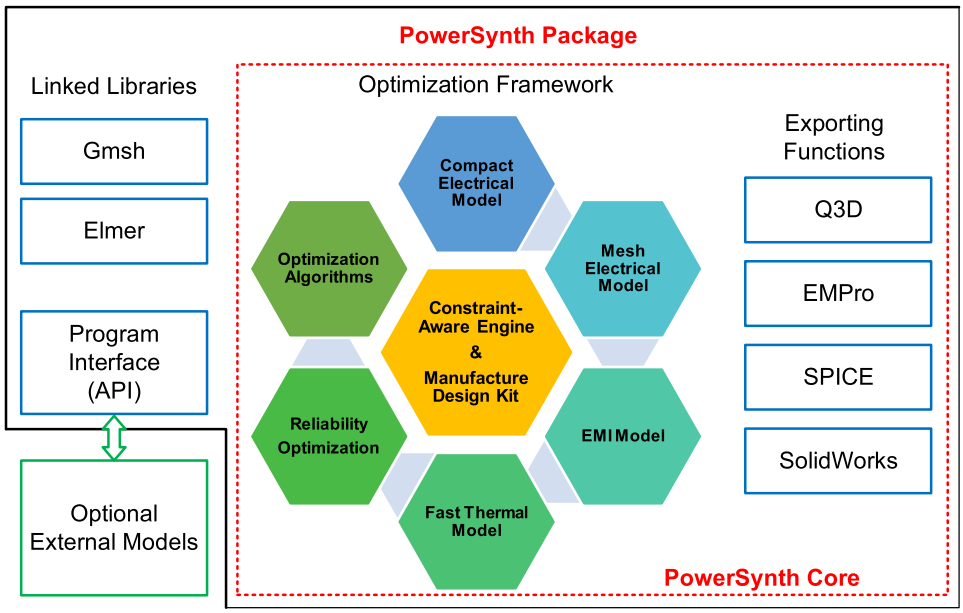


**Fig. 1.** Overview of the updated PowerSynth architecture.

- Moreover, the PowerSynth team has focused on models and algorithm research with software development. This leads to several significant breakthroughs such as automatic design constraint handling, a response-surface-based generic electrical parasitic model, a generic and scalable layout engine with hierarchical layout representation, an API to enable external optimization algorithms to be utilized, post-layout optimization with corner filleting, and an EMI model with module layout considerations.
- Finally, PowerSynth has been validated on layouts of a higher density and complexity with a focus on demonstration of optimization results. The team's software development was combined with hardware validation through fabricated DBC layouts and silicon-carbide power modules.

The development of PowerSynth aims to learn from existing approaches while addressing several challenges through a modular design approach (Fig. 1). In addition, as there exist many excellent contributions on power electronics modeling and optimization, PowerSynth also includes several interfaces so that external models and optimization algorithms can be used. This prevents duplication in software development and allows PowerSynth to be an integrated hub for research. The aforementioned new features are included in the latest version v1.3 as of the time this paper was composed. Some of the components are inherited from the previous version, such as symbolic layout input format, response-surface electrical model, fast characterization-based thermal model, genetic optimization algorithms, and export functions. Detailed description and validation results can be found in [9] regarding components developed in the previous version.

## 1.1 Evaluation of state of the art

While still having a lot of room for improvement, especially in the modeling and optimization areas, there is no other tool that combines design drafting, technology, material library creation, electrical and thermal modeling, and layout evaluation and optimization all together into a single package. Therefore, the comparison is limited to individual aspects of the flow.

- Layout Representation: Layout abstraction and evaluation of a minimum-sized layout are solved problems in VLSI CAD. Specialized data structures and models such as constraint graphs [29] are used to replace a more generic but time-consuming linear programming engine. However, PowerSynth is unique and leading in two aspects: First, it is the only layout generation tool specialized in and optimized for power electronics. Most existing layout tools are derived from PCB editors. This makes them highly suitable for routing thin signal lines, but not wide power

traces. The high-current/voltage traces and the sensitivity to parasitics are contradictory in nature. This tradeoff generally requires a lot of design experience to understand. Existing tools can only process constraints as a verification step. Designers draw planes and traces while the tool checks the design on-the-fly or afterward, but cannot make design decisions for users.

- Physical Design: In VLSI, the traditional approach is to consider each module as an independent module and wire connection is performed later during routing stage. This leads to some popular floorplan-driven algorithms such as Slicing Tree [16], Polish Expression [28], or Sequence Pairs [21]. Recently, these approaches are also extended to power electronics floorplanning problem, both in 2D [22] and 3D layouts [3], followed by a genetic algorithm for layout optimization.

  Previous work all focused on component placement while the routing or connectivity was not considered. Polish Expression or Sequence Pair cannot preserve the connectivity, thus they cannot be directly used for routing purposes. On the other hand, PowerSynth takes a different approach and uses a Layout-Driven Physical Design (LDPD) flow. The idea is behind this flow is simple. Since the layout naturally contains all of the design information such as the netlist, constraints, manufacturing layers, devices, and parasitics instead of constructing the layout, PowerSynth synthesizes the design from a layout provided by the user. Instead of performing schematic design, floorplanning, placement, and routing step-by-step, the physical design and optimization are constructed in a single step directly based on the layout.

  The LDPD flow, however, requires different layout creation and optimization algorithms since component connectivity must be preserved during the design stage, effectively maintaining an LVS-clean (Layout matches. Schematic) design. In addition, in order to enable the design to be manufacturable and reliable, design constraints and aging-induced constraints must be honored during the optimization stage. The first version of PowerSynth processes the DRC rules as a follow-up step after each layout is created. This approach is not efficient and scalable since many layouts are discarded because of design rule violations, resulting in an NP algorithm. In this work, the layout engine has been significantly updated to consider DRC during the layout generation step using a polynomial-time algorithm, allowing for more complicated design rules. For example, reliability concerns such as aging effects, current-crowding effects, or high-voltage safety operation can now be treated as reliability design rules on top of manufacturing design rules during layout optimization. The impact can be directly observed from the Pareto-Front and tradeoffs can be tuned across multiple targets.

- Electrical Modeling: Most existing models can be categorized into mesh-cell-based or wire-based models focused on extraction accuracy, because extraction is performed after the layout is generated and traditionally counted as a verification step. As a result, the runtime of these models can often be tolerated. Few models are created considering the special needs for power electronics such as Kelvin connections and vertical wide-bandgap (WBG) devices.

- Thermal Modeling: Most thermal tools are mesh-cell-based targeting generic structures. With a simplified thermal RC network, the runtime is generally acceptable in the optimization loop. Examples such as HotSpot [27] for IC designs and ParaPower [2] from ARL are all based on this approach. They improve the runtime compared to FEM simulations with tunable mesh size but are slow on complicated layouts.

- EMI Modeling: While the fast-transient behavior of WBG devices reduces switching losses, their high di/dt and dv/dt behavior at turn-on and turn-off can lead to increased current and voltage overshoots and converter EMI [23]. Reduction of these effects can be achieved through the strategic reduction and balancing of parasitic inductances and capacitances within the module layout [7]. However, these techniques often lead to more compact placement and routing of devices that can lead to increased mutual heating among closely-placed devices and less metal area for heat dissipation. To better explore these tradeoffs in power module layout design,

PowerSynth needs to incorporate EMI models and metrics that can be used within the multi-objective optimization framework.

- Layout Optimization: Most literature uses a generic optimization framework such as Genetic Algorithm [6] or gradient-based methods. These widely-adopted methods are easy to implement with packaged libraries. However, for 3D heterogenous layouts, the layout complexity and number of design variables grow exponentially. More importantly, the dependency between variables makes it difficult to control the optimization process in a generic way. Therefore, customized algorithms are in great need for expanding design capability without sacrificing flexibility and efficiency.

## 2. Layout engine

A constraint-aware, generic, and scalable layout engine has been integrated with PowerSynth to handle complex geometrical layouts considering heterogeneous components (i.e., passive components, gate drivers, sensors and EMI filters). Customized for power module design, the corner stitching [24] data structure with constraint graph [29] evaluation has been extended from traditional VLSI tools. Both design and reliability constraints are considered in this version to generate robust and optimized layouts ready for tape out.

### 2.1 Data structures

The corner stitching data structure uses non-overlapping tiles to represent a Manhattan layout. In general, there are two types of tiles: empty and solid. This is a planar structure, which can have two orientations: horizontal and vertical. In the horizontal (vertical) corner-stitched plane, all tiles are horizontally (vertically) maximized. Each tile is stitched with its neighbor by four pointers: east, west, north, and south. Using these pointers a plane can easily be traversed. However, some basic functions (i.e., splitting, merging, insertion) are modified and adjusted for the difference in between power electronics and VLSI design considerations. Two constraint graphs (CG) are created from the corresponding corner-stitched plane: horizontal constraint graph (HCG) and vertical constraint graph (VCG) to maintain relative location among components along the X and Y axis, respectively. Each rectangular tile is mapped into the constraint graph by two vertices and an edge with minimum constraint value as the weight. So, for each corner-stitched plane, two weighted directed acyclic graphs (DAG) are generated by one-to-one mapping of the constraints.

### 2.2 Design constraints

For power module design, a basic requirement is manufacturability. This leads to the design rule checking (DRC) process. However, power modules are also subject to reliability related constraints. These time-related constraints must be considered during the design phase to ensure a long-lasting product. At this time, there are no industry-standard reliability models mapping a target lifespan with a certain value in component spacing and trace width. Therefore, PowerSynth optimizes layout for reliability in two ways. First is to process reliability constraints during the initial input and enforce it in the layout optimization process. This approach is implemented in the layout engine itself. The other way is strengthening the design during the post-layout optimization process.

In this work, the reliability constraints are treated the same way as electrical constraints, since the aging and time-driven impacts on the layout are equivalent to voltage and current-induced impacts. For example, to ensure a longer design lifetime, designers must ensure a certain trace spacing during the design process and leave an engineering margin, depending on how long the target life time is or how accurate the predictive reliability model is. This effectively is the same as ensuring a lower E-field in the insulation material. On the other hand, electro-migration issues are mostly introduced with high-current density on traces, especially at corners. To lower the possibility of a stuck-open fault, designers can only leave a design margin, which is effectively the same as limiting the current density. Therefore, in this work, high voltage, high electrical field, and high current density design constraints are all treated as reliability constraints because of the similar impacts on layouts.

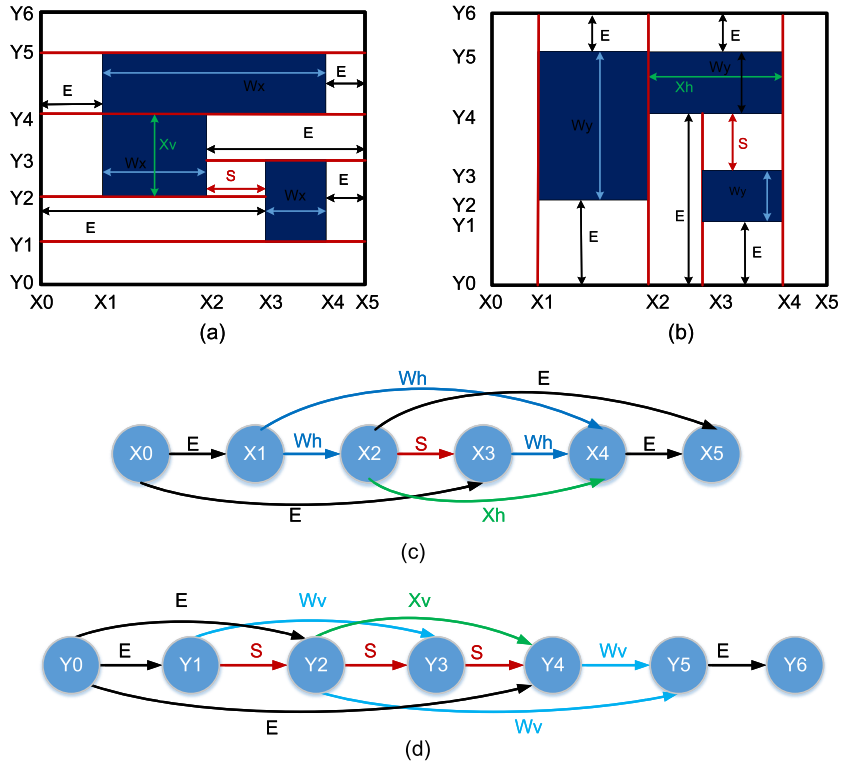


**Fig. 2.** Design constraints from (a) horizontal or (b) vertical corner-stitched plane and corresponding (c) HCG and (d) VCG.

In the current version, the following constraints are honored in the layout engine:

**Design Constraints**: These constraints are common technology constraints from the manufacturer. Such as minimum width of a component, minimum spacing between two components, minimum enclosure of one component to another, etc.

**Reliability Constraints**: For high voltage-current power modules, the spacing between two different voltage levels needs to be designed carefully to minimize the reliability issues such as partial discharge (PD), field focusing, current crowding, etc. In the updated layout engine, voltage-dependent minimum spacing and current-dependent minimum width have been considered. An example of different constraints and corresponding constraint graph is shown in Fig. 2.

A power module layout solution is generated by evaluating constraint graphs. In VLSI, constraint graphs are evaluated for floorplan compaction only. However, power electronics layout solutions are optimized not only by compaction but also by expansion to address the reliability issues. Therefore, in the constraint-aware layout engine, there are four different operating modes for layout generation. While evaluating a CG, if there are multiple edges in between the same pair of vertices the edge with higher weight dominates. So, if there are both design and reliability constraint between the same pair of vertices, the larger constraint value is considered in the evaluation.

### 2.2.1 Detailed reliability constraints

The basic reliability constraint values [1] cannot guarantee a detailed consideration of the voltage waveforms in power electronics. Most of the time, the voltage value is simply the highest voltage on that component. This results in non-optimum solutions in real-world applications. One example is the multi-phase converter. Neighboring traces with voltage synchronized but with a phase difference will result in a smaller voltage difference which cannot be captured by their maximum voltages. Even for sub-circuits with the same phase, a single voltage value could not cover all possible scenarios. For example, to find the maximum spacing between AC OUT trace and DC+ trace, AC OUT voltage should be considered at 0 V, which failed to find the maximum spacing between AC OUT and DC-, as DC- is always at 0 V. Therefore, single voltage level is not sufficient to represent all scenarios.

Therefore, detailed reliability constraints will require user to provide more information about dif-

**Table I.** Voltage Difference Calculation Formula.

| Waveform | Sync | Average Case | Worst Case |
|---|---|---|---|
| DC-DC/AC | - | $\|A_1 - A_2\| + \|B_2\|$ | $\|A_1 - A_2\| + \|B_2\|$ |
| AC-AC $f_1 = f_2$ | $\theta_1 = \theta_2$ | $\|A_1 - A_2\| + \|B_1 - B_2\|$ | $\|A_1 - A_2\| + \|B_1\| + \|B_2\|$ |
| | $\theta_1 \neq \theta_2$ | $\|A_1 - A_2\| + \sqrt{{B_1}^2 + {B_2}^2 - 2B_1B_2cos(\theta_1 - \theta_2)}$ | |
| AC-AC | $f_1 \neq f_2$ | $\|A_1 - A_2\| + \|B_1\| + \|B_2\|$ | |

**Table II.** A Summary of Various Modes for Layout Generation.

| Mode | Solution Type | Evaluation Criteria |
|---|---|---|
| 0 | Minimum-sized | Minimum constraint values are used only |
| 1 | Variable-sized | All edge weights are randomized within an arbitrary range |
| 2 | Fixed-sized | Edge weights are randomized within bounded range |
| 3 | Fixed-sized with fixed component | |

ferent frequency components and their corresponding peak values and phase information. Since most of the switching components are synchronized based on the gate driver control signals, however, there are still some on-package signals which may be asynchronous, such as sensors and digital logic. To capture all possible combinations and eventually all maximum spacings, in this work, each net voltage is considered as sinusoidal waveform, which enables to represent both minimum and maximum voltage level for each net. The phase difference is also taken into account to find the voltage difference between two nets.

While determining the voltage difference between two traces, two cases are considered: the average case and the worst case. Formulas regarding voltage difference calculation are shown in Table I. Here, two signals are expressed as $y_1 = A_1 + B_1 sin(2\pi f_1 t + \theta_1)$ and $y_2 = A_2 + B_2 sin(2\pi f_2 t + \theta_2)$, where $A_1$, $A_2$ are DC magnitudes, $B_1$, $B_2$ are AC magnitudes, $f_1$, $f_2$ are frequencies, and $\theta_1$, $\theta_2$ are phase angles. For the average case voltage difference, two sinusoids are considered to be perfectly synchronized. However, for the worst case, the maximum possible difference between two independent waveforms are considered if they are out-of-sync.

## 2.3 DRC-aware layout generation

Efficient, generic, and scalable algorithms are developed for each mode of operation. Detailed algorithms can be found in [1].

**Minimum-sized layout**: In this mode, the constraint graph with minimum constraint values as edge weights are evaluated using the longest path algorithm. The vertices are sorted in topological order and incremental locations from the source vertex to the rest of the vertices are determined through the longest path. The maximum distance of each vertex from the source vertex is defined as the minimum location of that vertex. The time complexity of this algorithm is known to be linear with the number of edges in the graph.

**Variable-sized layout**: HCG and VCG weights are varied randomly within an arbitrary range. Randomization produces different sets of edge weights as well as different floorplan size. The pseudocode for this mode of operation is shown in Algorithm 1. In this mode, users can generate an arbitrary number of layout solutions. All solutions are guaranteed to be "DRC-clean" referring to the fact that no design-rule-check violations are present.

**Fixed-sized layout with pre-defined components**: For the fixed floorplan layout generation mode, only the floorplan size is specified. Whereas for the other case, the floorplan size, along with any component locations, can be set by the user. Both of these cases are handled by the same algorithms. Before constraint graph evaluation, the source vertex and sink vertex of the graph has a fixed location

**Algorithm 1:** The top-level algorithm for layout generation

```
Input: Constraint Graph (G), No. of desired solutions (N),
Output: DRC-clean layout solutions
Create corner stitch data structure
Create constraint graph form corner stitch
Evaluate minimum-sized layout using longest path algorithm
for i in length(N) do
    foreach edge in G do
        RandomizeEdgeWeight(min,max,mean,std)
    LocationEval(G)
/* min:  minimum constraint value                    */
/* mean:  average of mean and max                    */
/* std:  standard deviation ≈ min                    */
/* max:  const.  × min                               */
```

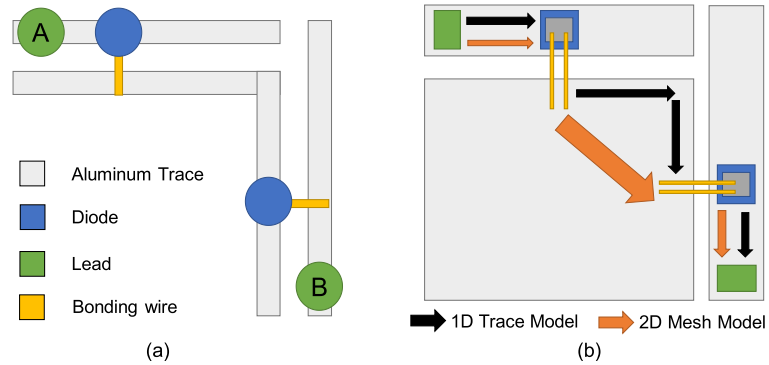


**Fig. 3.** A design example with (a) symbolic layout representation and (b) electrical model.

and some intermediate vertices may have a fixed location as well. Therefore, the edge weights are randomized within a calculated range. The simplified version of the layout generation algorithm is shown in Algorithm 1.

## 3. Electrical model

In the previous version of PowerSynth [9], the first-order linear approximation technique through the Laplacian matrix model has been used to quickly estimate the loop parasitic value during layout optimization. However, this methodology has two limitations of not accounting for current density or mutual coupling. Thus, it is not accurate for some 2D layouts with planar traces. For example, given the layout in Fig. 3, due to the use of a symbolic layout representation that does not consider current density for a 2D planar structure, the current from A to B follows the horizontal and vertical lines instead of diagonally on the 2D plane. This would result in an overestimated extraction of loop inductance due to consideration of a larger loop area. Besides the current density consideration, not accounting for mutual coupling between traces will give the same loop inductance result for the two loops with the same total length using a linear approximation model without considering the layout impact.

Most limitations coming from the previous electrical extraction model in PowerSynth can be addressed using a PEEC-based model using a mesh structure. The detailed equations are summarized in [18]. The main difference in terms of electrical model is their provided features. First, the 1D model assumes a uniform current density over the entire cross-section of the trace with some correction factors for the skin effect. It cannot be used to model the actual current distribution over the entire design layout thus not suitable reliability optimization for current-crowding and electro-migration problems. Second, being a wire-based model, it lacks enough mesh node on the layout to model the

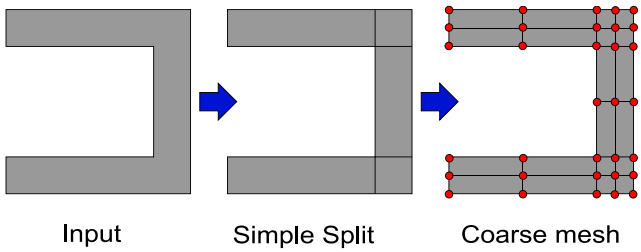


**Fig. 4.** Adaptive mesh generation for electrical modeling.

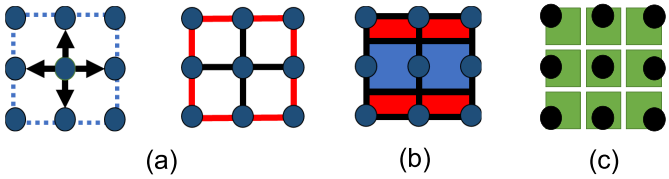


**Fig. 5.** (a) Node and edge formulation with extraction cells for (b) resistance and inductance and (c) capacitance.

E-field distribution, thus not suitable for high-voltage reliability optimization and breakdown analysis. Third, its accuracy is also negatively affected because of lacking detailed current and voltage distribution. Finally, the previous 1D model did not consider mutual inductance coupling between wires. Though this can be potentially added to the 1D model, a generalized equation for mutual coupling is hard to derive for large power traces without meshing the traces into smaller filaments.

In the new version of PowerSynth, we introduced a new PEEC-based distributed electrical model combined with a coarse mesh derived from the corner stitch data structure from the new layout engine. Since the PEEC model computation is time-consuming, we use a new meshing algorithm to accelerate the layout optimization process. It is based on the corner-stitch data structure from the layout engine and generates a coarse layout mesh in linear time complexity. Since PowerSynth is not targeting the accuracy level needed for sign-off verification, which is mostly performed through FEM extraction, the extraction accuracy with coarse mesh suffices for design planning phase. We further optimized our codebase to convert and compile the model in C programming language, which enables a fast and accurate layout optimization for high-voltage and high-current reliability consideration and signal integrity optimization.

### 3.1 Methodology

First, to capture the current density distribution, a coarse mesh is generated for any layout. Then, the loop parasitics of most planar 2D layout structures can be evaluated. This would support most 2D layouts from the above-mentioned new layout engine. The model takes layout input through a planar data structure, where each plane is a rectangular object with thickness and elevation. As seen in Fig. 4, based on the shared edges between input traces, an algorithm is used to perform a simple geometrical split, where each new trace always has one shared edge with another. In such a way, a uniform mesh (N x N) can then be applied to all planes and form a coarse mesh. The node and edge-forming process are illustrated in Fig. 5(a). To begin with, all mesh nodes are separated into two groups: internal or boundary, where the boundary nodes are nodes located on the trace group perimeter. During this process, each node is assigned to a unique node index and connected with its North, South, East, and West neighbors through an edge object. This edge data structure stores the width and length information of each trace. These width and length values are assigned as follows: For each pair of nodes, an edge is defined as an internal edge if one internal node is presented. Otherwise, if both nodes are of boundary type, a boundary edge is defined. The widths of boundary edges are always smaller than those of internal edges, giving a good approximation for skin effect. These internal and boundary edges also serve as an input to evaluate capacitance cells located at each node. For every node, half of the edge-length to each of its neighbors is used to form a bounding box area as seen in Fig. 5(b).

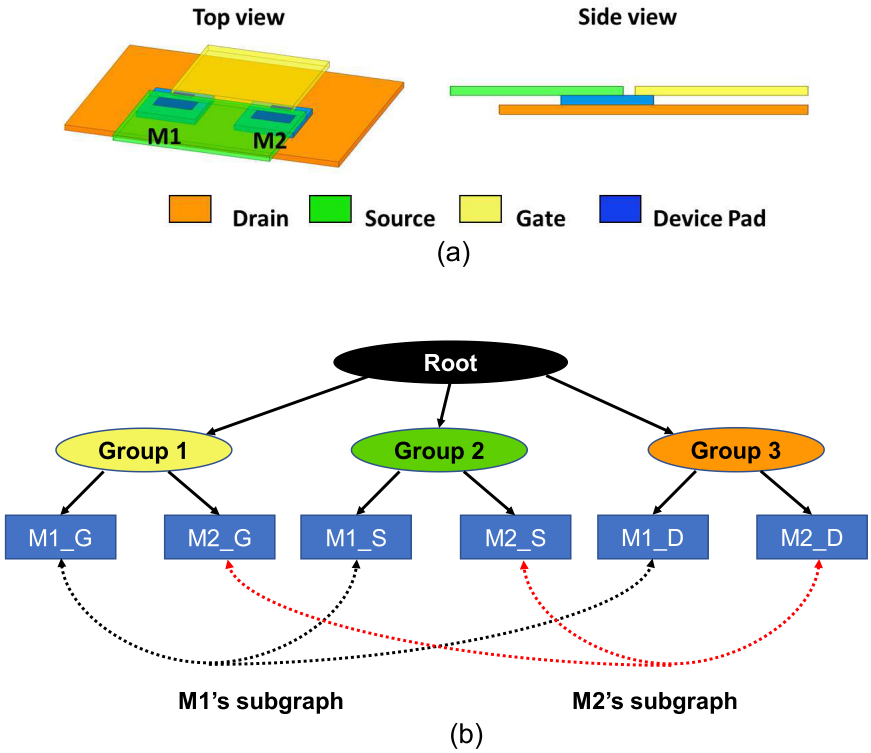


**Fig. 6.** (a) An example structure with (b) the hierarchical representation for extraction.

The response surface model described in [17] is then used to evaluate the self-parasitic values of every edge. The mutual inductance between every two edges can be evaluated using equations in [11]. When parasitic capacitance is included in the analysis for a full PEEC evaluation, and the layout has multiple layers, the capacitance cells are first created for both layers as described above. When an irregular mesh is applied for all trace groups, mesh nodes on two different layers are usually not aligned with each other. Hence, to compute the capacitance between two nodes in the z-direction, an algorithm will automatically find any overlapping region between two capacitance cells. This overlapping area along with the substrate thickness between two nodes is used to compute parasitic capacitance between them.

The layer-based approach has been used to handle multi-layer layouts. To handle the connection between device terminals and traces a hierarchical approach has been used. Figure 6 shows the hierarchical tree between two simple power MOSFETs and copper traces. This hierarchical representation has several advantages. First, the discretization for each trace island (tree node) can be performed individually to reduce the total number of meshes. Second, for layouts with multiple symmetrical structures, the parasitic value can be solved hierarchically to improve computational efficiency. Finally, most components can be handled through this method using multiple subgraphs. The internal parasitics between the terminals of the component can be represented through the edge weights.

Once all of the self and mutual parasitic values are evaluated, these values can be calculated using Eq. (1). There are five main matrices used in this evaluation: $\mathbf{G}+s\mathbf{C}$: the conductance and capacitance matrix; $\mathbf{A}$: adjacency matrix; $\mathbf{R}+s\mathbf{L}$: resistance and inductance matrix; $\mathbf{I_i}$: input current sources and $\mathbf{V_i}$: input voltage sources. As can be seen from Eq. (1), for the parasitic extraction application, normally R and L elements can be lumped into one single branch and stored in the (R+sL) matrix. This reduces the number of nodes significantly and improves the matrix evaluation time. Furthermore, this method provides no-voltage and no-current solutions through reorganization of the matrices into Eqs. (2) and (3). This can be used in different scenarios depending on the optimization objective to further reduce computational effort.

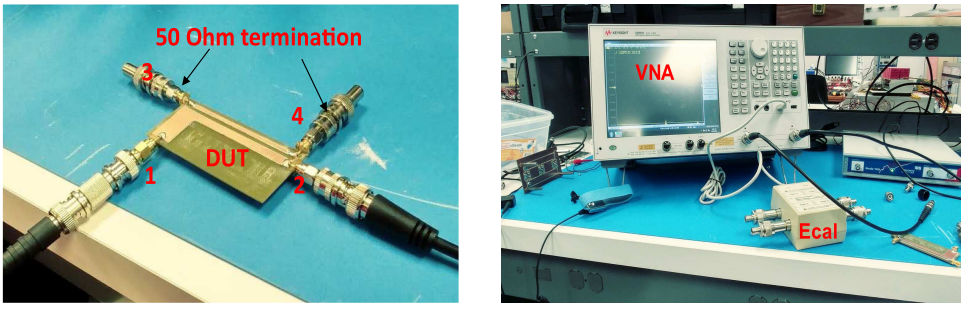


**Fig. 7.** (a) Fabricated test vehicle, (b) electrical model validation measurement setup.

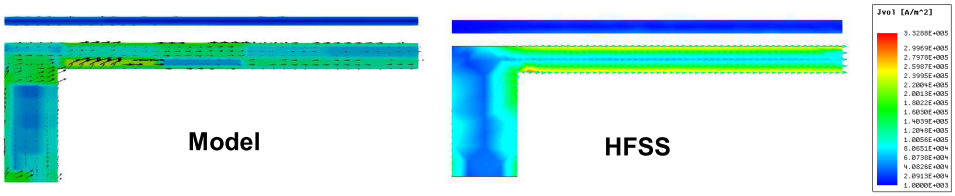


**Fig. 8.** Current density validation against ANSYS HFSS.

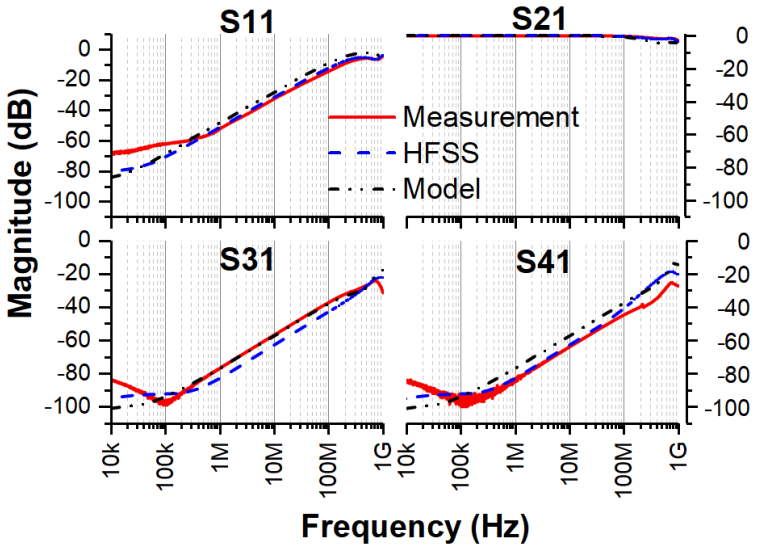


**Fig. 9.** S-parameter validation against HFSS and measurement.

$$\begin{bmatrix} \mathbf{G}+s\mathbf{C} & \mathbf{A} \\ \mathbf{A}^T & -(\mathbf{R}+s\mathbf{L}) \end{bmatrix} \begin{bmatrix} \mathbf{\Phi} \\ \mathbf{I} \end{bmatrix} = \begin{bmatrix} \mathbf{I_i} \\ \mathbf{V_i} \end{bmatrix} \tag{1}$$

$$[(\mathbf{G}+s\mathbf{C})+\mathbf{A}(\mathbf{R}+s\mathbf{L})\mathbf{A}^T]\mathbf{\Phi} = \mathbf{I_i} + \mathbf{A}(\mathbf{R}+s\mathbf{L})^{-1}\mathbf{V_i} \tag{2}$$

$$[(\mathbf{R}+s\mathbf{L})+\mathbf{A}^T(\mathbf{G}+s\mathbf{C})^{-1}\mathbf{A}]\mathbf{I} = -\mathbf{V_i} + \mathbf{A}^T(\mathbf{G}+s\mathbf{C})^{-1}\mathbf{I_i} \tag{3}$$

### 3.2 Experimental verification

To verify the model, a simple four-port PCB structure is designed and fabricated using 1 oz. copper on an FR-4 substrate. Four SMA connectors are used at the four ports of the PCB. The measurement setup for S-parameter extraction using a Keysight E5061B vector network analyzer (VNA) is shown in Fig. 7. A Keysight ECAL N4431B is used to perform the necessary two-port calibration. One port is excited at a time with the other ports terminated with individual 50 Ω loads. Six measurements

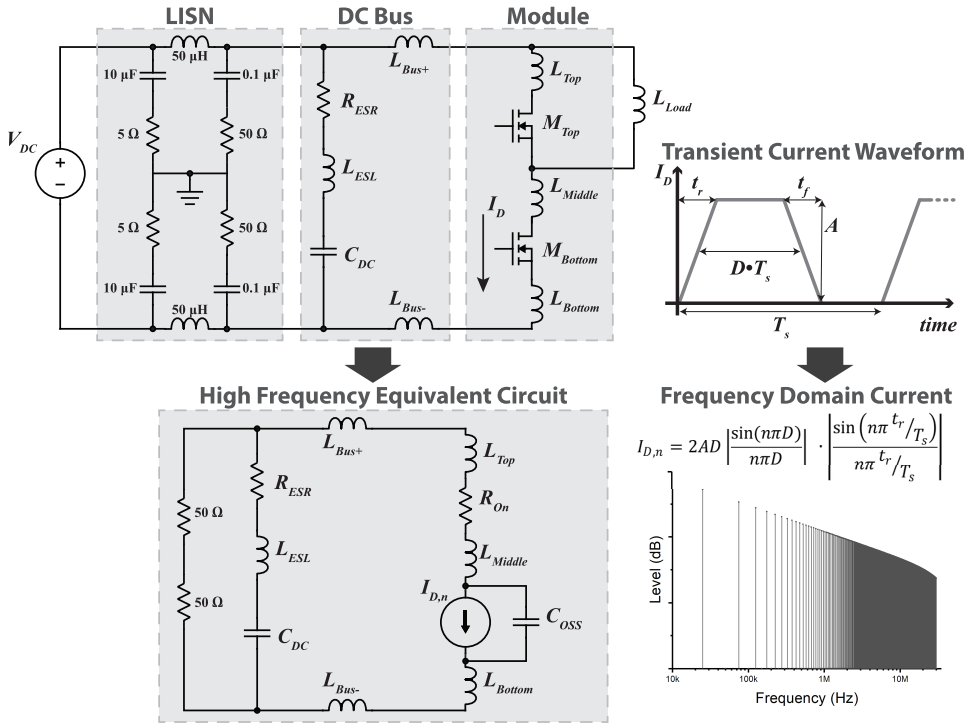


**Fig. 10.** High-frequency equivalent circuit for the differential mode (DM) EMI path of a converter system, along with the frequency domain representation of the switching noise source.

are carried out to collect all S-parameter data from 10 kHz to 1 GHz. To extract S-parameters from the model, an iterative process has been designed to sweep through a frequency range from 10 kHz to 1 GHz. At each frequency point, a full RCLM netlist is extracted from the model and evaluated in Synopsys HSPICE for S-parameter extraction. The simulated results are then converted to the touchstone format where the data can be easily accessed and plot using the MATLAB-RF toolbox. The same test structure is simulated in ANSYS HFSS, where four lumped-ports are connected to the structure, and S-parameter simulation is performed.

The current density map extracted from the model versus the result from ANSYS HFSS at 1 MHz is shown in Fig. 8. The current density results show very good agreement between the model and ANSYS HFSS and verify our 2D mesh model with current density prediction. Further, Fig. 9 shows the comparison between the new model, HFSS, and S-parameter measurements. The results show good agreement between three sets of data. The results between the model and HFSS match well with less than 3 dB absolute error for all frequencies. Measurement results show some noise in the frequency range less than 100 kHz. This is because the intermediate frequency of 3 kHz in the measurement setup only has a 75 dB dynamic range for the frequency range from 100 to 300 kHz. Also, the contact resistance between the solder and the SMA connector might also introduce some noise. However, the results fit very well in the high-frequency region (>100 kHz). This demonstrates the capabilities of the model allow it to accurately predict coupling between traces.

# 4. Conducted EMI modeling

## 4.1 EMI model formation

At present, PowerSynth excels at quickly optimizing power module layouts by minimizing device temperatures and electrical parasitics using reduced-order models as cost functions for each of these metrics. However, as the use of wide bandgap (WBG) devices in power modules increases, the greater $di/dt$ and $dv/dt$ that occur during the switching transients of these power semiconductors can lead to an increase in noise generation through both conducted and radiated emissions [23]. These high slew rates interact with layout parasitics, producing oscillations and overshoot conditions that manifest as electromagnetic interference (EMI). For these reasons, efforts to mitigate noise levels and help reduce

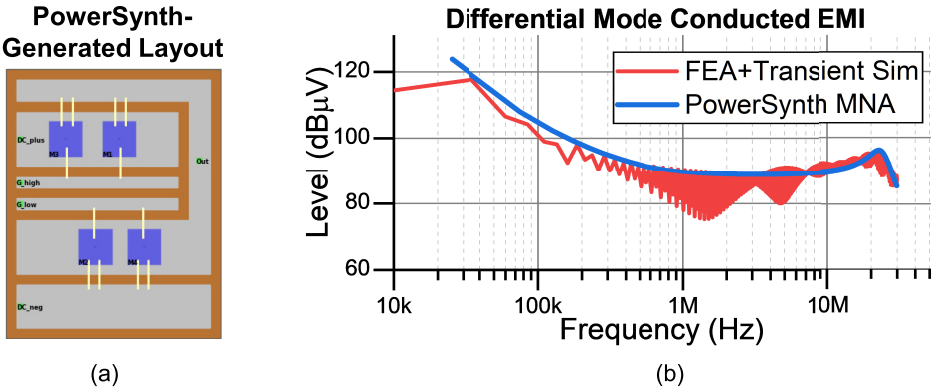


**Fig. 11.** (a) An example PowerSynth-generated layout and (b) DM noise model validation results.

filtering requirements through layout optimization in PowerSynth are currently being investigated. In the previous work, the extracted parasitic netlist is exported but conducted EMI results still rely on the designer to plug the netlist into an EMI testing environment and perform further simulations. Several important components for EMI testing such as LISN, device models, busbar models are not included in PowerSynth results. However, in this work, a dedicated EMI model is included with a noise distribution plot. Also, an exporting function to EMPro is included should user desire more detailed EMI analysis based on the S-parameters.

Initial studies into methodologies for modeling conducted EMI have focused on leveraging the existing parasitic extraction capabilities of PowerSynth. These layout parasitics are used in constructing high-frequency (HF) equivalent circuits for the differential mode (DM) and common mode (CM) noise propagation paths found in converter and inverter applications as put forth in [15]. To approximate the switching behavior of the power devices, they are represented as sources in the frequency domain by taking the Fourier transform of a trapezoidal waveform corresponding to the switching frequency, duty cycle, amplitude, and rise or fall time. The resulting circuit is then solved over the frequency range of interest using modified nodal analysis (MNA) [26] to yield a noise level prediction. Thus far, these techniques have been implemented in PowerSynth to evaluate the DM noise propagation path of module layouts. This is illustrated in Fig. 10 where a module layout is combined with the DC bus of the system and a line impedance stabilization network (LISN) to form a high frequency equivalent circuit for the DM propagation path. In this case, the setup reflects that of a double-pulse test where the low-side device is switching. This device is replaced by a current source representing the switching waveform in the frequency domain. Additionally, a capacitor is placed in parallel with this source to model the output capacitance, $C_{oss}$, of the device.

## 4.2 EMI model validation

To verify the results when using this method, a simulated conducted-EMI testbench has been established. In this setup, layouts generated by PowerSynth are first exported to commercial FEA software where an s-parameter model of the power module is determined by 3D full-wave analysis. Next, the S-parameter model is included in a transient circuit simulation of the complete system including load, DC bus, LISN and power supply. Switching devices are included in this simulation using physics-based SiC MOSFET models [19]. The FFT of the LISN voltage is finally used to compute the noise level generated by the module and system and compared with the results obtained from PowerSynth. For example, Fig. 11 shows a layout generated by PowerSynth and compares the results of the DM conducted EMI as calculated by the MNA solver in PowerSynth compared with the results of the FEA and transient circuit simulations. Here, this approximation method is shown to have good agreement with the envelope of the DM noise level found via the simulated EMI testbench. In addition, these models can be extended to model CM noise as well [10]. This methodology is quite fast when compared with the multiple steps and computation time associated with the simulated testbench. However, it is currently not suitable for use in a layout optimization loop. Further development is ongoing to

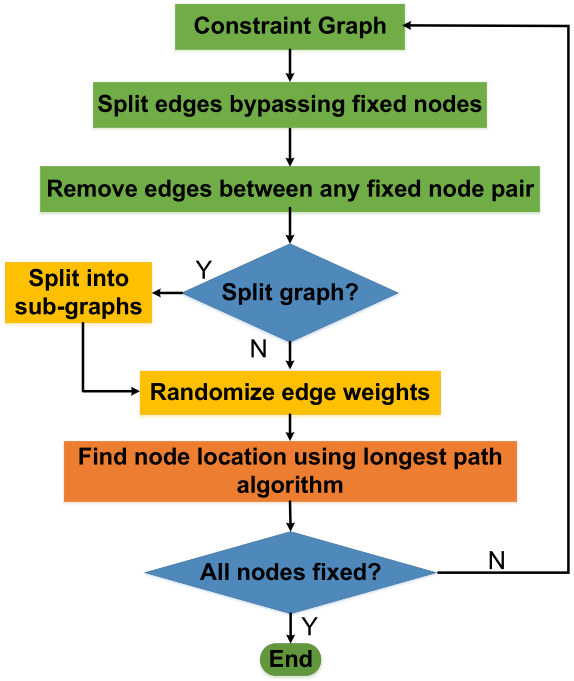


**Fig. 12.** The flowchart of layout generation with fixed sizes or locations.

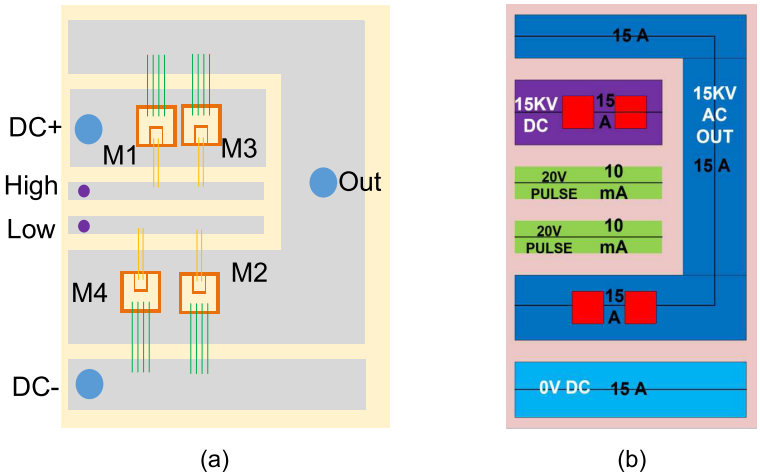


**Fig. 13.** (a) An example half-bridge power module and (b) the I-V loading.

reduce the evaluation time by modeling the transfer functions associated with the CM and DM HF equivalent circuits. These endeavors are continuing in order to establish metrics and cost functions for optimization that will enable PowerSynth to better produce layouts less prone to generating noise and more likely to pass EMC qualification with fewer design iterations.

## 5. Layout optimization for reliability

### 5.1 Basic reliability consideration

For the sample power module layout shown in Fig. 13(a), and corresponding I-V loading is shown in Fig. 13(b), two minimum-sized layouts are generated: one with design constraints only (Fig. 14(a)) and another with both design and reliability constraints (Fig. 14(b)).

When determining the voltage difference between two traces, the worst case is considered. For example, the gap between 15 kV DC trace and AC OUT trace is set by 15 kV voltage difference (0 V AC to 15 kV DC). Applying the proposed algorithms, two different solution sets are generated. For the first layout set, a fixed trace-to-trace distance of 0.2 mm is considered. This layout set represents the minimum manufacturable requirements with design constraints only. In the second data set,

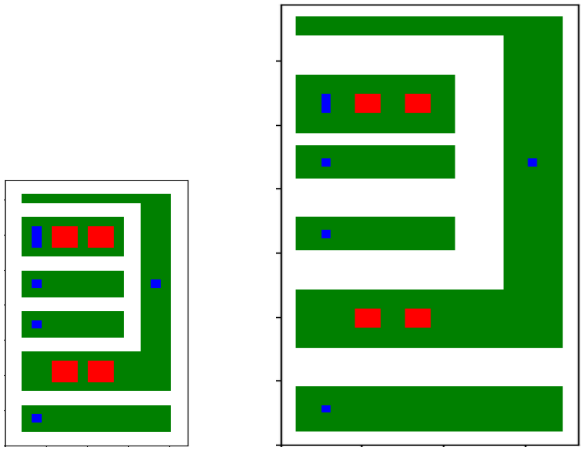


**Fig. 14.** Auto-generated minimum-sized (Mode 0) solution: (a) with only design constraints and (b) with reliability constraints. The dimensions are $22.22 \times 37.77$ and $36.6 \times 68.8$ mm$^2$, respectively.

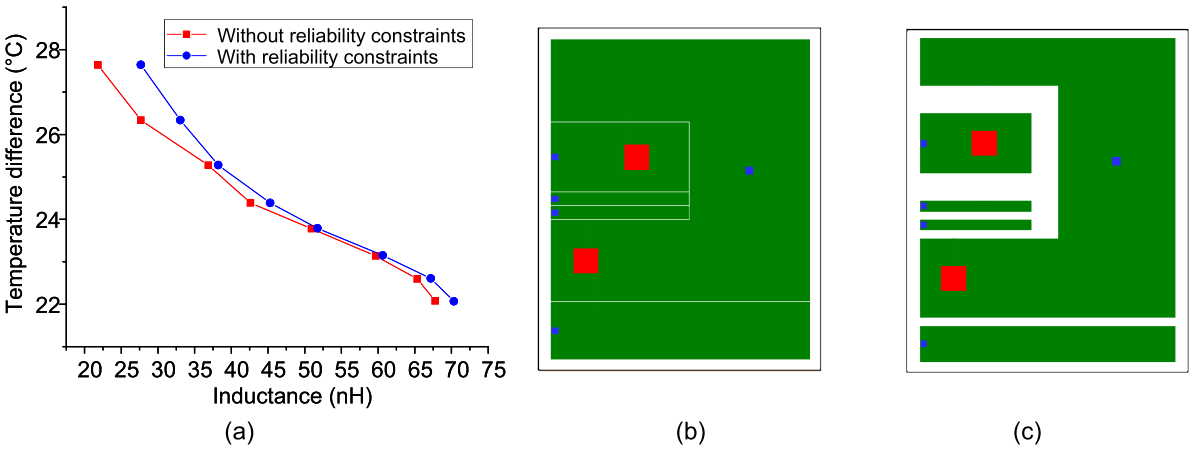


**Fig. 15.** (a) Mode 2 Layout optimization results with a fixed dimension of $45 \times 55$ mm$^2$. Optimized example solutions: (b) with only design constraints and (c) with basic reliability constraints.

both design as well as reliability constraints are considered. Here, trace-to-trace distance is varied according to the voltage difference between traces, while trace widths are varied depending on current rating. The min trace width is set to be 2 mm for 1 A of current and 3 mm for 20 A. In each case, 1000 candidate solutions with varying floorplan sizes from 2475 mm$^2$ to 9000 mm$^2$ are generated, and PowerSynth electrical and thermal models [9] are applied to evaluate the maximum temperature as well as the loop inductance for each layout. Two different Pareto-frontiers for the corresponding data sets are shown in Fig. 15(a). The results from the data sets illustrate expected relationships between inductance, temperature, and layout area. Inductance increases due to a larger conduction loop while temperature decreases with the increased layout area. Due to the smallest fixed gap of 0.2 mm, the first layout set has better performance results in terms of nominal I-V ratings. However, the second Pareto-front shows the tradeoff between inductance and temperature under higher I-V rating consideration. Two selected sample layout solutions with minimum inductance values from two data sets are shown in Figs. 15(b) and (c), respectively.

## 5.2 Detailed reliability consideration

Since the basic consideration only uses a single amplitude value, the constraints between the gates of the high-side transistor and low-side transistor are not correctly computed, resulting in a small gap between those traces. With our detailed constraint models, two different solution sets are generated.

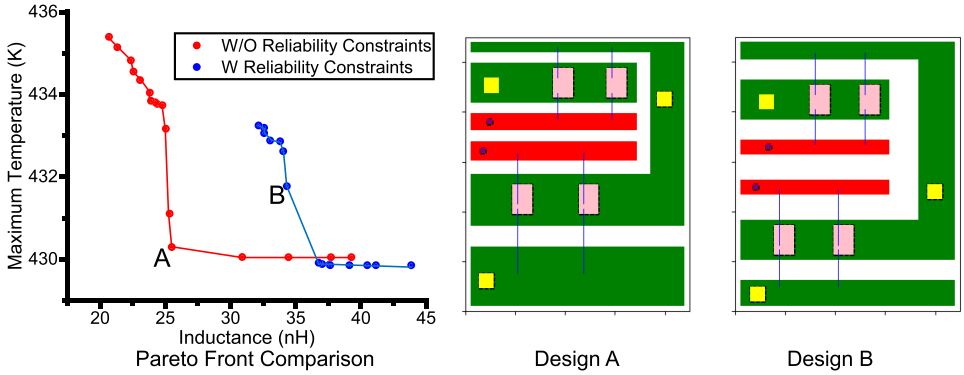


**Fig. 16.** Two Pareto-Fronts generated in Mode 2 with a fixed size of $45 \times 55\text{mm}^2$. Comparison is made between layouts with or without detailed reliability constraints.

For the first layout set, a fixed trace-to-trace distance of 2 mm is considered. This layout set represents the minimum manufacturable requirements with design constraints only. In the second data set, both design as well as reliability constraints are considered. Here, trace-to-trace distance is varied according to the voltage difference between traces and width of the traces are varied depending on the corresponding current rating. The min trace width is set to be 2 mm with 1 A maximum current and 3.5 mm with 15 A maximum current rating. In each case, 1000 candidate solutions with floorplan size of 2475 $\text{mm}^2$ are generated and PowerSynth electrical and thermal models are applied to evaluate the maximum temperature as well as the loop inductance for each layout.

Two different Pareto-frontiers for the corresponding data sets are shown in Fig. 16. The results from the data sets illustrate expected relationships between inductance and temperature. Inductance increases due to a larger conduction loop while temperature decreases with the decreased density. Due to the fixed gap of 2 mm, the first layout set has the better performance results in terms of nominal I-V ratings. However, the second Pareto-front shows the tradeoff between inductance and temperature under higher I-V rating considerations. Two selected sample layouts (A and B) with minimum inductance values are extracted from the Pareto front for comparison, as shown in Fig. 16.

Clearly shown from the results, the high-voltage/high-current reliability constraints will significantly push the Pareto front away. This impact mainly affects low-inductance layouts, since those designs generally have tighter spacing between traces and components. On the other hand, thermally-optimized layouts are less affected simply because spacing constraints are relaxed. However, even if the thermal optimization is highly coupled with mechanical reliability considerations, a designer cannot simply choose a low-temperature solution and assume the trace gaps are sufficient for high-voltage operation. An optimization algorithm without detailed reliability consideration cannot guarantee the electrical reliability since the temperature is a global effect while the electrical reliability is more limited to local patterns. Therefore, even though the Pareto fronts for temperature-optimized solutions look the same with or without reliability considerations, the actual designs on the Pareto front may vary. Without reliability constraints, the thermally-optimized solution may prefer designs with larger spacing between devices, while larger trace gap may be more critical with high I-V constraints.

## 6. Post-layout reliability optimization

### 6.1 E-field focusing and current crowding

In power modules, it has been observed that electric field concentrates at edges of traces and corners, especially at the triple point of a DBC metallization. This is confirmed in Fig. 17 for the case of a switching leg on DBC using ANSYS Maxwell. It is also seen that chamfering or filleting the corner reduces the E-field in that region to about half. Charge density also reduces as fillets are applied. Equations. (4) and (5) can be used to model the filleting impact on E-field distribution. This is in accordance with theoretical predictions of E-field and charge density in the vicinity of a sharp corner as described in [14], where $\sigma, E, \rho, \beta$ are the surface charge density, electric field, distance from the corner, and opening angle of the corner, respectively and $C_1$ and $C_2$ are two fitting constants.

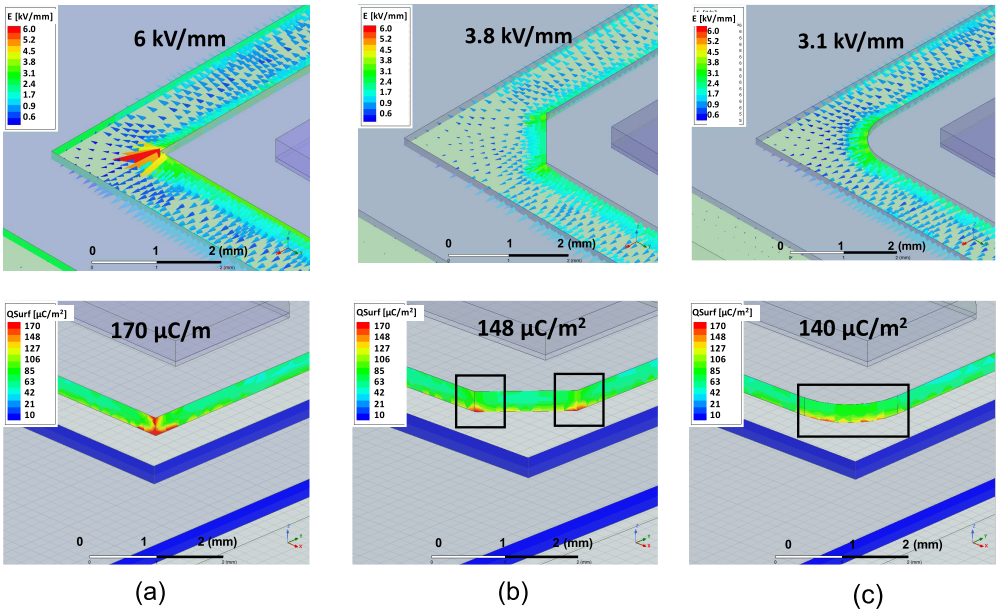


**Fig. 17.** E-field distribution (top) and surface charge (bottom) comparison with a (a) 90° corner, (b) chamfered corner, and (c) filleted corner.

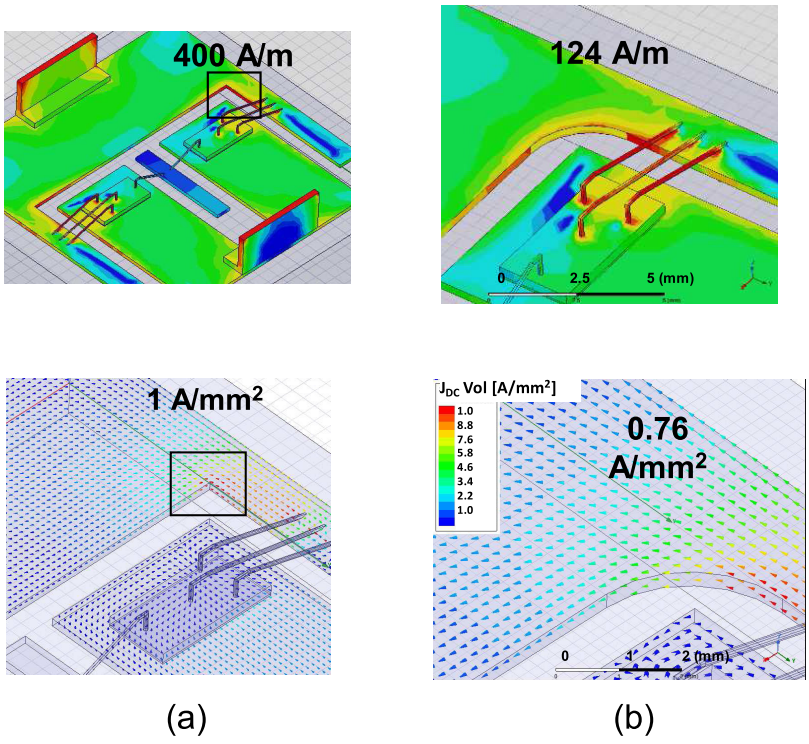


**Fig. 18.** Surface (top) and volume (bottom) current density comparison between (a) the original layout with sharp corners and (b) optimized layout with filleted corners.

E-field is calculated and compared to 2D simulations. The results are within 17% of each other. Further simulations to compare the degree of filleting and trace gap were conducted. While filleting offered a significant benefit in E-field reduction, the degree of filleting did not have as much impact.

$$\sigma(\rho) = \frac{E_\phi(\rho, 0)}{4\pi} \cong -\frac{C_1}{4\beta}\rho^{(\frac{\pi}{\beta}-1)} \tag{4}$$

$$E = -\frac{C_2\pi}{\beta}\rho^{(\frac{\pi}{\beta}-1)} \tag{5}$$

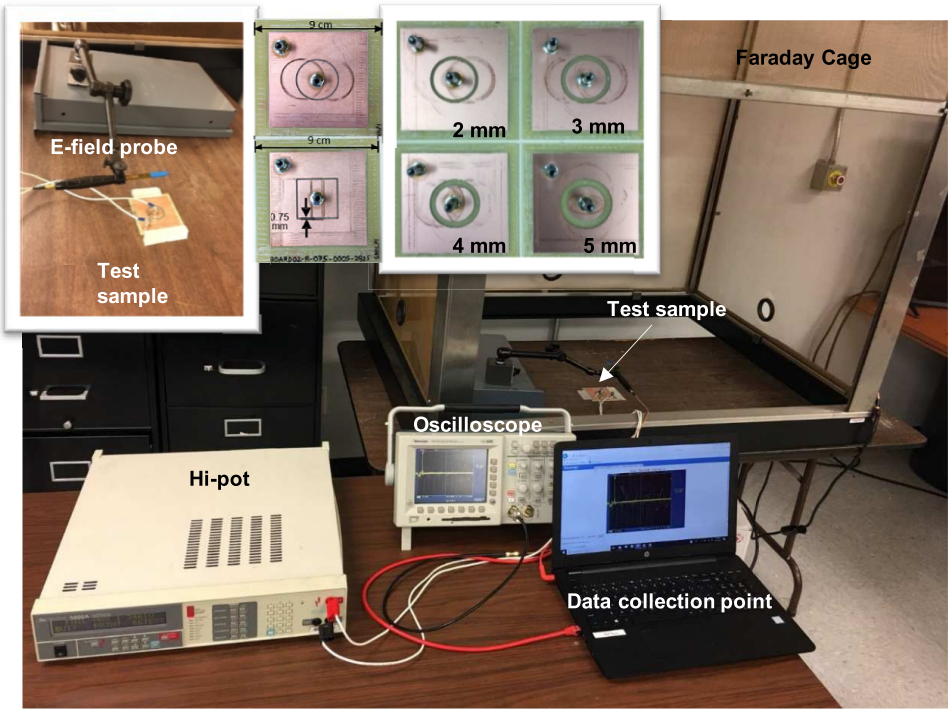


**Fig. 19.** Test setup with close-up shots of the E-field probe and some test samples.

**Table III.** Breakdown Voltage Measurement Results from Hipot Testing.

| Samples | Trace Spacing (mm) | | | | |
|---|---|---|---|---|---|
| | 0.25 | 0.5 | 0.75 | 1 | 1.25 |
| Square | 1021 | 1263 | 1400 | 1465 | 1712 |
| Circular | 1360 | 1435 | 1475 | 1757 | 2200 |
| Δ (%) | 33 | 14 | 5 | 20 | 29 |

Another detrimental effect of keeping sharp corners is current crowding. High current density can cause Joule heating of the conductor, exacerbating electro-migration and making the placement of nearby devices difficult. Migration issues were found in sintered-silver die attaches operating at high temperatures [4, 25]. FEA simulations showed current crowding at corners reduced to less than a third of the original value when fillets were used (Fig. 18). With increasing layout density, it is imperative to consider partial discharge and current crowding effects. Further experimentation would be needed to determine spacing rules for various voltage levels.

## 6.2 Breakdown voltage testing

To validate our assumption, test samples were fabricated on an FR4 substrate to gauge the effect of sharp corners and fillets on breakdown voltage for various trace gaps. They are designed with various trace spacings as shown in Fig 19. Square trace gaps are compared to circular trace gaps to assess the impact of having corners. A hi-pot was used for these experiments along with E-field probes. The breakdown voltage data are summarized in Table III.

The experiments thus showed about a 20% increase in breakdown voltage going from a trace with corners to one without. This means power modules with filleted corners can have better voltage safety margins. Further experimentation is required to analyze partial discharges at the advent of breakdown for power modules on DBC. Partial discharge is a "localized electrical discharge that only partially bridges the insulation between conductors and which may or may not occur adjacent to a conductor" [13]. Based on partial discharge experiments, a more informed filleting strategy may be implemented in the EDA tool.

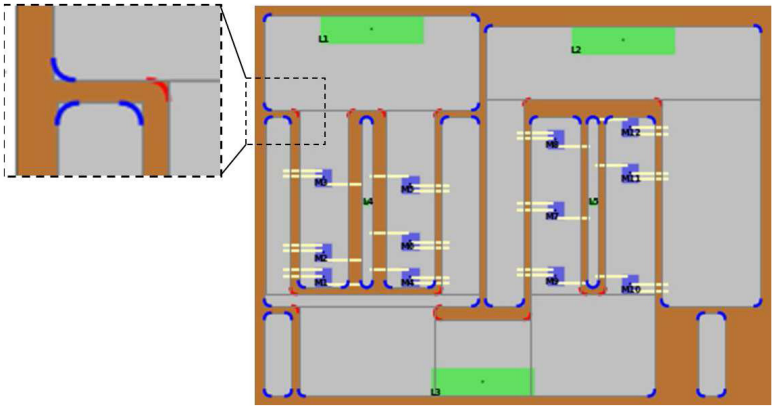

**Fig. 20.** Post-layout optimization with filleted sharp corners.

### 6.3 Post-layout optimization

The final power module generated in PowerSynth is exported to FEA tools and rendered in 3D. However, the sharp corners on the metallization are retained. Typically, for fabrication, sharp corners in the metallization of a direct bond copper (DBC) substrate are filleted with a radius of 2 to 4 mm applied. This rule-of-thumb was codified in PowerSynth as a post-layout optimization feature of the final layout. Detailed results can be found in [20]. Figure 20 shows an example of a final layout generated by PowerSynth and the assignment of appropriately sized fillets at sharp corners. For traces that are very narrow, such as gate traces, fillets need to be sized accordingly. Some of these fillets are highlighted. The main reason for filleting sharp outer corners (blue) is to reduce electric field focusing and the likelihood of mechanical delamination. Filleting inner corners (red) reduces current crowding.

## 7. Conclusions and future work

PowerSynth has been extended in various aspects to design the next-generation high-density 3D power modules. Both the layout engine and updated models are capable of optimizing heterogeneous components with high design flexibility. The constraint-aware layout engine with the layout generation algorithms can process a variety of DRC-clean layouts through a generic approach. The mesh-based electrical model improves accuracy and provides current density modeling in complicated layouts. Integration with EMI models further enhance the design process by combining signal integrity and noise reduction with layout design. Post-layout optimization with filleting also improves reliability and alleviate E-field focusing and current-crowding issues. Further, extending to 3D layouts and integrating heterogeneous components can bring the latest innovative devices and components into physical designs with a significant reduction in time-to-market and man-power costs.

The continuous development aims to demonstrate the entire PowerSynth-based design flow through fabricating an optimized power module and validating electrical and thermal performance using experimental measurements. These efforts can provide the power electronics society with application notes, tutorials, and reference designs of how to integrate PowerSynth into their workflows.

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