Electronic Design Automation (EDA) Tools and Considerations for Electro-Thermo-Mechanical Co-Design of High Voltage Power Modules

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***Abstract*— Recent developments in EDA tools for power electronics modules have led to simultaneous analysis and optimization of package features with regard to electro-thermal and thermo-mechanical aspects. In this work, two of these EDA tools, PowerSynth and ParaPower, are linked together with a software application programming interface (API) to rapidly explore a combined electro-thermo-mechanical design space and present the user with co-optimized solutions and tradeoffs in a fraction of the time consumed using traditional analysis methods. An overview of this co-design process and its advantages over that of the traditional, iterative approach is presented along with an explanation of the methods used by the respective tools for analysis. Finally, additional considerations and constraints are introduced that ensure manufacturing feasibility and reliable operation at high voltages. A case study in co-design using these tools has been proposed for the final paper.**

Keywords—design automation, co-design, design rules, electro-thermal, thermo-mechanical, power electronics, power semiconductor, packaging

I. Introduction

Recent advances in wide bandgap (WBG) power semiconductor devices have been driving development toward modules and packaging solutions with ever-increasing withstand voltage and power density [1]. WBG devices such as silicon carbide (SiC) can operate at higher switching speeds and frequencies, higher temperatures, and higher voltage levels than their silicon counterparts—potentially allowing for a reduction in system size by decreasing filtering and cooling requirements. Yet, the promise offered by incorporating WBG devices in power electronic systems is only realized when packaging and interconnection results in designs that effectively limit electrical parasitics and thermal coupling while ensuring feasibility and reliability. The traditional approach for designing power modules is iterative, time-consuming, and challenging, resulting in long design and prototyping phases [2,3]. However, new strategies in the simultaneous co-design of electrical, thermal, and mechanical aspects of power electronics packaging provide solutions aimed at reducing this development time with optimal results.

At the beginning of the design phase, a module designer might start with a given circuit topology from which a module layout is synthesized. From there one might focus on running finite element analysis (FEA) simulations on the layout to minimize electrical parasitics with the goal of reducing current and voltage overshoots during switching events—decreasing switching losses and electromagnetic interference (EMI). Next, thermal FEA might be employed to adjust the arrangement and spacing of the devices to minimize the thermal coupling among them. The designer may then choose to perform additional simulations that account for mechanical stress and strain when considering different material layers and their thicknesses. However, any changes made to one aspect of the design are likely to affect others as the electrical, thermal, and mechanical aspects of module design are conflicting with each other. For example, increasing the spacing among devices might result in decreased thermal coupling and lower junction temperatures at the expense of greater parasitic inductance due to increased loop area. This leads to a highly iterative design flow where each stage of the design process requires checking and re-evaluating every performance metric sequentially.

To overcome these challenges, several groups have turned toward automating these steps and begun incorporating multi-objective optimization strategies through the development of frameworks and EDA tools tailored to power module design [4]-[6]. More recently, other groups have focused on module layout optimization and parametric analysis using reduced-order modeling and accepting lower solution fidelity to rapidly explore a design space and quickly arrive at a starting-point solution. PowerSynth [7, 8] and ParaPower [9] are two such tools that take this approach and are currently under active development.

Critical to ensuring feasibility of module manufacturing, design rules are employed. Similar to a process design kit for integrated circuit design, power modules need a manufacturing design kit (MDK). Most module design rules are based on

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technology parameters such as minimum spacing required for complete etching. For example, the minimum gap between two traces is typically 0.5 mm since the chemical wet etching process does not allow for traces to be closer together. And while some rules are designed for manufacturing, others are needed for reliability, especially when operating voltages are higher than 1 kV where dielectric breakdown and partial discharge concerns begin to arise [10] - [12]. Although EDA tools incorporate basic parameters like trace gap spacing, few to none include rules that are a function of voltage and materials. PowerSynth is the first tool to determine and include these as design rules.

The key contribution of this work is as follows:

1. Efficient exploration of the co-design-space tradeoffs considering electrical, thermal, and mechanical aspects of power module design accomplished through the development of EDA tools,
2. An API for linking the two co-design tools to yield an EDA tool that is more comprehensive, and
3. Constraint-aware layout concepts and design rules accounting for voltage levels and material choices implemented with their application toward optimizing high voltage power module layouts.

In the first section of this paper, the two EDA tools are described and used in conjunction with one another to provide a comprehensive electro-thermo-mechanical co-design environment with the goal of optimizing high-voltage, high-density power module layouts, with appropriate design rules. In the next section, a case study is presented as an example for layout design optimization performed using PowerSynth and ParaPower.

II. Co-Design Methodology for Power Modules

A. EDA Tools Towards Co-Design

1) PowerSynth

Given an initial starting layout, PowerSynth is a standalone EDA tool that varies component positions and trace geometries to optimize toward tradeoffs in electrical and thermal performance metrics with candidate solutions presented to the user on a Pareto frontier. This is accomplished by using reduced-order thermal and electrical models within a multi-objective optimization loop. While some assumptions must be made when using these models—particularly the thermal one—they both return results orders of magnitude faster than FEA simulation and within about 10% accuracy to simulated and measured results [7]. Additionally, user-defined constraints and inputs allow for a full description of the module geometry, ensuring only feasible, manufacturable solutions are produced while preserving design goals. For example, a screen capture displaying the component selection and layout assignment portion of the PowerSynth GUI is shown in Fig. 1.

2) ParaPower

The US Army Research Laboratory is actively developing an open-source, fast, thermo-mechanical parametric analysis tool for the co-design of power electronics modules using MATLAB [9]. In contrast to PowerSynth, ParaPower is tailored

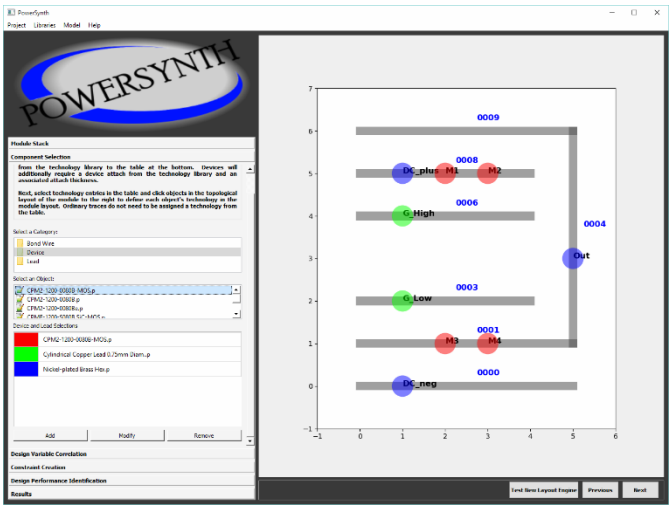


Fig. 1. PowerSynth component selection window.

toward more generalized thermal analysis that incorporates static or transient evaluation, stress estimation, support for phase change materials, and support for various boundary conditions. Additionally, by allowing for parameterization of a design geometry, using ParaPower allows for fast exploration of the thermo-mechanical design space. An example of a PowerSynth-generated layout entered in ParaPower is shown in Fig. 2.

3) API

While PowerSynth excels at quickly generating constraint-aware layouts and analyzing their electrical and thermal performance, as mentioned above, the PowerSynth thermal model does indeed make some assumptions that limit the range of boundary conditions possible and does not account for thermally-induced stress on the power module—whereas ParaPower can. Therefore, leveraging the thermo-mechanical analysis capabilities of ParaPower within the PowerSynth optimization routine leads to an API that combines layout-generation along with the electrical, thermal, and mechanical

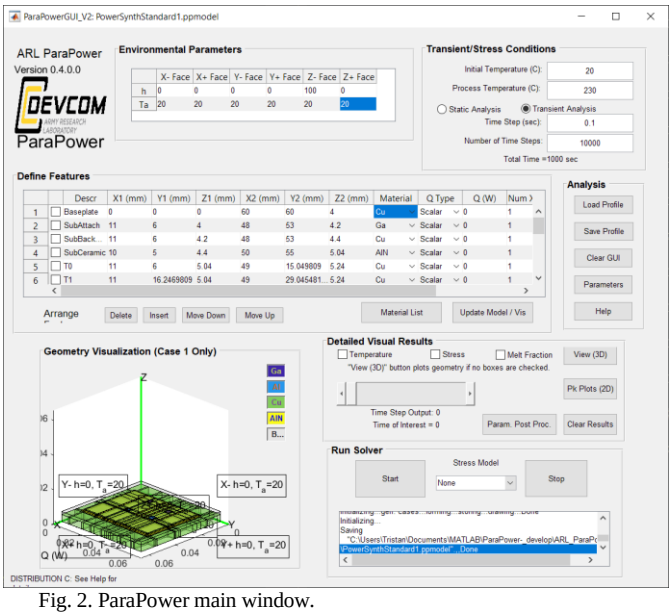


Fig. 2. ParaPower main window.

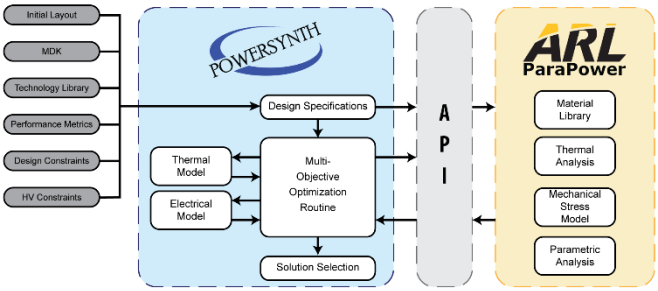


Fig. 3. Proposed electro-thermo-mechanical design flow using PowerSynth and ParaPower.

models of each respective tool. Fig. 3 illustrates this interaction between the two EDA tools. Currently the API provides bi-directional dataflow through PowerSynth. Here the user supplies the initial layout, MDK, technology library, and design constraints and provides performance metrics (such as loop inductance, maximum temperature, or maximum stress) to PowerSynth. Some of these input files and parameters are outlined in Section C while more detailed descriptions can be found in [7, 8]. During the multi-objective optimization routine, the API facilitates the transfer of layout geometry, components, and materials to ParaPower for the desired thermal analysis. Results of these analyses are then returned to the PowerSynth optimization routine through the API where PowerSynth then updates performance metrics for the current evaluation in real time.

B. *Performance Metrics and Models*

1) Electrical

As mentioned above, one of the critical design elements in MPCM to achieve high power density at high switching speed is electrical parasitics, especially parasitic inductance. In PowerSynth, the response surface method [13] and partial element equivalent circuit (PEEC) method [14], are used. An API is built within the tool where an adaptive meshing technique is applied to convert the corner-stitching data structure to equivalent RLC netlist efficiently. A simple Modified Nodal Analysis (MNA) solver is used to evaluate the parasitic loop inductance value. This model is much faster than using existing Finite Element Method (FEM) tools in a loop while maintaining similar accuracy. It aids the co-design and optimization process since it reduces the time needed to find the optimal solution set. Furthermore, parasitics extracted from the layout using this model can be converted to a netlist for further analysis. One example of this is shown in [15] where layout-specific EMI mitigation concepts are presented and evaluated using PowerSynth.

2) Thermomechanical

ParaPower thermal analysis is based on a 3D thermal resistance evaluation using the finite difference method allowing both static and transient evaluation of the power module layout [16]. To estimate the stress induced on these structures due to coefficient of thermal expansion mismatch, the ARL team has incorporated reduced order stress models within ParaPower [17]. Here individual layer stress is a function of the temperature difference between the current temperature of the structure and module processing temperature—the reflow temperature of the solder used and the zero-stress point. An example of these

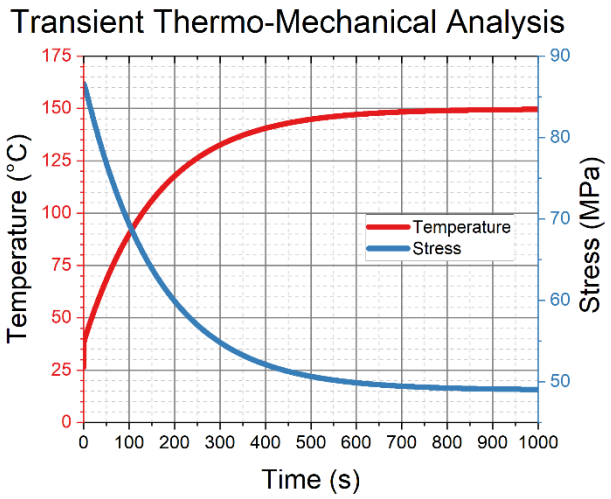


Fig. 4. Transient thermo-mechanical analysis in ParaPower.

transient results is shown in Fig. 4 and is obtained from the setup in Fig. 2.

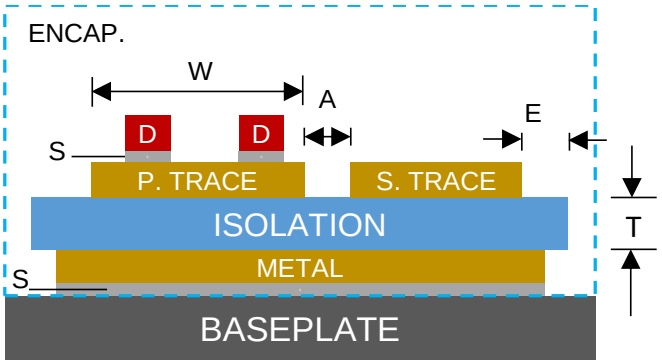
C. *Constraints and Reliability*

PowerSynth enables the user to specify design rules and constraints based on fabrication process parameters, much like a process design kit for integrated circuits, and specify rules based on reliability aspects. These rules are contained in the manufacturing design kit (MDK) that is specific to each customer based on their process parameters and operating conditions. The MDK comprises of a layer stack, a layout constraints list (design rules), that includes electrical reliability constraints (for high voltage and high current operation).

1) Layer Stack

The layer stack is a list of materials and dimensions that make up the power module going from bottom to top (Fig. 5). It is a text file containing the following fields: layer ID, name, material, thickness, length, width, and encapsulant. In the example shown (Fig. 5), the stack from bottom to top comprises of baseplate, substrate attach, bottom metal of the direct bond copper (DBC), the DBC ceramic (isolation), the top metal layer of the DBC (etched to form power traces and signal traces), device attach, and devices. The encapsulant may cover multiple layers and is thus specified for each layer that it covers. In Fig. 5, the encapsulant covers all layers except the baseplate.

Every material listed in the layer stack is indexed in a materials database that contains all the relevant properties of each material such as thermal conductivity, specific heat capacity, coefficient of thermal expansion, young's modulus, Poisson's ratio, density, electrical resistivity, relative permittivity, relative permeability, dielectric strength and ANSYS Q3D ID. Q3D ID is used at the time of export for automatic rebuilding of the 3D layout in ANSYS Electronics Desktop.



W: lateral width of trace
A: lateral trace gap
E: minimum enclosure
T: vertical thickness of a layer
D: device
P. trace: power trace; S. trace: signal trace
S: substrate attach or die attach

Fig. 5. Example layer stack for MDK.

The thickness of each layer affects the thermal resistance of that layer, which in turn affects the maximum die temperature of the module. The capacitance of traces is affected by the thickness of the isolation layer. Mutual inductance is impacted by this thickness as well.

2) Constraint-aware Layout and Design Rule Check

The 2D layout that is optimized in PowerSynth must adhere to design rules and thus go through a design rule check (DRC). These design rules are constraints that ensure the final module is manufacturable. Design parameters such as the minimum distance between two traces (dimension A in Fig. 5) and minimum width of a trace (dimension W in Fig. 5) are limited by the resolution of the wet etching profile of a DBC. Typically, this is 0.5 mm. The layout constraints file also contains information specifically about the minimum spacing between combination-pairs of the following: power traces, signal traces, bond wire pads, power leads, signal leads, and devices. It also contains specifications about the enclosure distance for each of the above. The enclosure distance is the distance from the element to the edge of the substrate (E in Fig. 5). The width and length of traces affect the loop inductance and loop resistance. A set of solutions (Fig. 6) show how inductance and temperature vary with varying terminal locations, dimensions of traces, and device proximity. In this solution set, PowerSynth randomizes the trace widths and lengths as long as they meet the minimum dimension and spacing requirements. Layout 2 is the most compact of the three yielding the lowest loop inductance, but relatively higher device temperature due to thermal coupling. Layouts 1 and 3 are other variants that yield corresponding inductance and temperature values.

3) High Voltage and High Current Constraints

With increased packaging density and higher voltage applications, electrical phenomena like partial discharge become a greater concern. Partial discharge (PD) is a localized electrical breakdown in an insulating material that may or may not bridge the gap between the conductors. PD deteriorates the insulation material making electrical breakdown more likely to occur at a lower voltage. In power modules, PD happens in the

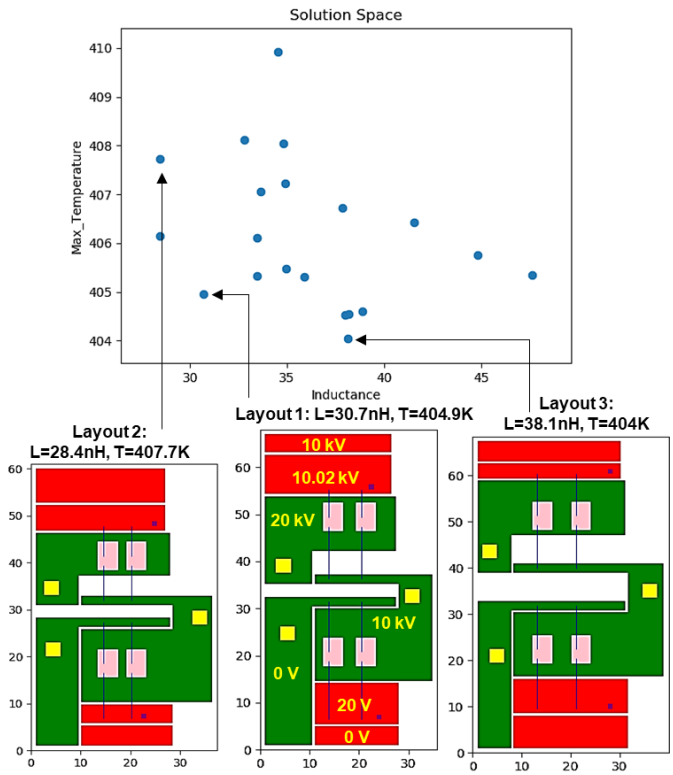


Fig. 6. Electro-thermal trade-off solution set with simple design rules (without reliability constraints)

encapsulant, between two traces, in the ceramic isolation between the two metal layers, and along surfaces (called surface tracking) between two leads. PD is initiated where there is an electrical stress that surpasses the dielectric strength of the insulator. This can occur in impurities or bubbles in the material where the relative permittivity changes, resulting in higher concentration of E-field, at points where conductors have sharp edges or corners, and at triple points where three different materials (one of them being a conductor) meet. In the case of a power module, this happens where the metal trace meets the ceramic and encapsulant. This critical point must be accounted for when developing rules for reliable layout designs.

To account for the above effect, a 2D model (Fig. 7) was simulated in ANSYS Maxwell and E-field was determined as a function of trace-gap, potential difference between traces, and the relative permittivity of the encapsulant. E-field follows an inverse power relationship with trace gap, with the coefficient and exponent depending on the potential difference between traces and the relative permittivity of the encapsulant. A model was formed using this and used in PowerSynth to determine the appropriate trace-gap for the given encapsulant and potential difference between traces. Table I shows the trace-gap for various voltages determined by this model for an encapsulating material with a relative permittivity of 2.83 and a dielectric strength of 20 kV/mm (representative of a commonly used gel encapsulant such as Dow Corning's 3-6635 dielectric gel). These trace gaps are reflected in the layouts for the solution set shown in Fig. 8 where the reliability constraints override the default design rules mentioned in the previous section, yielding larger footprint layouts but that satisfy high-voltage spacing requirements.

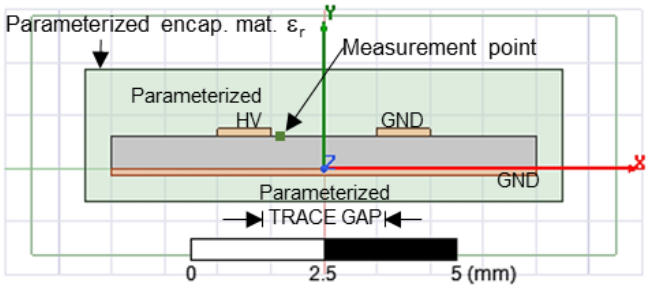


Fig. 7. 2D trace gap model.

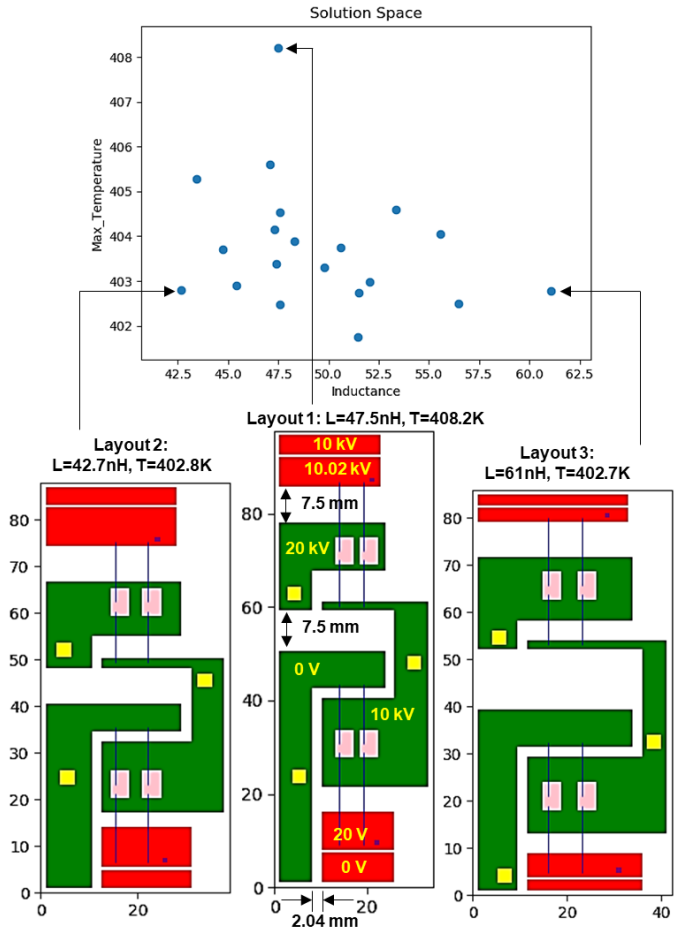


Fig. 8. Electro-thermal trade-off solution set with voltage reliability constraints.

Table I. Minimum spacing for potential difference

Voltage difference (V)	Minimum spacing (mm)
<= 20	0.5
~10,000	2.04
~20,000	7.5

Increased gap between traces due to higher potential difference moves traces farther apart, making the path between the leads longer, resulting in greater loop-inductance and resistance. The overall layout footprint increases, increasing the capacitance between the top and bottom layers. Trace gap impact on temperature depends on the thermal coupling between devices on two separate traces.

PowerSynth also incorporates design rules that help prevent current crowding. Current crowding can lead to electromigration, creating short circuits and hotspots. A minimum trace width is established to help prevent this. The increased width of a trace reduces the overall resistance of the trace. Same is the case with inductance. Temperature is also reduced with increased trace width as the total area over which heat dissipates increases. The effect of design rule factors on the electro-thermal tradeoff is summarized in Table II.

Table II: Effect of various parameters on co-design

	R, L, Footprint	T
Trace gap	▲	▼
Voltage	▲	▼
Encapsulant permittivity	▼	▲
Isolation thickness	▼	▲
Dielectric strength of the encapsulant	▼	▲

Sharp trace corners in a layout are known sites for PD and mechanical delamination. One straightforward way to mitigate these is by filleting the sharp corners. This reduces the E-field at the triple point by more than half. Fig. 8a shows a 3D model of two simple traces with sharp corners and 10kV potential difference between them across a gap of 2.04mm (according to voltage constraints). For the example shown, when the corners of both traces were filleted 1 mm (Fig. 8b), the E-field near the triple point reduced by 65%. This means the trace gap could be reduced to 0.75mm (Fig. 8c) before the E-field would reach the value it had for the sharp cornered case. Thus, filleting can save space and make the module safer for high voltage operations. This would also reduce parasitic inductance and resistance and the likelihood of trace delamination. PowerSynth can produce filleted and non-filleted layouts. An example is shown in Fig. 10.

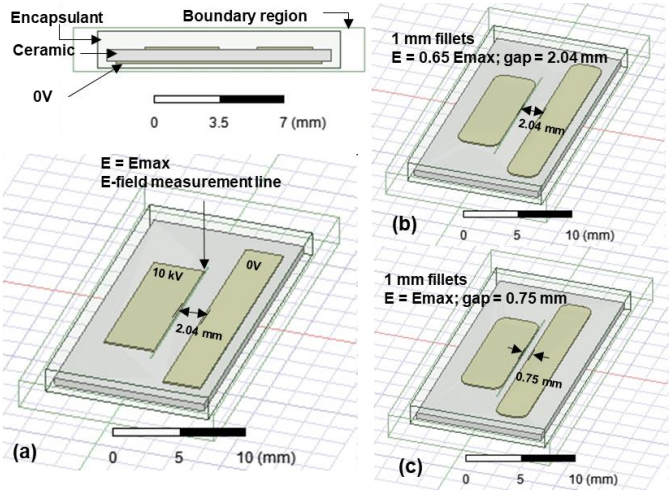


Fig. 9. Effect of filleting on E-field and trace gap.

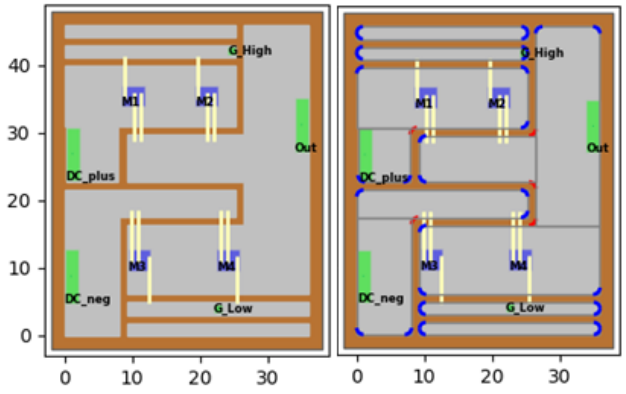


Fig. 10. Half bridge layout generated by PowerSynth without fillets (left) and with fillets (right).

III. Case Study

To demonstrate the capabilities of both tools when coupled with the API, this section contains an example of power module layout design optimization performed using PowerSynth and ParaPower. The example design is a half-bridge power module with two devices per switching position as shown in Fig. 11. The footprint of the module varies between 30 x 40 mm and 152 x 62 mm during optimization. This allows for footprint sizes incorporating the smallest possible layout—when considering the MDK and design constraints—as well as several other sizes commonly found in commercial power modules. Performance metrics chosen include the loop inductance, thermal resistance, and maximum stress. For the loop inductance calculation, the power loop is defined as being from the DC+ to DC- terminals of the power module as shown in Fig. 11. Module thermal resistance is measured from junction to case with the backside of the power module kept at a constant of 25 °C with 10 W of power dissipation per die., Maximum thermal stress results are decoupled from the thermal resistance calculation and run as a separate analysis with no power dissipation in the devices and a temperature differential between the processing temperature of the solder (230°C) and a user specified minimum environment temperature (-40°C) to represent the greatest thermal excursion from the processing temperature. In total, 650 layouts were evaluated in approximately 60 minutes using this API. The solution space is shown as three graphs in Fig. 12 where

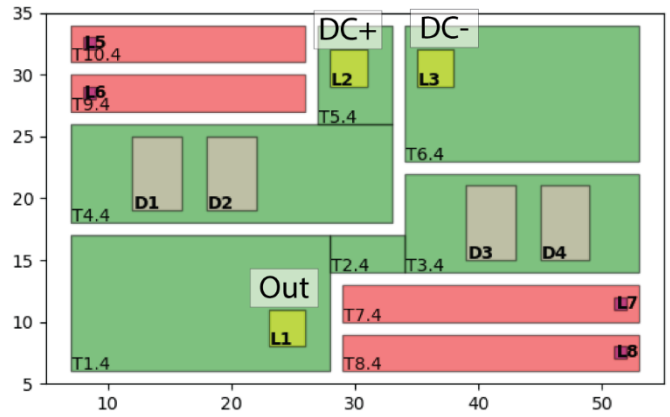


Fig. 11. Initial layout for the case study showing trace, device, and lead locations.

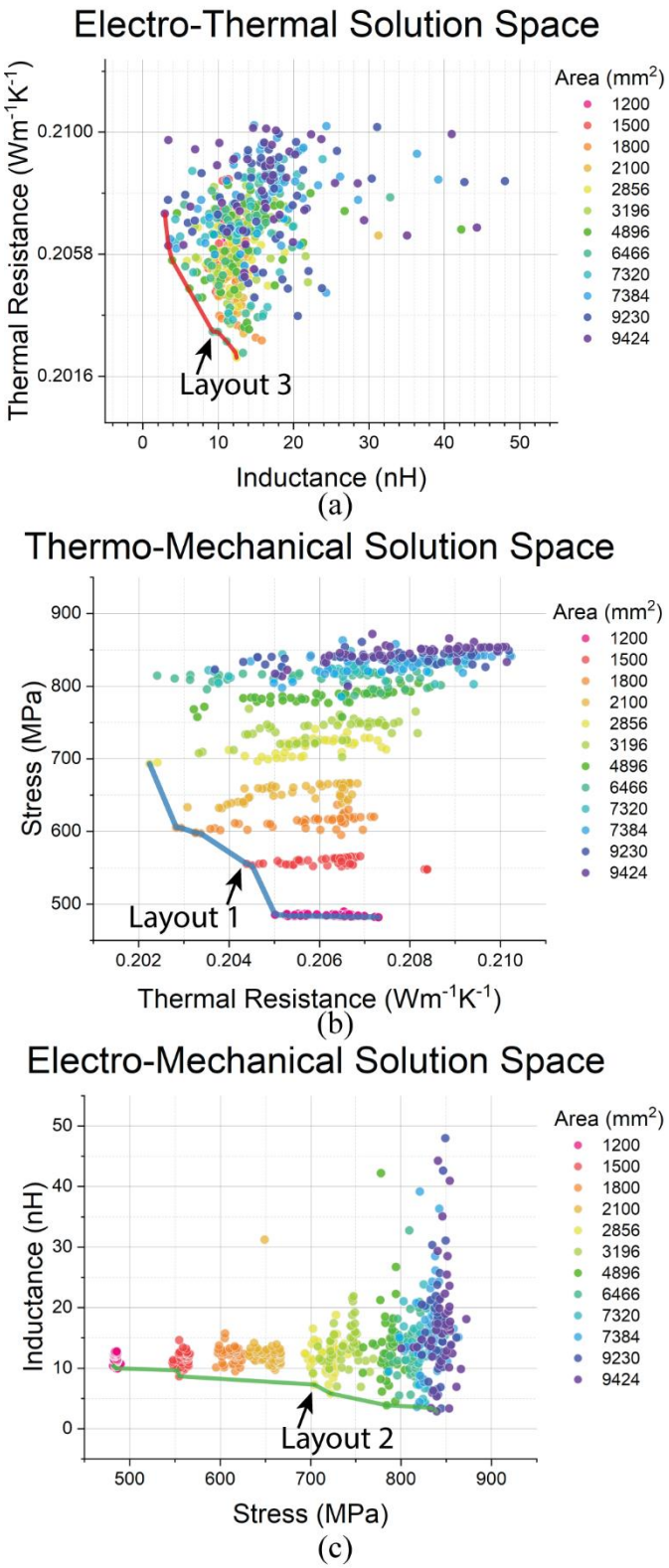


Fig. 12. Solution space consisting of 650 candidates generated from the layout in Fig. 11. Tradeoffs in performance metrics for the (a) electro-thermal, (b) thermo-mechanical, and (c) electro-mechanical solution spaces are shown. Non-dominated solutions lie along the pareto frontiers in each solution space and are denoted by a solid line. Labeled solutions are shown in Fig. 13.

performance metrics are shown as pair-wise tradeoffs whereas the 3 selected layouts from along the Pareto frontier are illustrated in Fig. 13. Final values for these performance metrics are shown in Table III. Of note is that, while Layout 1 has a much smaller footprint and lower stress values when compared with Layout 3, their inductances are very similar due to their similar loop areas however Layout 3 has a slightly reduced thermal resistance at the expense of higher stress. Layout 2 represents a compromise with lower inductance and higher thermal resistance than the other two and with stress values in between.

Table III: Layout Performance Metrics

	Dimensions (mm)	Inductance (nH)	R_{TH} ($Wm^{-1}K^{-1}$)	Stress (MPa)
Layout 1	50x30	9.93	0.204	556
Layout 2	84x34	7.23	0.206	704
Layout 3	106x61	9.26	0.203	816

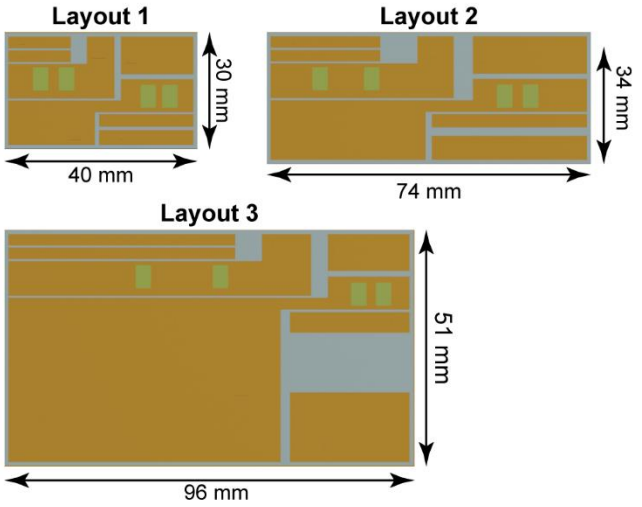


Fig. 13. Final layout solutions shown to relative scale.

IV. Conclusion and Future Work

The push toward design automation and co-design of power electronics modules continues to gain momentum as more tools are introduced and collaborations formed among research groups. PowerSynth and ParaPower are two such EDA tools that are shown here to benefit greatly from integration with each other. The layout generation capabilities of PowerSynth ensure not only manufacturable solutions but also allow for modification of design rules based on operating voltage and material properties. Finally, by developing an API for these two tools, their respective electrical, thermal, and mechanical models can be used together as performance metrics in a multi-objective layout-optimization routine. Moving forward, continued development will increase the reliability of generated layouts, and the fidelity of existing models while introducing new ones—allowing the power module designer more opportunities to rapidly explore their chosen design space.

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References

[1] J. Rabkowski, D. Peftitsis and H.-P. Nee, "Silicon carbide power transistors: A new era in power electronics is initiated," *IEEE Industrial Electronics Magazine*, vol. 6, pp. 17-26, 6 2012.

[2] U. Drofenik, D. Cottet, A. Muesing and J. W. Kolar, "Design Tools for Power Electronics : Trends and Innovations," *Ingénieurs de l'automobile*, vol. 791, pp. 55-62, 2007.

[3] B. Du, J. L. Hudgins, E. Santi, A. T. Bryant, P. R. Palmer and H. A. Mantooth, "Transient Electrothermal Simulation of Power Semiconductor Devices," *IEEE Transactions on Power Electronics*, vol. 25, pp. 237-248, 2010.

[4] M. Hammadi, J. Y. Choley, O. Penas, J. Louati, A. Rivière and M. Haddar, "Layout optimization of power modules using a sequentially coupled approach," *International Journal of Simulation Modelling*, vol. 10, pp. 122-132, 2011.

[5] P. Ning, F. F. Wang, K. D. T. Ngo and S. Member, "Automatic Layout Design for Power Module," *IEEE Transactions on Power Electronics*, vol. 28, pp. 481-487, 2013.

[6] B. Ji, X. Song, E. Sciberras, W. Cao, Y. Hu and V. Pickert, "Multiobjective design optimization of IGBT power modules considering power cycling and thermal cycling," *IEEE Transactions on Power Electronics*, vol. 30, pp. 2493-2504, 2015.

[7] T. M. Evans, Q. Le, S. Mukherjee, I. Al Razi, T. Vrotsos, Y. Peng and H. A. Mantooth, "PowerSynth: A power module layout generation tool," *IEEE Transactions on Power Electronics*, vol. 34, pp. 5063-5078, June 2019. doi: 10.1109/TPEL.2018.2870346 .

[8] Imam Al Razi, Quang Le, H. Alan Mantooth, and Yarui Peng, "Hierarchical Layout Synthesis and Design Automation for 2.5D Heterogeneous Multi-Chip Power Modules", in *Proc. IEEE Energy Conversion Congress and Exposition*, pp. 2257-2263, Sep 2019.

[9] US Army Research Laboratory, ARL ParaPower, https://github.com/USArmyResearchLab/ParaPower, 2019.

[10] M. Ghassemi, "PD measurements, failure analysis, and control in high-power IGBT modules," *High Voltage*, vol. 3, pp. 170-178, 2018.

[11] M. Ghassemi, "Electrical Insulation Weaknesses in Wide Bandgap Devices," InTechOpen, Ed., InTechOpen, 2018, pp. 129-149.

[12] S. Mukherjee, T. M. Evans, et al., "Towad Partial Discharge Reduction by Corner Correction in Power Module Layouts." *IEEE 19th Workshop on Control and Modeling for Power Electronics* (COMPEL), pp. 1-8, 2018.

[13] Quang Le, Tristan Evans, Shilpi Mukherjee, Yarui Peng, Tom Vrotsos, and H. Alan Mantooth, "Response Surface Modeling for Parasitic Extraction for Multi-Objective Optimization of Multi-Chip Power Modules (MCPMs)", in *Proc. IEEE Workshop on Wide Bandgap Power Devices and Applications*, pp. 327–334, Oct 2017.

[14] Quang Le, Tristan Evans, Yarui Peng, and H. Alan Mantooth, "PEEC Method and Hierarchical Approach Towards 3D Multichip Power Module (MCPM) Layout Optimization", in *Proc. IEEE International Workshop on Integrated Power Packaging*, pp. 131–136, Apr 2019.

[15] Tristan M. Evans, Quang Le, Balaji Narayanasamy, Yarui Peng, Fang Luo, and H. Alan Mantooth, "Development of EDA Techniques for Power Module EMI Modeling and Layout Optimization," *International Symposium on Microelectronics*: Fall 2019, Vol. 2019, No. 1, pp. 000193-000198. 2019. doi: 10.4071/2380-4505-2019.1.000193

[16] M. Deckard, P. Shamberger, M. Fish, M.Berman, J.Wang, and L. Boteler, "Convergence and Validation in ParaPower: A Design Tool for Phase Change Materials in Electronics Packaging," in *2019 18th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems* (ITherm), pp. 878-885, 2019.

[17] L. Boteler and S. Miner, "Evaluation of Low Order Stress Models for Use in Co-Design Analysis of Electronics Packaging," in *Proc. ASME 2019 International Technical Conference and Exhibition on Packaging and Integration of Electonic and Photonic Microsystems*, 2019