General Equation to Determine Design Rules for Mitigating Partial Discharge and Electrical Breakdown in Power Module Layouts

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***Abstract*—Systematic design rules to prevent partial discharge in power modules have been formulated for the first time and incorporated into PowerSynth, an electronic design automation tool. The tool's existing framework for supporting reliability constraints has been leveraged to incorporate voltage and material specific design rules that are informed by finite element simulations. A new general equation to predict the minimum trace gap for various voltages and encapsulants has been determined from these simulations. The tool can now generate layouts of power modules that can be operated up to 30kV.**

Keywords—Design rule, power module, partial discharge, trace gap, electric field, encapsulant permittivity, simulation, high voltage

I. INTRODUCTION

Partial discharge (PD) is a known problem in power modules that can deteriorate an insulating material. The likelihood of PD is increased with the focusing of electric fields at the triple points (metal-ceramic-encapsulant interfaces at metallization corners). Many studies have been done to understand and address this. Most of the factors affecting PD are related to the geometry [1], [2], and materials [3] in the modules, voltage stress in the system [4], and the environment. While these analyses help in understanding the causes and effects of PD for a specific case, they do not predict or inform general power module design structures. This work addresses practical power module layouts. Design rules are developed for these layouts to operate at high voltages, considering geometry and material aspects. These rules are incorporated into PowerSynth [5], an in-house layout optimization tool, where the existing design rule framework [6] is expanded with data obtained from finite element simulations.

E-field concentration is a precursor to a partial discharge inception, and it is infinitely large at sharp corners such as at a triple point in a simulation model or in a calculation [7]. Bayer's team [8] found a way to account for this singularity using a virtual fillet radius concept. The reduction in E-field with increasing fillet radius was correlated to the reduction in E-field with decreasing mesh density. The virtual radius was found to be about 80% of the grid size. This means a grid of 1mm near the triple point would yield the same E-field as if there was a 0.8mm radius fillet. The E-field magnitude at a sharp corner is not realistic. Filleting the corner, the E-field values converge as mesh density is increased. Bayer's team measured E-field values 50 μm from the triple point as this is where various E-field vs. mesh resolution curves matched. These adjustments guided the 2D simulations for this work.

Other E-field simulations were performed by Abdelmalik, Ghassemi and Tousi, DiMarino, and others. Abdelmalik's work focused on effects of low pressure at high altitudes on PD. He considered trace gaps on printed circuit boards and found E-field concentrating at the triple point [9]. Ghassemi and Tousi also showed E-field concentration at the triple point and considered field dependent conductivity layers to mitigate E-field focusing in high voltage power modules [10]. ANSYS 2D simulations done by Dimarino showed methods to improve PD inception voltage using stacked substrates that reduce the E-field at triple points [11].

While many simulation and experimental efforts have been made in PD mitigation, there are no design rules established for high voltage operation of power modules. For this work, 2D and 3D models are designed and simulated in ANSYS Maxwell for the development of an equation that can be used to determine safe distances for metal traces on a ceramic substrate. And this equation is implemented in PowerSynth for the benefit of ensuring all designs satisfy the high voltage reliability rules based on this work.

II. 2D SIMULATIONS

A. Model Description

A 2D representation of a patterned and encapsulated direct bond copper (DBC) substrate is shown in Figure 1. There are two traces on top and a ground plane at the bottom, with ceramic isolation in between. Trace A, as shown in the figure,

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is the trace on which voltage excitation is parameterized, while the other two traces (B and C) are held at zero volts.

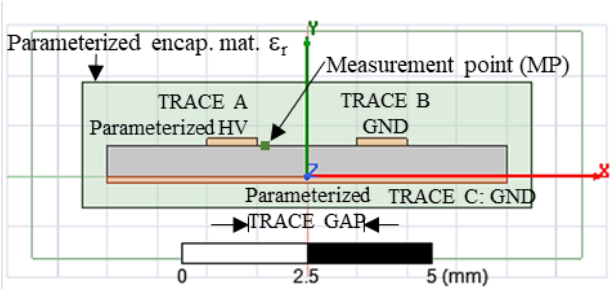

Fig. 1. 2D model of a power module substrate.

Mathematically, E-field is infinitely large at the triple point. So, E-field is measured at a point very close to the triple point (TP), yet a distance from the TP that is relative to the trace-gap. The measurement point (MP) is 5% of the trace-gap away from the triple point. Parametric sweeps on voltage (v), trace gap (x), and encapsulant relative permittivity (ε_r) are applied. Alumina ceramic thickness and permittivity, and copper thickness are kept constant (Table I).

Table I. Sweep Parameters and constants for 2D simulations.

Parameter	Range	Step size
Trace gap (x)	0.5 mm to 5.0 mm	0.5 mm
Voltage (v)	5 kV to 30 kV	5 kV
Encapsulant relative permittivity (ε_r)	1 to 10	1
Ceramic thickness	0.625 mm (25 mil)	
Metal thickness	0.125 mm (5 mil)	
Ceramic ε_r	9	

B. Simulation Results

E-field results for 2D simulations are shown in Figure 2. At 2.5mm trace gap, the capacitive effect between Traces A and C dominates over that between traces A and B. But as the two traces on the top are brought closer together, the E-field is affected by the presence of Trace B (as shown by the bottom figure) where trace gap is 0.5mm. Since traces B and C are at the same potential, it is as though they are electrically connected, though physically separate. So, there is a capacitive effect between traces A and B that should be considered for compact modules operating at high voltages. The field gradients also vary in the two dielectric materials as can be seen in Figure 2. Therefore, dielectric material mismatch should be considered, and this was accounted for in 3D simulations.

The variation of E-field with respect to trace gap followed an inverse power relationship as shown in Figure 3 for the corner cases, and Equation 1 where E is the E-field at the measurement point, x is the trace- gap, v is the voltage on Trace A with respect to Traces B and C, ε_r is the relative permittivity of the encapsulant material, the coefficient f and the exponent g are separate functions of v and ε_r , and are determined from Tables II and III. The practical dielectric strength value along with the relative permittivity of the encapsulant and the practical voltage overshoot value can be used to determine the appropriate coefficient and exponent, and thus back-calculate the minimum trace-gap needed.

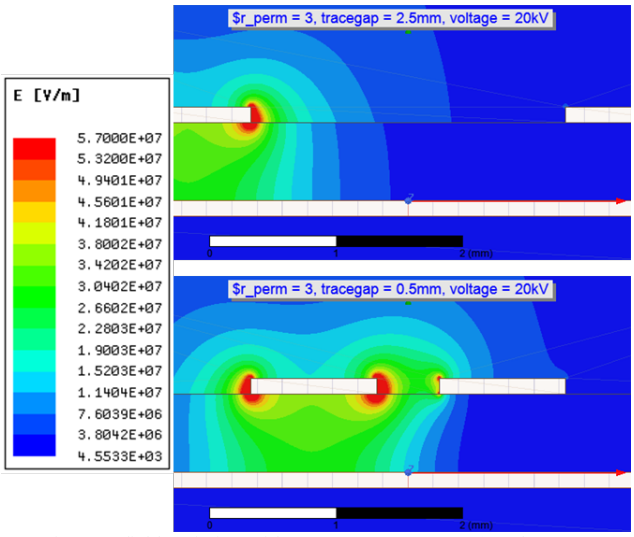

Fig. 2. E-field variation with trace-gap (2.5mm (top) and 0.5mm (bottom)).

$$E = f(v, \varepsilon_r) * x^{-g(v, \varepsilon_r)} \quad (1)$$

Table II. f (v, ε_r): Effect of voltage (v) and relative permittivity (ε_r) on the coefficient in Eq 1, f, expressed in 10^7 V/m.

ε_r	5 kV	10 kV	15 kV	20 kV	25 kV	30 kV
1	1.48	2.96	4.43	5.91	7.75	8.87
2	1.48	3.02	4.27	5.75	7.60	9.11
3	1.41	2.94	4.23	5.61	7.51	9.11
4	1.38	2.77	4.15	5.74	7.17	8.30
5	1.62	2.90	4.24	5.48	7.22	8.64
6	1.39	2.78	4.07	5.51	6.88	8.18
7	1.35	2.69	4.03	5.38	6.80	8.20
8	1.35	2.72	4.05	5.41	6.80	8.11
9	1.33	2.67	4.00	5.35	6.66	8.01
10	1.32	2.64	3.96	5.29	6.61	7.92

Table III. Effect of v and ε_r on the exponent, g, of the power curves.

ε_r	5 kV	10 kV	15 kV	20 kV	25 kV	30 kV
1	0.63	0.63	0.63	0.63	0.66	0.63
2	0.56	0.55	0.51	0.55	0.53	0.53
3	0.57	0.54	0.49	0.51	0.57	0.53
4	0.56	0.56	0.51	0.60	0.56	0.51
5	0.53	0.61	0.56	0.54	0.56	0.55
6	0.54	0.53	0.54	0.55	0.53	0.56
7	0.52	0.53	0.53	0.53	0.54	0.54
8	0.54	0.54	0.54	0.55	0.56	0.56
9	0.55	0.55	0.55	0.55	0.55	0.54
10	0.55	0.55	0.55	0.55	0.55	0.55

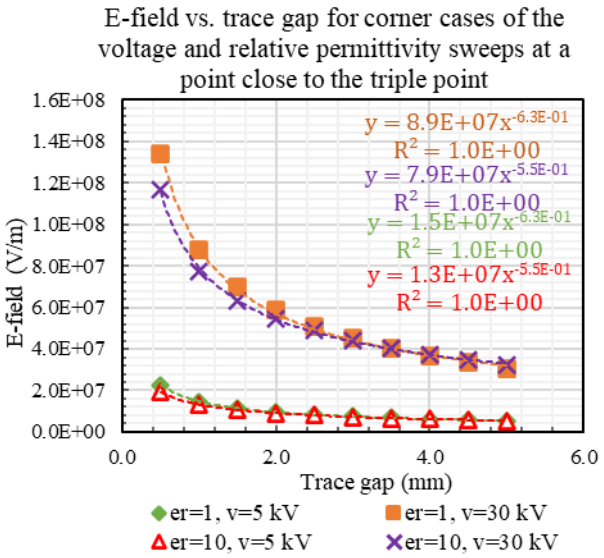

Fig. 3. E-field vs. trace gap for corner cases.

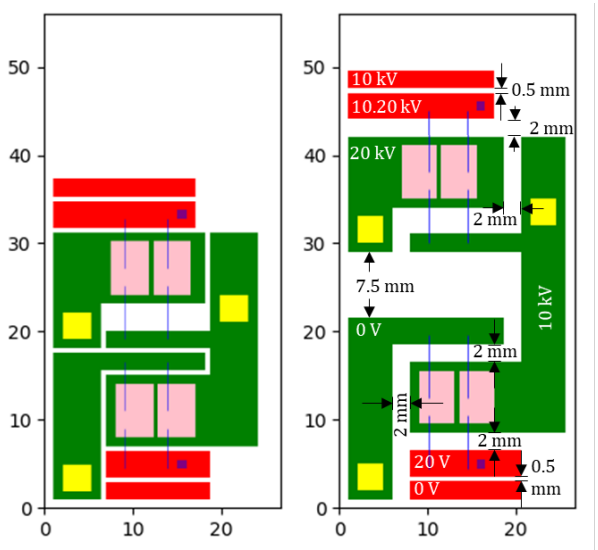

Fig. 4. Layout without reliability constraints (left) and with reliability constraints (right).

C. *Implementation in PowerSynth*

PowerSynth, an electronic design automation tool, was created to help power module designers rapidly assess and optimize layouts for electro-thermal performance. As layouts are automatically modified by the software, they must adhere to certain design rules that dictate trace spacings, component spacings, trace widths, etc. The default design rules are based on process parameters. For example, the minimum trace gap is set to 0.5 mm, which is the minimum feature size that can be achieved with wet etching of a direct bond copper substrate. But the default design rules do not account for increased spacings needed when operating at higher voltage levels. Equation 1 is used to find minimum trace gaps for layouts given the potential difference between traces, the dielectric strength, and the dielectric constant of the encapsulant. The E-field in Equation 1 is the dielectric strength of the encapsulant. This is stored in PowerSynth in a material property library which also includes the relative permittivity of materials. The dielectric strength provided in PowerSynth is the datasheet value, which is typically measured under ideal conditions. For practical purposes, two-third of that value can be assumed as more realistic. Materials used in the layer stack up of the power module are provided by the user. The user can also add novel materials to the library. Tables II and III are exported to PowerSynth and used as look up tables for the coefficient and exponent of Equation 1. The trace-gap is then calculated, and it replaces the default trace gap in the design rule kit.

Figure 4 shows two layouts generated by PowerSynth, one with the trace-gap constraints applied, and the other without. In this example, 20 kV/mm is assumed as the dielectric strength of the encapsulant and the relative permittivity of that encapsulant is 3. For a 10 kV potential difference between two traces, the trace-gap is approximately 2 mm according to this equation. With a potential difference of 20 kV, the minimum spacing is 7.5 mm. The tradeoff is that the overall footprint of the layout increases, and this also results in an increase in the parasitic inductance and resistance.

III. 3D Simulations

A. *Model Description*

A 2D model can sometimes be too simplistic. The investigation of E-fields at and near the triple point is tridimensional in nature and should be assessed as such. Therefore, to obtain a more realistic picture, a 3D model is created. While the trend of E-field with respect to trace gap in a 3D model continues to follow an inverse power relationship, the magnitude of the E-fields is very different and difficult to compare to physical systems. 3D simulations yield four times higher E-field compared to 2D simulations. This could be attributed to the increased capacitive effect between Traces A and B due to the area introduced and charge distribution at the four corners and edges. Also, the analysis is computationally expensive as millions of volume elements in the insulation material are meshed for each design variation. Even with higher density mesh applied to a small volume region near the triple point and coarser mesh in the remaining volume, it is computationally very expensive to run multiple design variations on a volumetric mesh.

More informative and less computationally expensive is the analysis of surface charge density. It is faster to work with surface charge density since it is measured on a conductor surface and the conductor surfaces are much smaller to mesh than insulator surfaces (where E-fields are measured). Figure 5 depicts the 3D model. Surface charge density was measured on the face of Trace A that is facing Trace B. Charges accumulated at the corners as expected. However, to avoid mesh related charge magnitude dependencies at the corners, the measurement point is chosen to be at a place where the average charge density could be captured.

As seen in Figure 2, E-field dominates in the space between the top trace (A) and bottom trace (C). This is due to the smaller gap between traces A and C compared to the gap between traces A and B. But as the top two traces (A and B)

are brought closer together, at a certain point, there is an effect between Traces A and B due to their potential difference and reduced spacing. This happens when the trace gap is comparable to the thickness of the ceramic isolation layer. In this case, it happens when the trace-gap is 0.33 mm, when the ceramic thickness is 1.0 mm. The ratio of the trace-gap to the ceramic thickness is, therefore, important. Instead of using an absolute trace-gap (between traces A and B) in the empirical equation, a ratio of distances is used; the ratio of the absolute trace-gap between traces A and B, and the distance between traces A and C. For convenience, 1 mm is chosen as the ceramic thickness. This is also the largest thickness for a ceramic in a manufactured DBC. The metallization thickness was also maximized to 0.3 mm.

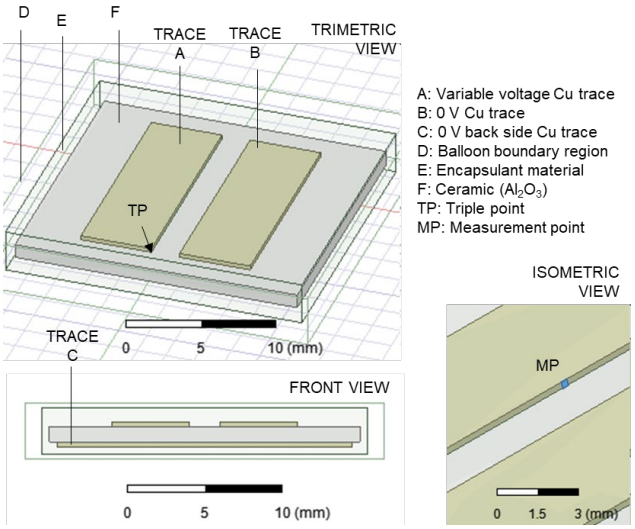

Fig. 5. 3D model of a power module DBC substrate.

Figure 2 also shows how E-field distributes differently in the ceramic and in the gel encapsulant. This is attributed to the difference in the relative permittivity of the two materials. Since there are two insulating materials to be considered, the permittivity in the empirical equation is also a ratio: a ratio of the permittivity of the encapsulant material and the permittivity of the ceramic. Constants and parameters for the 3D simulations are shown in Table IV.

B. Simulation Results

The 3D simulation results for surface charge density followed the same trend as that of the 2D simulations for E-field. The inverse power relationship between the surface charge density and the normalized trace gap is shown in Figure 6 and by Equation 2.

$$Qsurf = f(v, \varepsilon_r') * x^{-g(v, \varepsilon_r')} \quad (2)$$

where Qsurf is the surface charge density between the two traces on the top side in mC/m^2, x is the ratio of the trace-gap on the top to the ceramic isolation thickness between the top metallization and the bottom, v is the voltage applied to Trace A (in kV) with respect to the bottom trace and Trace B, ε_r' is the ratio of the relative permittivity of the encapsulant and the ceramic, f and g are separate functions of v and ε_r'.

Table IV. Sweep Parameters and constants for 3D simulations.

Parameter	Values or Range
Trace gap (x), mm	0.2, 0.4, 0.6, 0.8, 1.0, 1.5, 2.0
Voltage (v), kV	2.5, 5.0, 7.5, 10.0, 15.0, 20.0
Encapsulant relative permittivity (ε_r)	1-4, 7, 10
Ceramic thickness	1 mm (40 mil)
Metal thickness	0.3 mm (12 mil)
Ceramic ε_r	9.8

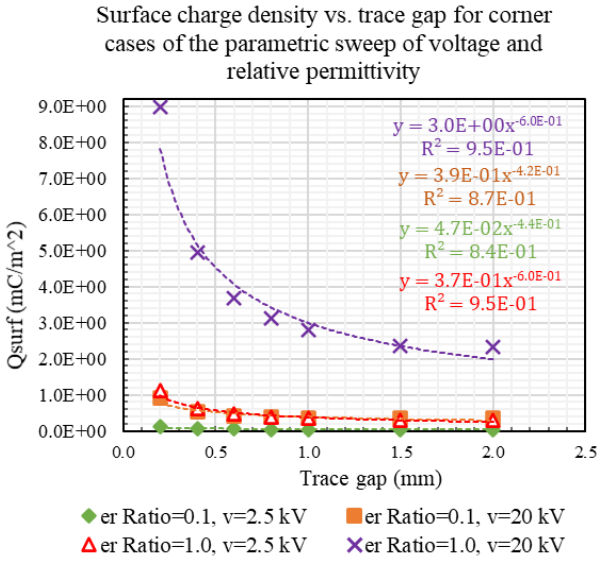

Fig. 6. E-field vs. trace gap for corner cases.

Table V. Effect of v and ε_r' on the coefficient, f, of the surface charge density power curves, in mC/m^2.

ε_r	ε_r'	2.5 kV	5 kV	7.5 kV	10 kV	15 kV	20 kV
1	0.10204	0.047	0.097	0.150	0.190	0.290	0.390
2	0.20408	0.093	0.190	0.280	0.370	0.560	0.740
3	0.30612	0.130	0.270	0.400	0.530	0.800	1.100
4	0.40816	0.170	0.340	0.520	0.690	1.000	1.400
7	0.71429	0.280	0.550	0.830	1.100	1.700	2.200
10	1.02041	0.370	0.750	1.100	1.500	2.200	3.000

Table VI. Effect of v and ε_r' on the exponent, g, of the surface charge density power curves.

ε_r	ε_r'	2.5 kV	5 kV	7.5 kV	10 kV	15 kV	20 kV
1	0.10204	0.44	0.42	0.42	0.42	0.42	0.42
2	0.20408	0.45	0.45	0.45	0.45	0.45	0.45
3	0.30612	0.48	0.48	0.48	0.48	0.48	0.48
4	0.40816	0.50	0.50	0.50	0.50	0.50	0.50
7	0.71429	0.56	0.56	0.56	0.56	0.56	0.56
10	1.02041	0.60	0.60	0.60	0.60	0.60	0.60

Since E-field (E) and charge density (Qsurf) are related by the permittivity as shown in Equation 3, this relationship can be used to find E-field and then implement the same way in PowerSynth as is done for the 2D case. Here $\varepsilon = \varepsilon_0 * \varepsilon_r$ where

ε_r is the relative permittivity of the encapsulant since E-field is higher in the encapsulant than in the ceramic.

$$Qsurf = \varepsilon * E \quad (3)$$

C. *Effect of Filleting*

Filleting is a standard approach in the industry for mitigating partial discharge due to E-field concentration at sharp corners and delamination of traces due to thermo-mechanical stresses at sharp corners. The effect of filleting on surface charge density is shown in Figure 7. Charge density is reduced to about 54% its original value with a 0.5 mm fillet and is further reduced when the fillet radius is 1.0 mm. The reduction of surface charge density due to filleting allows the trace-gap to be smaller. This is also shown to be true with E-field simulations where the field is reduced to about 65% its original value when a 1.0 mm fillet is used. With the filleted design, the trace-gap can be reduced to about 40% its original value (Figure 8). Fillets also have a mechanical advantage (Figure 9). Stress simulations confirmed that stress is concentrated at sharp corners and filleting those corners reduces stress at those corners by 18%.

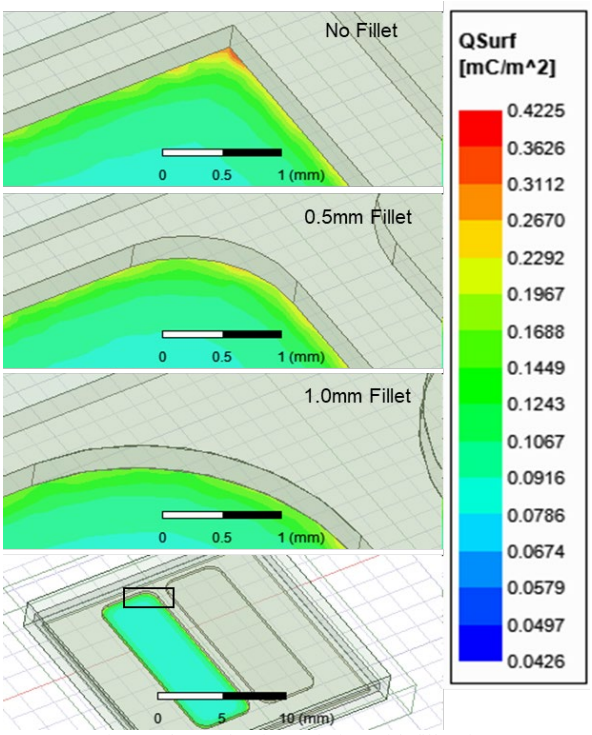

Fig. 7. Charge density variation with fillet size.

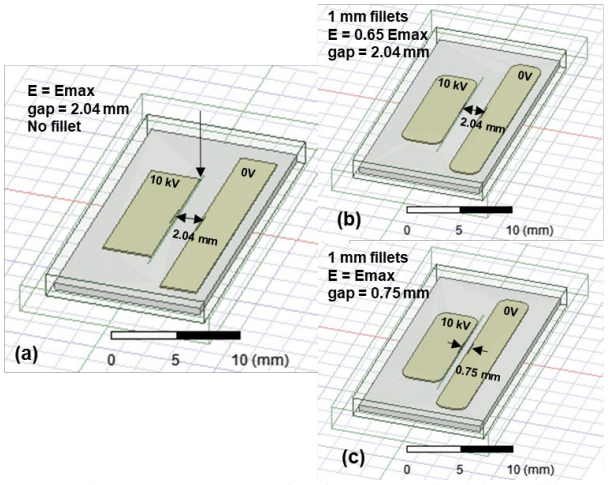

Fig. 8. Reduction in trace gap with reduction in E-field due to filleting.

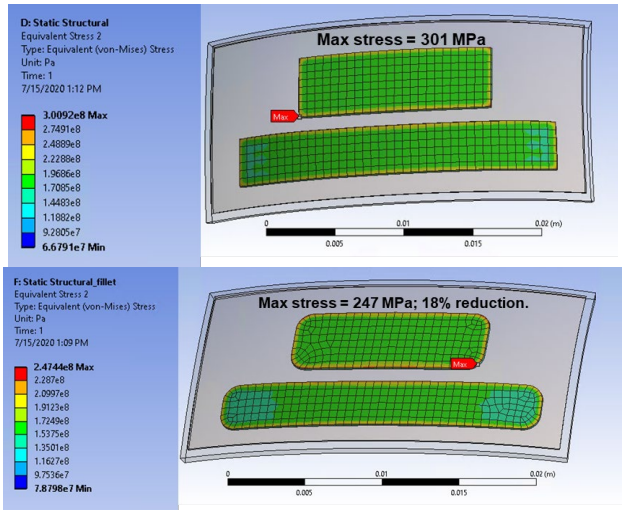

Fig. 9. Stress comparison with (bottom) and without (top) fillets.

IV. Conclusion

While partial discharge is a complex problem and requires detailed analysis of the physical phenomena occurring at the PD inception point, an estimate can be attained using E-field and surface charge density simulations. Empirical equations can be derived and used to inform design rules for power modules. Such equations were derived in this work using ANSYS Maxwell simulations. The general equations incorporate material properties, voltage level, and inform the designer of the appropriate trace-gap that could be used. While this work is based on estimates from simulations, future work will include test structures fabricated and tested for partial discharge. The equations will be further enhanced by being calibrated to experimental values, and then analyzed statistically to incorporate the random processes involved in the occurrence of a partial discharge. In the meantime, PowerSynth will continue to inform users of updated layout structures based on these constraints. This is the first time a design rule based on voltage and material aspects has been determined for power modules and incorporated in a power module design automation tool.

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