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The Increasing Role of Design Automation in Power Electronics

Gathering what is needed

The second Design Automation for Power Electronics (DAPE) workshop was held in the beautiful historical city of Genova, Italy, on 6 September 2019. This was one day after the successful European Conference on Power Electronics and Applications (EPE ECCE). With approximately 40 participants and a nice mix of industry and academic affiliations, the workshop provided outstanding presentations covering the wide field of design automation for power electronics. A very novel exchange of views was performed by breakout sessions, and the use of online voting technology to rapidly poll the attendees on

prepared questions of interest in DA provided valuable information (Figure 1).

The breakout sessions were focused on group discussions about the fundamental questions in the domain of design automation, such as:

- 1) For DA, which aspects need research, and in which cases is it good enough?
- 2) What are the major bottlenecks in data quality and accessibility? How could standardization help?
- 3) What are the desired features for power electronics design engineers?
- 4) How do you verify the results of DA algorithms?
- 5) How do you see the role of artificial intelligence (AI) in DA?

The breakout sessions tackled these questions with the final session devoted to reporting the results. A postmeeting notes

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compilation was provided to all attendees along with the presentations, which are available in the IEEE Power Electronics Society (PELS) Resource Center [2]. More information about the workshop can be found on the DAPE website [3].

Promoting DA in the field of power electronics is the goal of the DAPE initiative within the IEEE PELs. Starting with workshops to highlight the importance of DA, the DAPE initiative is already working on further activities to become the collaborative platform for exchanging ideas about DA for power electronics. Facilitating DA is of utmost importance to make technological advances and keep up with the demands of modern societies on electric power supply. The shortening of product development cycles and increasing use of power electronics with the demand for more tailored solutions lead to a higher complexity with which power electronics designers have to cope. The only way to address the resulting challenges is through DA.

State-of-the-Art Solutions

The first part of the DAPE workshop consisted of several presentations from a wide range of academia, computer-aided design (CAD) vendors, design houses, and testing equipment providers. It was divided into two sessions with a break in between for follow-up discussions. Several interesting topics captured most of the attention, including fast-yet-accurate models and circuit simulators, system-level optimization algorithms, layout-driven component optimization methods, model-based design space exploration, and automated design synthesis workflows.

With the exponential growth of computing power, the question of how to effectively utilize these ever-increasing hardware resources to construct an efficient workflow becomes a challenging but rewarding problem to solve. One of the most generic solutions is to start with efficient models and algorithms. Unlike generic circuit simulators, such as the Simulation Program With Integrated Circuit Emphasis (SPICE), the Latency Insertion Method (LIM), developed by Prof. Jose Schutt-Aine's group from the University of Illinois, is highly customized for simulations on RLC mesh networks, which are widely used to analyze power distribution networks or thermal effects. By dividing the network into RL branches and GC nodes and then separately updating branch currents and node voltages, the general nodal analysis can be accelerated, resulting in linear-scaling time complexity and predictable stability. This approach can be applied on standard netlists and provides a computational speed up by several magnitudes compared with SPICE. Other extensions, including device simulation and stochastic analysis, have the potential to replace commercial general-purpose simulators for power analysis.

Dr. Thomas Guillod and Prof. Johann Kolar from ETH Zurich further evaluated and compared different optimization algorithms, including brute-force search, analytical model, genetic algorithm, gradient method, and neural network, in terms of computability, efficiency, and applicability for PE applications. Through automation, the design space can be quickly explored within sufficient accuracy for a converter design case study. A standard interface to allow smart switching between algorithms may further enhance design diversity and flexibility.

Besides stand-alone algorithms, other speakers focused on integrating various DA tools into repeatable design flows to replace the best practices in PE engineering. Prof. Yaru Peng from the University of Arkansas (UA) presented a multiobjective layout synthesis tool called *PowerSynth* (Figure 2). Inspired by the physical design tools used in integrated-circuit designs, *PowerSynth* was developed collaboratively within the UA Power Group led by Prof. Alan Mantooth. It generates a Pareto front of manufacturable and optimized module layouts with predictable electro-thermal metrics. Resembling the semiconductor foundry

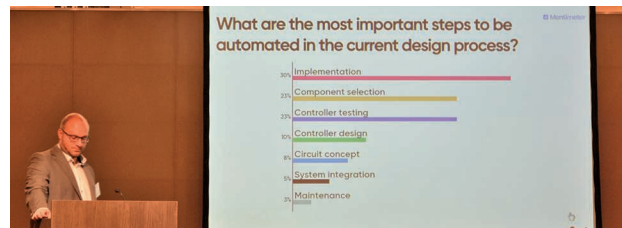


FIG 1 Kevin Hermanns presenting an online voting question at the second DAPE workshop: What are the most important steps to be automated in the current design process?

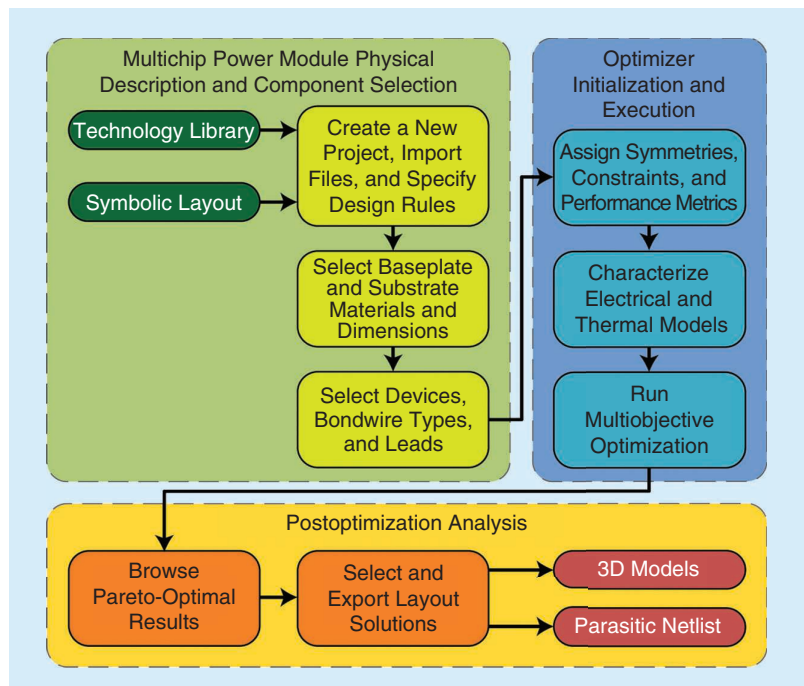


FIG 2 The *PowerSynth* layout synthesis and optimization workflow.

business model, it can further enable customized power package prototyping through a fabrication plant with quick turnaround time. Riccardo Giacometti from Keysight Technologies also shared its electromagnetic (EM) cosimulation solutions for power electronics designers (PEDs). Unlike the time-consuming trial-and-error approach, the PathWave Design Suite provides an interactive schematic and layout design environment with parasitic-annotated netlists for accurate EM simulations and an integrated thermal analysis engine for risk-proof agile development.

Targeting various applications, customized tools are needed to drive further innovations forward. Dr. Andreas Rosskopf from the Fraunhofer Institute for Integrated Systems and Device Technology reviewed several candidate problems as the potential killer applications for automated workflows, i.e., component placement problems, multiple-objective optimizations, and complex designs involving multiple CAD tools. In addition, Dr. Ki-Bum Park of ABB Zürich looked at several common optimization approaches that can be automated to reduce repetitive work for grid applications. The impacts of modulation, passive-component, circuit-topology, device, and cooling solutions are all well known to society but yet remain to be automated in design practices to avoid common mistakes and repetitive work. To address the challenges for space applications, Vladimir Svikovic from Thales Alenia Space presented an automated design flow (Figure 3) combined with a rigid review process to meet thermal and performance targets, while ensuring reliability and standard compliance at the same time. Although many highly customized tools and scripts are used, this process combines computer assistance with designer guidance interchangeably and can also be standardized and applied to other areas. For testing and verification, Dr. Jost Allmeling

from Plexim also demonstrated its hardware-in-the-loop simulation platform integrating hardware-accelerated testing with model-based analysis to enhance productivity and reduce costs.

During the follow-up discussion, many agreed that power electronic design automation (PEDA) tools are currently most useful for simulation, verification, and evolutionary optimizations rather than finding revolutionary alternatives. However, new automation algorithms, i.e., machine learning and neural networks, may redirect some decision-making processes from rule-based search to data-driven approaches. Other attendees also shared their experiences about the bottlenecks and existing limitations of PEDA tools, such as difficulties of combining system-level with component-level designs, absence of industry interchangeable models and software standards, and the lack of portable algorithms and open-source libraries. Uncertainty in accuracy and applicability further hindered the adoption of academic models into commercial solutions. Some potential solutions were discussed during the afternoon sessions as an initiative for pathfinding.

Needs and Challenges

The second part of the DAPE workshop used a structured conversational process for knowledge sharing, based on the “world café” format. In two consecutive sessions, the participants discussed, in groups, 12 preformulated questions on PEDA. The results of the discussions were captured by moderators and are outlined in this section.

If the state-of-the-art solutions can be summarized as the islanded utilization of different design tools and methods (simulators, synthesis tools, test and measurement), DA makes itself conspicuous by coaction of all these tools and the consistent use of generated data throughout the design process. Thus,

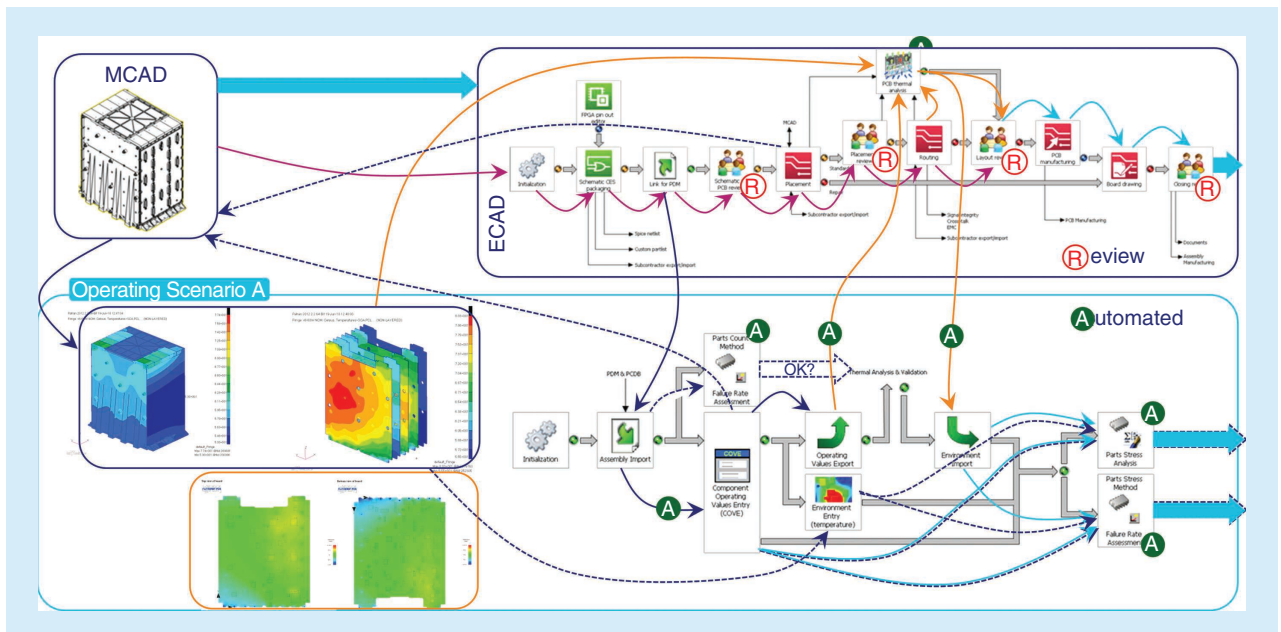


FIG 3 The guided DA flow for space applications showing the interaction of mechanical CAD (MCAD) and electronic CAD (ECAD). (Image courtesy of Vladimir Svikovic of Thales Alenia Space.)

one of the major needs required to conduct DA was identified in the consistent processing of data, starting from the components through to the design of the entire system and later during the full lifecycle of a PE system. To make use of the benefits, standardization of interfaces and data generation is required.

There are already standards in place, but these often do not lead to a compatible solution usable in an application. Furthermore, data required for systems design are in many cases not available in a machine-readable format, and the data sets are not sufficient for a more sophisticated system design, such as field- and temperature-dependent power losses in ferrites. Today, design engineers have to re-extract data from datasheets that were already available in machine-readable formats during the characterization process. This makes data availability one of the major challenges in DA. As a prominent example, the switching losses of semiconductors can be named.

Subsequent to the availability and machine-readability of data throughout the design process, more issues arose, such as the liability of data and data processing. Additionally, with the nondisclosure of sensitive process data—which might be read out from a larger set of data—the answer could not be derived on this question. This makes it a classic chicken–egg problem. While the data availability and quality are poor, DA could not generate benefits necessary to invest in better and more data. Therefore, the added value of PEDAs needs to be named and further qualified in advance. This is a typical task for academia.

Another challenge worked out by the participants of the workshop is seen in a necessary paradigmatic change on how systems design is conducted. To reduce the complexity of the design process, designers have to convert requirements from the design space into a mathematical problem or formulate it so that a solution from DA tools can be worked out independently. This significantly shortens today's lengthy manual, iterative design process (Figure 4) and also requires a change in education of design engineers. Model fidelity, deep knowledge about optimization problems, design of suitable boundary conditions and fitness functions for optimization algorithms, and interpretation of simulation results, together with data processing and handling, will play a crucial role.

While education and access to data in the required quantity and quality are more of a general nature, during the DAPE workshop even more specific needs were worked out by the participants. In almost all fields of tooling, improvements are desired. Starting from faster and more accurate simulators, design synthesis and optimization methods have to be enhanced over model generation.

Taking simulators as an example, new methods like the presented LIM algorithm are promising to lower the computational effort on the solution of network problems. To make these methods attractive, the parametrization of models has to be carried out on available data sets within the same time frame. Otherwise the added value stays limited.

When it comes to DA, another very important task is verification. The design process is increasingly dependent on

models. Determination of model errors rather than occasional plausibility checks is of importance to ensure the achievement of design goals. As a result, it becomes necessary to have more verification loops on minimum viable units. By this the deeper integration of test and measurement equipment into the design process is of greater importance than for a semiautomatic or manual approach. So far, the interaction between simulation tools and test and measurement uses proprietary formats mostly based on comma-separated values files that have to be adapted for each tool or from each source in a different manner. A first solution was presented at the DAPE workshop on how tooling and measurement equipment can be further integrated. The solution was still vendor-specific. The big challenge in DA will be to create a common ground on which all tools and equipment can work. The barriers are wasted time and money, which are limiting further innovations. Codesign processes between different tooling and equipment—in some cases between different companies—will become a key role for DA. This includes a trade-off between fast models with limited functionality and holistic implementations with large computational effort.

So far the discussed needs are just based on the design of power converters to fulfill their dominant task of processing electrical energy in a certain manner, but DA has to do more. The compliance with EM-compatibility standards and the consideration of manufacturing restrictions increase the complexity of problem formulation. DA addresses these challenges as well.

Outlook for DAPE Initiative

DAPE will now begin to transition into more dedicated activities within PELS. Working with PELS leadership, the DA initiative will become part of the technical committee structure, have tracks at conferences where appropriate, and perhaps a dedicated workshop will continue. This two-year exploratory effort led to the identification of the following needs/gaps in DA for PE:

- widely accepted design flow
- parasitic extraction and back annotation onto schematics
- signal integrity and EM interference analysis for PE
- simultaneous electrothermal–mechanical codesign
- circuit synthesis and layout optimization
- module and cabinet design optimization
- uncertainty quantification
- design for reliability and manufacturability
- data standardization
- education on design tradeoffs
- AI/machine-learning methods.

While not necessarily an exhaustive list, it clearly indicates that the field of PE has room for growth in the automation space. PELS will do what it can to facilitate the dissemination of advances in these areas in conferences and publications, while also organizing symposia for industry and academia to discuss solutions for the entire field.

Two efforts are already underway to assist with this. The first is that the 2020 ECCE organizers have agreed to add DA and AI to the big data and machine-learning topic to add more

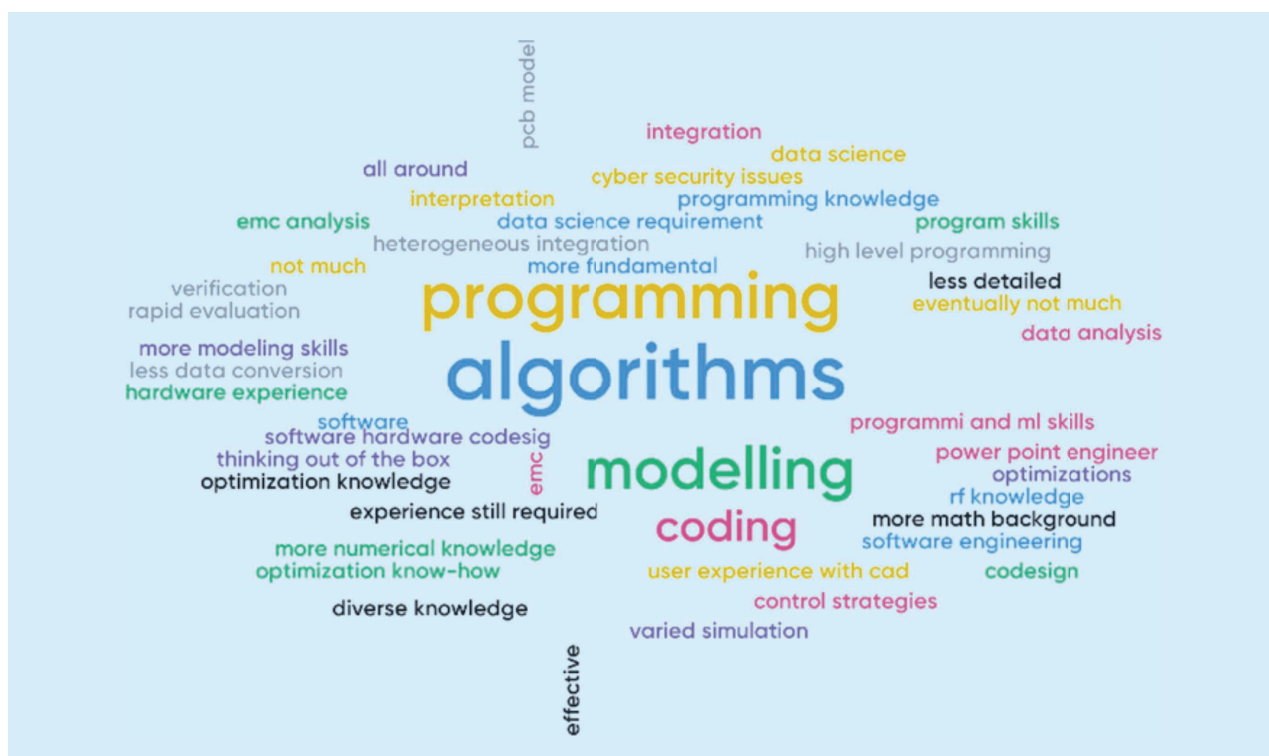


FIG 4 A word cloud of responses to the online voting question: What are the future skills of PED engineers?

to that track. The second is that *IEEE Open Journal of Power Electronics (OJ-PELS)* is interested in articles in this area, and authors are encouraged to submit. *OJ-PELS* is a rapid-turn publication with a seven-week submission-to-publication goal. It began publishing in January 2020.

About the Authors

Kevin Hermanns (kevin.hermanns@pe-systems.de) graduated from the Technical University Braunschweig, Germany, in 2013. He is the general manager of PE-Systems GmbH and a member of the Design Automation for Power Electronics Initiative within the IEEE Power Electronics Society. He started his professional career at Siemens and has worked as a research associate at the Technical University Darmstadt in the Power Electronics Department. During that time, his research interests were mainly focused on the distortions of high-power converters. He is active in several national and international standardization groups in the field of power electronics.

Yarui Peng (yrbpeng@uark.edu) received his B.S. degree from Tsinghua University, Beijing, in 2012 and his M.S. and Ph.D. degrees from the Georgia Institute of Technology, Atlanta, in 2014 and 2016, respectively. He is an assistant professor in the Computer Science and Computer Engineering Department at the University of Arkansas and leads the Energy-Efficient Electronics and Design Automation Lab. His research focuses on computer-aided design for multichip heterogeneous integration and high-efficiency power electronics. He studies methodologies and algorithms for signal integrity and reliability optimizations in 2.5D and 3D

integrated circuits and develops design automation tools for power electronics layout synthesis and electrothermal-mechanical optimizations.

Alan Mantooth (mantooth@uark.edu) received his B.S. (summa cum laude) and M.S. degrees in electrical engineering from the University of Arkansas, Fayetteville, in 1985 and 1986, respectively, and his Ph.D. degree from the Georgia Institute of Technology, Atlanta, in 1990. He is an IEEE Fellow and the immediate past president of the IEEE Power Electronics Society (PELS), and editor-in-chief of *IEEE Open Journal of Power Electronics*. He is a distinguished professor in the Electrical Engineering Department at the University of Arkansas, where he is also the 21st-century research leadership chair in engineering. He helps lead the PELS initiative on design automation and spent eight years at Analog working in the modeling group for the Saber simulator. He continues research in this area in the field of power electronics.

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