Development of EDA Techniques for Power Module EMI Modeling and Layout Optimization

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Abstract

The design of power electronics modules is undergoing renewed interest as new challenges and technologies emerge in the realm of wide bandgap (WBG) power device packaging. In order to meet the demands of these high-speed transistors, novel techniques are required to produce modules with reduced parasitics and noise generation without exceeding the operating temperature of the devices or their packaging materials. Traditionally, power module design has been a highly iterative process—repeatedly reworking and simulating designs using finite element analysis (FEA) tools that require considerable time in terms of both labor and computation. To overcome these issues, an electronic design automation tool (EDA) known as PowerSynth is ongoing in its development toward power module layout synthesis and optimization based on electrical and thermal criteria. In this paper, work to extend the capabilities of PowerSynth to optimize layouts with reduced electromagnetic interference (EMI) is presented. Optimization strategies based on the transfer functions of noise propagation paths are introduced and results showing layouts with reduced noise generation are compared with FEA simulations.

Key words

Electronic Design Automation (EDA), Electromagnetic Interference (EMI), Power Modules, Packaging, Wide Bandgap (WBG) Devices

I. Introduction

As wide bandgap (WBG) devices such as silicon carbide (SiC) and gallium nitride (GaN) transistors continue to develop and open more application areas, new packaging solutions are necessary in order to take full advantage of the benefits these devices offer [1], [2]. In the area of power electronics, WBG devices promise greater switching frequencies at higher voltages and temperatures than their silicon counterparts. These advantages can lead to a reduction in the size of passive components or cooling system requirements [3]. However, faster switching speeds lead to larger di/dt or dv/dt in the power loop—interacting with package parasitics and leading to oscillations in device voltages and currents that contribute to electromagnetic interference (EMI) [4], [5]. Similarly, as power module packages tend towards higher density designs, proper placement of devices becomes critical to avoid mutual heating effects and mitigate thermal management issues [6]. These concerns require careful evaluation of the trade-offs associated with power module layout and die placement in the early stages of package design. Since designing electronic packages is a multi-domain problem, common approaches make extensive use of finite element analysis (FEA) and transient circuit simulation to predict the electro-thermal response for a given physical design[7]. However, this can be computationally expensive and places a large burden on the designer in preparation for FEA simulations. To overcome these issues, this team continues to develop an electronic design automation (EDA) tool—PowerSynth—for power module layout using reduced-order models in a multi-objective optimization framework.

In its current iteration, PowerSynth takes input from the package designer in the form of a simplified layout and design rules as specified by a manufacturer design kit (MDK)[8]. PowerSynth then uses a genetic algorithm to alter trace geometry and die placement with goals including minimization of electrical parasitics and device junction temperatures. Estimation of package parasitics is performed using response surface modeling (RSM) techniques where pre-computed parasitics data are fit to a function based on trace geometry and spatial position[9]. Similarly, die temperature rise is predicted using a fast thermal model characterized using a single FEA simulation which is then reduced to a 1-D thermal impedance network with additional

thermal resistances accounting for relative locations among devices and trace edges[10]. The performance of both the electrical parasitics model and thermal model has been verified through simulations and physical measurements to show good agreement among the results while reducing computation time by up to three orders of magnitude[11]. Using these models within its optimization framework allows PowerSynth to then present users with hundreds of candidate-designs along a Pareto frontier within minutes. Selected solutions can then be exported to several commercial FEA tools or as a parasitics netlist for further analysis and verification before prototyping. Additionally, by using an MDK, only feasible designs are among those reported to the user—further reducing time and overhead associated with the early stages of physical design.

As the development of this tool has progressed, the need to incorporate EMI-aware layout design has become of greater interest. To this end, research has begun on incorporating models and methods to produce layouts with reduced EMI noise generation while simultaneously accounting for impact on device temperature and overall parasitics.

The goal of this paper is to develop a generalized method for evaluating candidate layout solutions based on their effectiveness at minimizing conducted emissions at the module input—regardless of external dependencies such as switching frequency, duty cycle, load, etc. In Section II a brief literature review serves to address how conducted EMI is typically modeled in power electronic systems as well as some of the impacts module layout has on generated noise. From there follows a discussion on modeling methods and cost functions used in this work to optimize layouts toward decreased noise generation. After that, Section III presents the results of layout optimization and compares them to those from simulations. Finally, Section 0 concludes with observed limitations in this approach and outlines future work to improve and extend these techniques.

II. Conducted EMI Modeling for Layout Optimization

A. EMI Modeling and Layout Effects

The capability to accurately predict the noise generated by power electronics systems is of high value to designers in their efforts to reduce the amount of iterative simulation and prototyping required before a product can pass compliance tests. Most often, this can be accomplished to varying degrees by separating a converter or inverter system into separate high-frequency equivalent circuits for the differential mode (DM) and common mode (CM) noise propagation paths as detailed in [12]–[15]. For example, a typical converter system including line impedance stabilization network (LISN), dc link and bus bars, and power module is shown in Fig. 1 with the corresponding equivalent DM and CM noise paths shown in Fig. 2 (a) and (b), respectively. Here the noise voltages for the DM and CM paths can be expressed by those observed at the LISN as V_{DM} and V_{CM}, respectively, in (1) and (2) below.

$$V_{DM} = \frac{V_{LISN,1} - V_{LISN,2}}{2} \tag{1}$$

$$V_{CM} = \frac{V_{LISN,1} + V_{LISN,2}}{2} \tag{2}$$

Additionally, each of these noise voltages can be expressed as a transfer function associated with their respective propagation paths. In both cases, the switching device is replaced by either a voltage or current source and is combined with the module and system parasitics to form the specified transfer function. For the DM propagation path, this is defined as

$$V_{DM} = I_D Z_{Tr} \tag{3}$$

where I_D is the switching current through the device and Z_{Tr} is the transfer impedance along the DM path to the LISN. Similarly, for the CM propagation path,

$$V_{CM} = V_{DS} G_{CM} \tag{4}$$

where V_{DS} is the voltage being switched and G_{CM} represents the voltage gain across the propagation path to the LISN. One method for defining the aforementioned values is detailed in [16] where switching voltages and currents are represented in the frequency domain as the Fourier transform of a trapezoidal wave while the remaining transfer coefficients are populated via parasitic extraction using FEA.

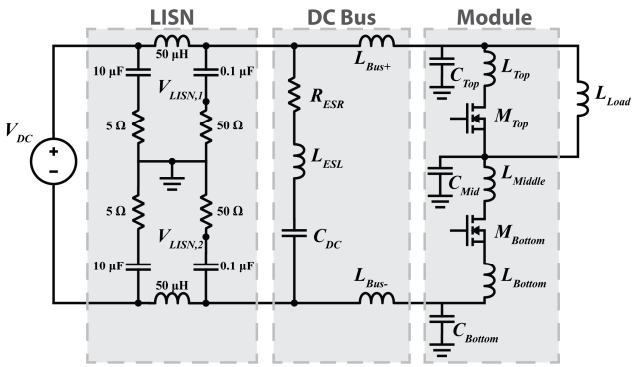

Fig. 1. Converter system overview including LISN, DC bus, and module components.

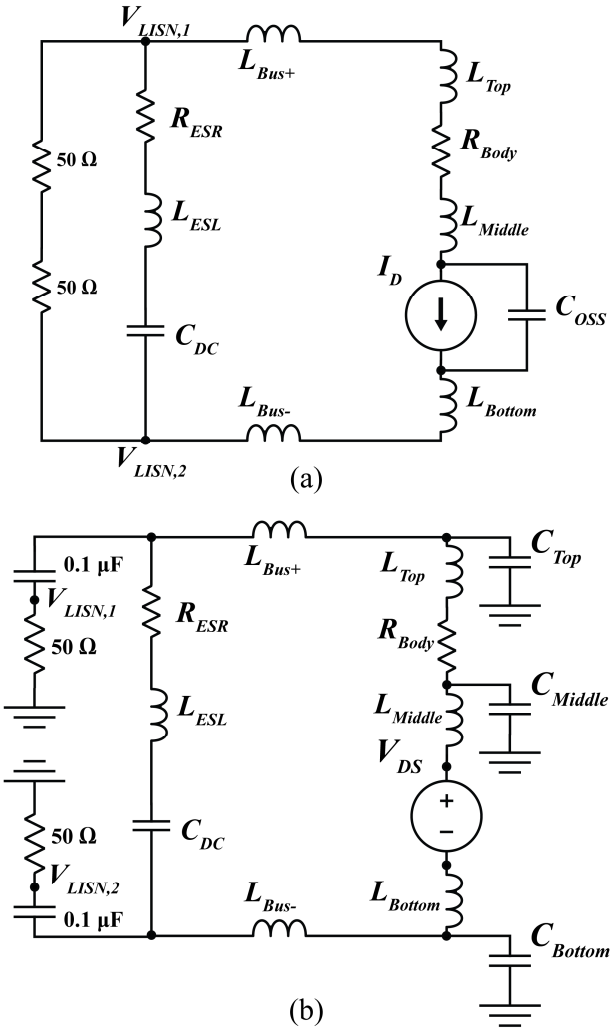

Fig. 2. High frequency equivalent circuits for (a) DM and (b) CM noise paths of the converter in Fig. 1.

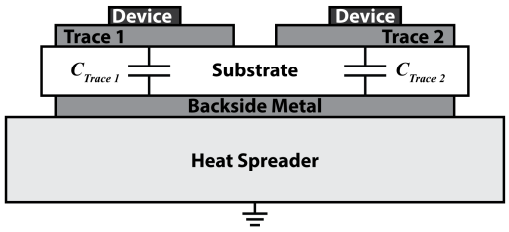

Fig. 3. Illustration of a power module cross section with trace capacitances and their coupling to ground.

Using these high-frequency equivalent circuits, the degree to which the layout of a power module affects EMI can be summarized as follows. The DM propagation path is characterized by the overall loop inductance—including both the module and dc bus—and has a local maximum at the resonance frequency formed by the loop inductance and output capacitance, C_{oss}, of the switching device. Whereas the CM noise path is dependent upon the capacitive coupling between conductors and ground. The coupling effect of traces to ground is explored in [15] where the authors evaluate several iterations of a layout design to show reduction in EMI by minimizing stray capacitances within the layout. The trace-to-ground capacitances found in a power module layout are illustrated in Fig. 3

B. Proposed Method

The techniques outlined in the previous section have been expanded upon to work within the multi-objective optimization framework of PowerSynth. To achieve this, and to allow for a generalized approach with reduced computational effort, several assumptions have been made. First, only the device C_{oss} and layout-specific parasitics are considered—system interconnects and load are not represented. Furthermore, other parameters such as duty cycle and turn-on and turn-off times of the devices are neglected. The rationale behind this is because PowerSynth only attempts to optimize module layouts rather than complete systems. So, by optimizing toward layouts with reduced EMI and parasitics, the designers may choose the best candidate layout for their applications.

Reduction of DM noise generation at the layout level requires minimization of the module loop inductance as stated in the previous section. PowerSynth already excels at this type of optimization as reported in [9] and [11]. Thus, its existing parasitic extraction capabilities are leveraged here. Additionally, when extracting a parasitic netlist of module layout, PowerSynth currently estimates trace capacitance as

$$C = \frac{\epsilon A}{d} \tag{5}$$

where ϵ is the permittivity of the substrate, A is the area of the trace, and d is the thickness of the isolation material.

To establish a cost function for CM reduction during layout optimization, a simple circuit solver based on modified nodal analysis (MNA) [17] has been developed for this tool. This solver takes the form of

$$\mathbf{TX} = \mathbf{W} \tag{6}$$

where $\mathbf{T}$ is a matrix representing the parasitic components and $\mathbf{X}$ is a vector to be populated with unknown voltages and currents and $\mathbf{W}$ is a vector containing source values. Furthermore, $\mathbf{T}$ is defined as

$$\mathbf{T} = \mathbf{G} + s\mathbf{C} \tag{7}$$

where $\mathbf{G}$ contains frequency-independent components and conductors and $\mathbf{C}$ holds values for capacitors, inductors, and other frequency-dependent components.

Inside the optimization routine, PowerSynth populates the **T** matrix with extracted layout-parasitic values. In order to obtain the frequency response of the CM transfer function, an ac voltage source of 1 V is inserted into the **W** vector and the system of equations is solved over the frequency range of interest—with points spaced geometrically across this range to establish a representative sampling with as few points as possible. Once this transfer function has been solved, the average of the magnitude of the voltage gain of the CM propagation path is used as the CM cost function metric to be minimized during optimization. It is worth noting that, while forming a distributed netlist, the extracted parasitics used in this evaluation do not constitute an accurate broadband model. So, at frequencies greater than approximately 30 MHz, this method continues to show the trend in CM noise generation but cannot predict levels accurately. Examples of this approach and results are presented in the following section.

III. Model Validation

A. PowerSynth Layout Optimization

To demonstrate results using this approach, a simple, half-bridge module layout with a single device per switching position has been optimized in PowerSynth. Module dimensions are 40 x 50 mm and the power devices are mounted on a direct bond copper (DBC) substrate. For this setup, optimization goals are set to measure overall loop inductance from the DC+ to DC- terminals of the module as well as the average of the CM voltage gain transfer function. During the optimization routine, PowerSynth uses widths and lengths of traces as well as device positions as design variables for the NSGA-II genetic algorithm [18] with the loop inductance and CM gain average as cost functions. Throughout this process, the MDK serves to enforce constraints on the design variables by evaluating each layout to ensure DRC-clean solutions without overlapping components are produced. In total, 2201 layouts are generated and evaluated in 3675 seconds on an Intel® Core™ i7 when optimizing this design for trade-offs in CM voltage gain versus loop inductance. Of the 2201 generated layouts, 228 solutions are shown in Fig. 4 (a). From the remaining 228 solutions, three have been chosen for further evaluation as illustrated in Fig. 4 (b). The CM transfer functions for these three layouts obtained by the MNA solver are shown in Fig. 5. Here, 50 frequency points are spaced geometrically between 10 kHz and 100 MHz to establish the CM cost value associated with each layout. These three layouts are then automatically exported to a simulated EMI testbench for further validation.

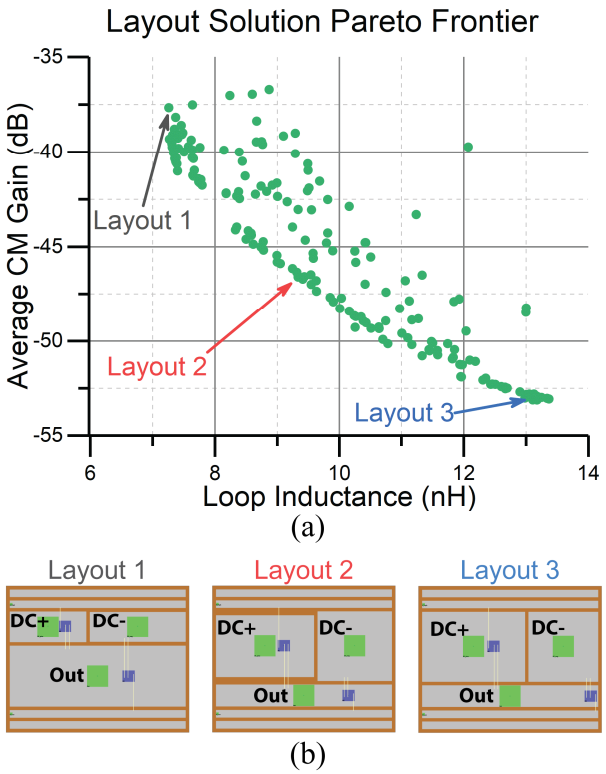

Fig. 4. (a) Pareto frontier of layout solutions generated by PowerSynth and (b) illustrations of the selcted layouts for evaluation.

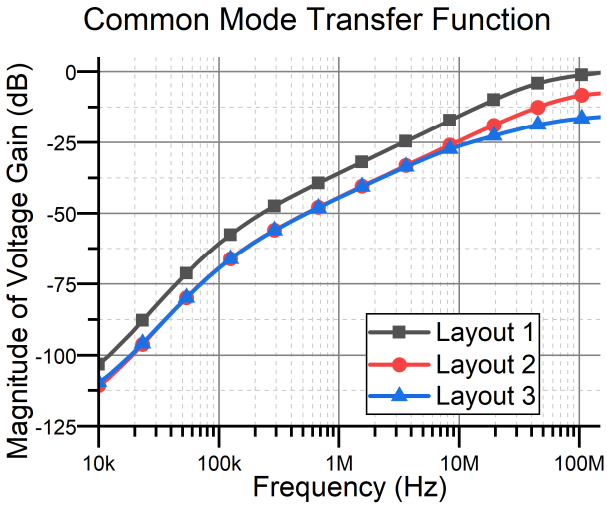

Fig. 5. Plots of the CM voltage gain transfer functions for the selected layouts in Fig. 4.

B. Simulated EMI Testbench

A simulated EMI testbench has been established to aid in rapid validation of PowerSynth-generated layout solutions. An overview of this testbench is presented in Fig. 6. Layouts exported from PowerSynth are then imported into a commercial, full-wave FEA solver. The results of this 3D electromagnetic simulation are used to construct an S-parameter model of the power module layout with ports

representing each of the interconnects and device pads. Next, this S-parameter model of the power module is combined with the rest of the system components in a transient circuit simulation. This also includes physics-based device models for the SiC MOSFETs[19] employed in this study. After the transient simulation is completed, spectral analyses of the generated noise voltages are obtained by taking the FFT of the LISN voltages.

In this study, the circuit evaluated using the EMI testbench is a clamped inductive load test. The switching frequency of the device is set to be 25 kHz with a 50% duty cycle and load current of 10 A with a 600 V DC bus. Comparison of these results with the PowerSynth layout optimization is presented in the next section.

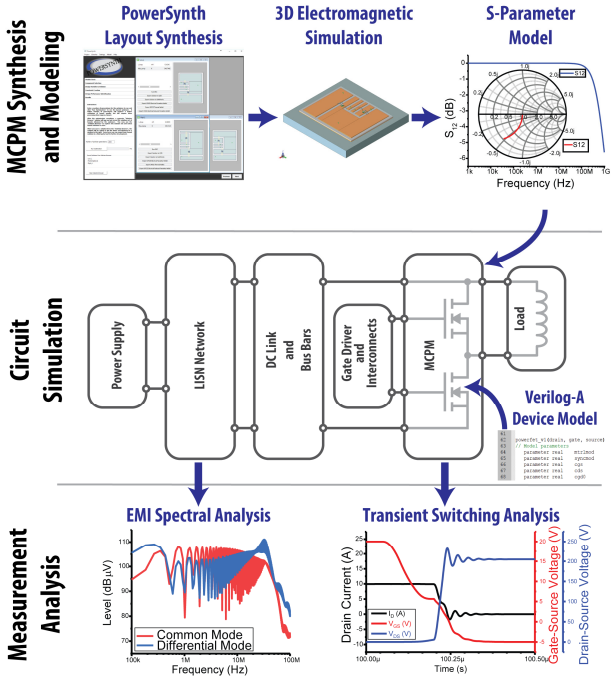

Fig. 6. Overview of the simulated EMI testbench used in evaluating PowerSynth-generated layout solutions.

C. *Comparison of Results*

As shown in Fig. 4 and Fig. 5, Layouts 2 and 3 exhibit lower CM noise levels than that of Layout 1. On further inspection, the level of the CM transfer function for both Layout 2 and Layout 3 are nearly coincidental except for higher frequencies. However, Layout 3 has a higher loop inductance than Layout 2. Comparing these results with the CM results obtained by the simulated testbench confirms the trend in CM noise level reduction made by PowerSynth during optimization. At their peak CM noise values, both Layout 2 and Layout 3 are approximately 6.5 dB less than layout 1 in this scenario. The effects of this reduction can be seen in Fig. 8 where the peak CM current is reduced from 0.66 A in Layout 1 to 0.33 A in Layouts 2 and 3. Also of note is that Layout 3 exhibits the lowest CM noise level at frequencies above 50 MHz, indicating that it may also perform better at reducing radiated emissions.

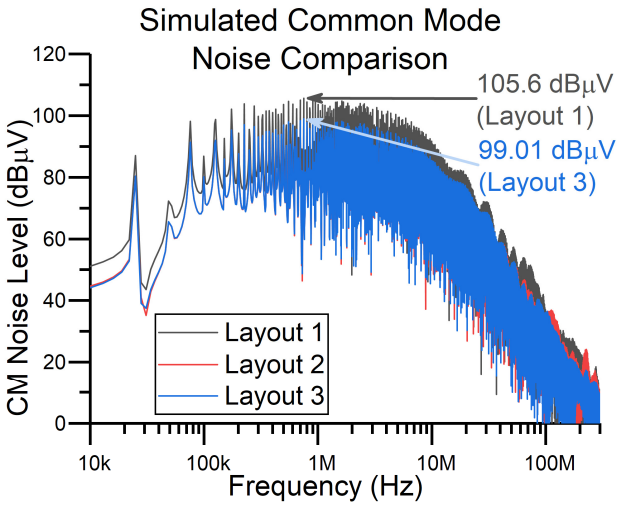

Fig. 7. Comparison of CM noise level results among the layouts evaluated using the simulated EMI testbench.

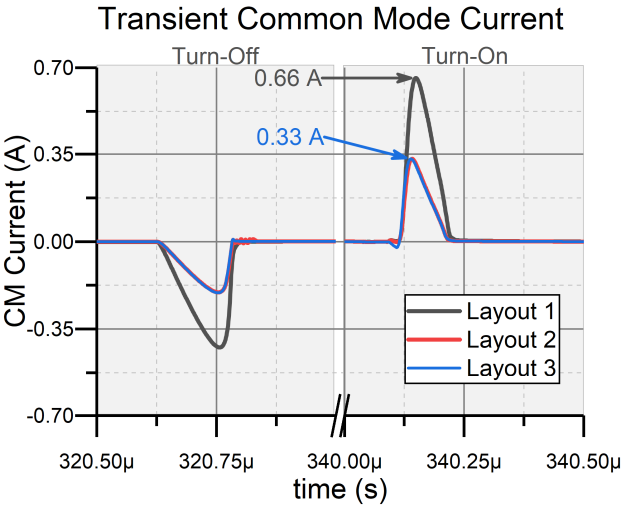

Fig. 8. CM current results for each layout obtained from transient simulation using the EMI testbench.

DM noise level comparison results are also obtained using the simulated EMI testbench and presented in Fig. 9. In this case, the three layouts exhibit similar noise levels from the low frequency range until approximately 10 MHz where they begin to diverge. In the high frequency region, Layout 3 has the highest DM noise levels while Layout 1 has the lowest. For example, at 28 MHz, the DM magnitude of Layout 3 is 75.6 dBµV whereas that of Layout 1 is 72.1 dBµV. From these results, a designer may consider choosing layout 2 for their application since it represents a solution with a trade-

off in loop inductance—or DM noise, as is also the case—that maintains a low CM noise level throughout the conducted EMI region.

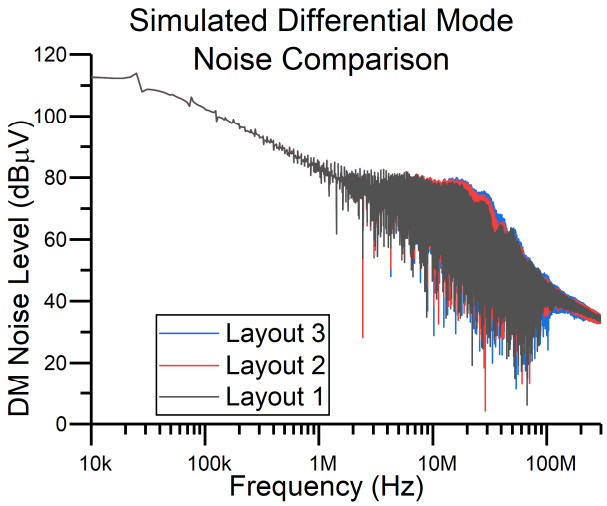

Fig. 9. Simulated EMI testbench results comparing DM noise levels among the selected layouts.

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IV. Conclusion

By including CM noise reduction in the layout optimization routine, PowerSynth now has the capability to better inform the designer on trade-offs in die placement and routing that go beyond the loop inductance and thermal tradeoffs explored in the past. The method established in this work allows PowerSynth to detect the trends in noise generation associated with layout geometry by examining the transfer function of the CM voltage gain. Continued development of the techniques presented here will be used to extend this functionality further by allowing designs with a plurality of devices in parallel to be optimized. Furthermore, in cases with paralleled devices and by considering the substrate isolation thickness as a design variable, additional tradeoffs between thermal performance and CM noise generation can be realized. These designs will eventually be fabricated and tested to better determine the accuracy of this method and that of the simulated EMI testbench. Finally, as both module design and PowerSynth are trending towards 3D and heterogeneous layouts, further improvements to this model will be made to capture capacitive coupling effects among traces and to ground.

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