PEEC Method and Hierarchical Approach Towards 3D Multichip Power Module (MCPM) Layout Optimization

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***Abstract*— Recent advances in packaging technologies have improved multichip power module (MCPM) power density through innovative designs with layout size reduction, multi-layer stacking, and heterogeneous components integration. As these layout designs are getting denser, signal integrity issues due to mutual couplings demand more consideration. Hence, in order to handle these new layouts in the power module design automation tool—PowerSynth, a new electrical model has been developed based on the PEEC method. This method provides further insights into electrical reliability during optimization by evaluating current density and electric field inside each conductor. A coarse meshing process is applied to every generated layout to ensure accurate parasitic extraction while maintaining efficient computation time. Furthermore, a hierarchical approach has been applied to form connections between traces and components during placement to evaluate electrical parasitics without increasing the number of mesh points. Comparisons versus FEA simulation tools and experiments have shown promising initial extraction results using this model.**

Keywords—MCPMs, parasitics, layout optimization

I. INTRODUCTION

Nowadays, the increased applications of wide bandgap (WBG) devices such as SiC and GaN in MCPMs have enabled high voltage, high current and fast switching power electronic circuits. At high switching frequencies, electrical parasitics are one of the most important metrics for MCPMs designs. This is because these unwanted elements can lead to voltage overshoot, current imbalance, and increased switching losses, which in turn reduce the reliability and achievable performance of the power electronic circuits they comprise. To overcome these issues, recent studies in MCPM design automation in [1] and [2] have applied fast extraction techniques to estimate parasitics values during layout optimization. In [2], the method of moments (MoM) calculations are first applied to extract current results. These results are then used in a boundary element method solver to extract loop inductance. More recently in PowerSynth [1], a response surface model is built prior to the layout optimization process for self-inductance and resistance of rectangular conductors to overcome the dimension ratio limitations of analytical equations. This method has been used along with a Laplacian matrix solver and has been shown to yield accurate loop parasitics approximation. Both of the methods above, however, do not consider the impact of mutual inductance coupling—which is of critical importance as MCPM package designs become ever denser. Hence, a new method needs to be developed for the PowerSynth layout optimization tool (Fig. 1).

To illustrate the impacts of parasitic coupling, two double pulse test (DPT) simulations with and without the inclusion of mutual inductance have been run using an extracted netlist from FastHenry for the layout in Fig. 2-a. M1 and M2 are always off with a -5 V gate-source bias voltage, while a 50 kHz pulse signal from -5 to 20 V is applied to the gates of M3 and M4. In Fig. 2-b, a difference in false turn-on voltage in the gate-source signals of up to 50% has been observed in the two cases. Also, it is worth mentioning that, as new packaging technologies have allowed multi-layer DBC stacking and integration of gate drivers within the MCPM, mutual couplings between conduction paths will also become more important. In practice, some layout designs have taken advantage of magnetic field cancellation in current paths that conduct in opposite directions to minimize the overall loop inductance [3], [4]. Therefore, consideration of mutual coupling is crucial for a good layout optimization cost function.

Besides mutual coupling, current density inside conductors and the electric field between conductors are other concerns for

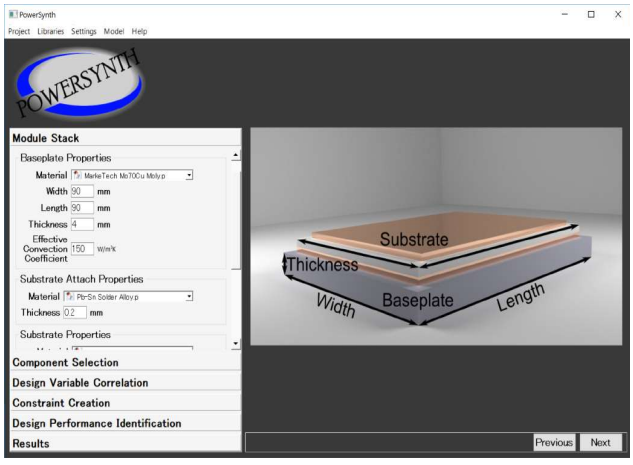

Fig. 1. PowerSynth layout optimization tool [1].

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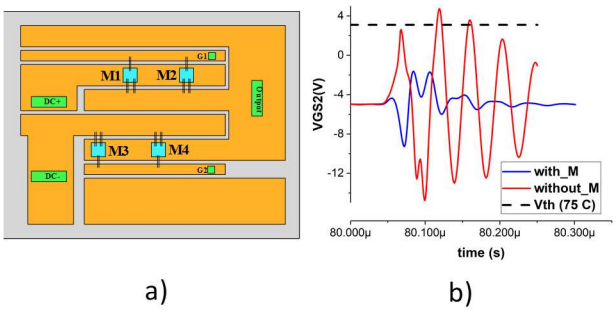

Fig. 2. a) Half bridge layout b) Mutual coupling impact on gate signal.

a reliable MCPM design. Advances in WBG devices also enabled high voltage applications up to 15 kV [5]. Such high-voltage operation demands more reliability consideration such as partial discharge and dielectric breakdown [6]. One practical solution for partial discharge is applying appropriate isolation materials with high dielectric strengths between traces in the layout. Furthermore, recent studies from [7] and [8] have shown some alternative solutions. In [7], it was demonstrated that by adjusting the amount of trace filleting the peak electric field magnitude between adjacent conductors can be reduced. Future work on this study will provide a partial discharge awareness model for determining the appropriate fillet radii within the layout design. More recently, an approach in [8] has shown that by using a reliability-aware layout constraint technique, appropriate spacing can be applied between two conductors of different voltage to prevent breakdown. To further improve layout reliability in PowerSynth, layout current density and voltage distribution based on electrical modeling are necessary. While the existing PowerSynth electrical model as described in [1] provides fast and accurate loop parasitics results, the Laplacian matrix approach cannot solve for voltage distribution and electric field information. As such, a new electrical model is required for improving reliability with layout optimizations. Some studies in other literature have shown that the Partial Electrical Equivalent Circuit (PEEC) method [9] has the most potential for this target.

The method described in this work provides a suitable solution for accurate loop parasitics calculation taking into account mutual coupling along with voltage and current distribution. All of this is possible while having a reasonably fast computation time suitable as an optimization cost function within PowerSynth.

II. Methodology

A. *Limitations of the Current Method in PowerSynth*

As briefly mentioned above, the existing method in PowerSynth is based on a Laplacian matrix solver to estimate loop resistance and inductance results over a discrete frequency range. Due to the similar linearity between R and L, this technique has been used for a fast and accurate approximation for loop inductance and resistance. However, since inductance is sensitive to the current path, some overestimation has been shown when using the effective resistance technique to approximate loop inductance values. To overcome this issue, a heuristic model has been used in [10] to apply correction values due to the current crowding effect at trace corners. While this has shown a more accurate solution for loop inductance approximation, there are several drawbacks. Firstly, this method is not general since it requires solving for the corner correction model for every different layout input. Secondly, this model depends on a previous version of layout representation in PowerSynth refeed to as a symbolic layout. This symbolic layout data structure consists of line and point objects, where the line objects define a single current direction either horizontally or vertically. As such this model can only handle layouts with multiple, uni-directional current paths. Fig. 3 below shows a simple layout where the existing method cannot accurately predict the current path of the 2D planar structure. This results in overestimation in extraction due to the longer conduction path (A→B). Finally, the prior method does not account for mutual coupling among nets, which is important in some 2D and 3D layouts. For instance, given the layout in Fig. 4 a) and b) the existing model would give the same results for loop-inductance in both cases. However, due to the mutual inductance impact, loop b) has a smaller loop inductance value due to a smaller current loop area. In the next sections, by combining the PEEC method with response surface techniques, most of these limitations can be overcome.

B. *PEEC Modeling Overview*

A brief overview of the PEEC method [9] along with its capabilities to solve loop parasitics while providing current and voltage information is described here. There are several advantages to the PEEC method. To start with, this method can be used to automatically determine the current loop for arbitrary layout geometries, which is often hard to determine analytically in several problems. On top of that, distributed voltage and current information can be obtained through Modified Nodal Analysis (MNA). This information can be used to evaluate current density and near field values in the post-extraction

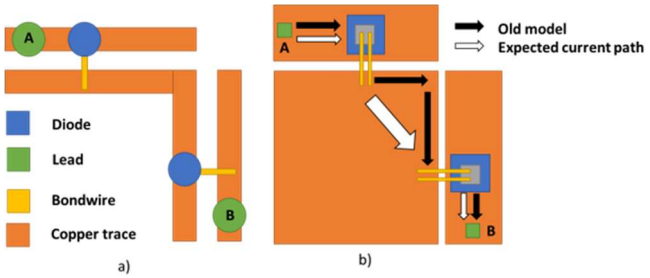

Fig. 3. a) A symbolic layout representation b) expected layout solution.

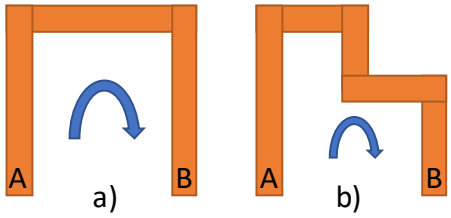

Fig. 4. Mutual inductance impact.

$$\begin{bmatrix} G+sC & A \\ A^T & -(R+sL) \end{bmatrix} \begin{bmatrix} \Phi \\ I \end{bmatrix} = \begin{bmatrix} I_i \\ V_i \end{bmatrix}$$

Fig. 5. PEEC matrix representation.

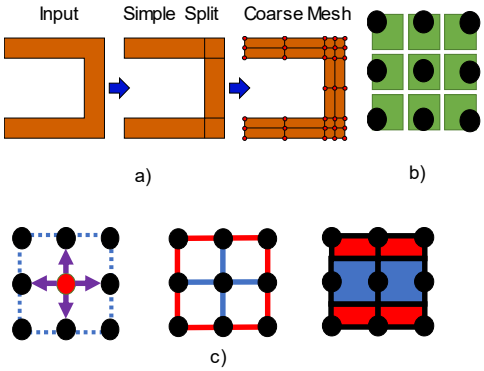

Fig. 6. a) Discretization steps b) edge formation steps c) capacitance cell formation.

analysis. Finally, since each discretized conductor piece contains self-inductance, resistance, and capacitance information, a distributed netlist can be easily obtained for accurate transient or broadband AC analysis. There are three main steps in formulating a PEEC model: Discretization of the input, matrix stamping, and circuit solution. This section focuses on the matrix stamping and circuit solution techniques while the layout input discretization is described in more detail in Section C.

The matrix stamping for PEEC requires five main matrices which are (**G+sC**): the conductance and capacitance matrix, **A**: adjacency matrix, (**R+sL**): resistance and inductance matrix, $\mathbf{I_i}$**:** input current sources and $\mathbf{V_i}$: input voltage sources. As can be seen in Fig. 5, for the parasitic extraction application, normally R and L elements can be lumped into one single branch and stored in the (**R+sL**) matrix. This reduces the number of nodes significantly and improves the matrix evaluation time.

In loop parasitic evaluation, another common approach is to evaluate loop R and L results separately from C. Using this fact, the matrix solution can be further reduced, since it is not necessary to compute all node voltage (Φ) and branch current (I) solutions. This can be solved separately using Eqs. (1) and (2) below:

$$[(\mathbf{G}+\mathrm{s}\mathbf{C})+\mathbf{A}(\mathbf{R}+\mathrm{s}\mathbf{L})\mathbf{A}^{\mathbf{T}}]\Phi = \mathbf{I_i} + \mathrm{A}(\mathbf{R}+\mathrm{s}\mathbf{L})^{-1}\mathbf{V_i}] \quad (1)$$

$$[(\mathbf{R}+\mathrm{s}\mathbf{L})+\mathbf{A}^{\mathrm{T}}(\mathbf{G}+\mathrm{s}\mathbf{C})^{-1}\mathbf{A}]\mathrm{I} = -\mathbf{V_i} + \mathbf{A}^{\mathbf{T}}(\mathbf{G}+\mathrm{s}\mathbf{C})^{-1}\mathbf{I_i}] \quad (2)$$

When only the loop R and L solutions are considered, the (**G**+s**C**) matrix is zero. Hence, (2) can be used to evaluate branch current solutions with one single input voltage source. Using the branch current information, the current density can be evaluated via the mesh geometry parameters. The electric field inside of the conductor can also be evaluated using Ohm's law:

$$E = J/\sigma \quad (3)$$

Where J is current density (A/m^2) and σ is the conductivity of the material (S/m).

C. *Proposed Methodology*

Compared with layout designs in VLSI applications, power module layouts usually contain significantly fewer nets. However, the physical size of MCPM conductors is much larger than their skin-depth. As a result, the PEEC method requires a relatively large number of mesh points in order to yield accurate parasitic extraction. This would be computationally expensive and therefore unfavorable as an optimization cost function inside PowerSynth. To overcome this problem while ensuring a good approximation, first a coarse and uniform mesh is used to discretize every layout input into edges and nodes. During this step, widths and lengths are assigned to each edge on the mesh. Once the coarse meshing process is complete, an interpolated model using a response surface method [10] is used to find self-resistance, self-inductance, and self-capacitance of each edge. The partial mutual inductance is then computed between every parallel edge while ignoring the orthogonal pairs. To handle device connections, a hierarchical representation is used to store the trace group information. Finally, the PEEC evaluation can be applied to performed loop extraction and current density evaluation of the layout. The above-mentioned evaluation processes are designed and programmed in Python.

1) Discretization

The model takes layout input through a planar data structure, where each plane is a rectangular object with thickness and elevation. As seen in Fig. 6a, based on the shared edges between input traces, an algorithm is used to perform a simple geometrical split, where each new trace always has one shared edge with another. In such a way, a uniform mesh (n x n) can then be applied to all planes and form a coarse mesh. The node and edge forming process are illustrated in Fig. 6b. To begin with, all mesh nodes are separated into two groups: internal or boundary, where the boundary nodes are nodes located on the trace group perimeter. During this process, each node is assigned to a unique node index and connected with its North, South, East, and West neighbor through an edge object. This edge data structure stores the width and length information of each trace. These width and length values are assigned as follows: For each pair of nodes, an edge is defined as an internal edge if one internal node is presented. Otherwise, if both nodes are of boundary type, a boundary edge is defined. The widths of boundary edges are always smaller than those of internal edges, giving a good approximation for skin effect. These internal and boundary edges also serve as an input to evaluate capacitance cells located at each node. For every node, half of the edge-length to each of its neighbors is used to form a bounding box area as seen in Fig. 6c. This information is later used to calculate the capacitance of the node to ground and also between every other node in multilayer cases.

2) RLCM Evaluation

Once width and length values are updated for all edges, accurate self-resistance and self-inductance can be computed through the response surface model described in [10]. The design space of this response surface model is based on the

layout floorplan dimensions, number of mesh elements, and operating frequency range. It is worth mentioning that, since self-parasitic values are a function of frequency, they also provide a reasonable approximation for the skin-depth effect. Once all self-parasitic values are stored into their respective edge objects, the mutual inductance between every edge pair is computed using Eq. (14) in [11], which takes width, length, thickness, and separation distance in both the horizontal and vertical directions for two rectangular bars as inputs. Since there are multiple pairs sharing the same mutual coupling value. A table is formed during this process to make sure these values are computed only once.

When parasitic capacitance is included in the analysis for a full PEEC evaluation, and the layout has multiple layers, the capacitance cells are first created for both layers as described above. When an irregular mesh is applied for all trace groups, mesh nodes on two different layers are usually not aligned with each other. Hence, to compute the capacitance between two nodes in the z-direction, an algorithm will automatically find any overlapping region between two capacitance cells as seen in Fig. 7. This overlapping area along with the substrate thickness between two nodes is used to compute parasitics capacitance between them.

3) Device Handling Through Hierarchical Consideration

Several power module topologies, such as a full-bridge or three phase inverters, usually have identical layouts for each switch-leg. Hence, it would be beneficial to consider a hierarchical representation for this electrical model. A hierarchical representation has shown several other advantages for power module layout. To start with, discretization can be performed individually for different nets to reduce the total number of mesh elements. Furthermore, loop parasitics of different nets can be solved individually where a divide-and-conquer approach can be later applied to speed up the extraction time for more complicated structures. Finally, this method allows generic component connections through multiple sub-graphs. A zero-thickness plane object is used to represent the pad connections for each device. From the input layout information, an algorithm is used to form the relationship between traces and pad to form a hierarchical tree. Fig. 8a shows a simple 3D layout and Fig. 8b shows its corresponding hierarchical tree structure. For each trace group, a uniform mesh is first applied. Then, a special hierarchical edge is formed to connect a device pad to its closest mesh nodes (Fig. 9). Since these hierarchical edges have not been assigned R or L values, effective R and L values are then calculated based on a linear approximation between the hierarchical edge and its neighbors

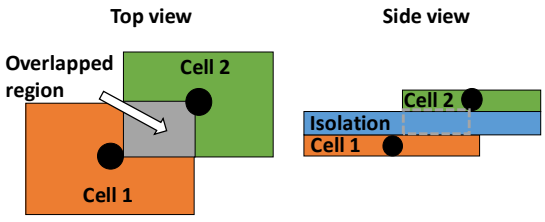

Fig. 7. Parasitics capacitance between two layers.

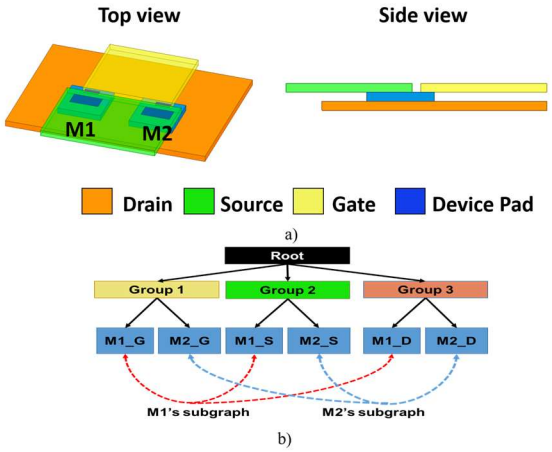

Fig. 8. a) Simple layout input b) hierarchical tree structure.

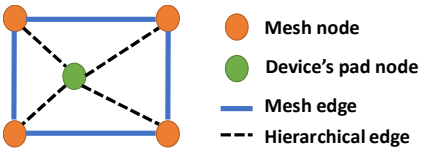

Fig. 9. Hierarchical edge concept.

based on their length to length ratio. To handle bondwires and external connection, a sub-graph is used to represent each device. Each edge on this sub-graph contains parasitic values between every two terminals.

Once all parasitic values are updated for hierarchical edges, an iterative process will add each node index to the PEEC matrix. Element stamping is performed for every edge to update the **(G**+s**C)** and **(R**+s**L)** matrices. The adjacency matrix (**A**) can be formed easily through graph representation. During this step, a positive current direction is defined from West to East and South to North. This would ensure correct signs assignment for the adjacency matrix. The matrix is then solved using a sparse matrix library.

III. Validation Results

Three different scenarios have been chosen to validate the model: Current density versus frequency comparison with FEA, s-parameter coupling comparison with VNA measurement, and a loop evaluation for a half-bridge module compared with impedance analyzer results.

A. *Current Density Validation*

A simple 10 mm x 10 mm U-shaped structure is designed to show current density comparison. The same layout is designed in ANSYS HFSS, where a 1 V sinusoidal signal is applied to the input port and a 50 Ω load resistance is connected to the output. The current density map is captured at dc, 100 kHz, and 100 MHz. Fig. 10 shows the current density map using this model versus HFSS at these frequencies. The results show that current density is quite uniform at dc, becoming more crowded at the 90-degree corners as operating frequency increases. The current crowding effect from the model has shown good

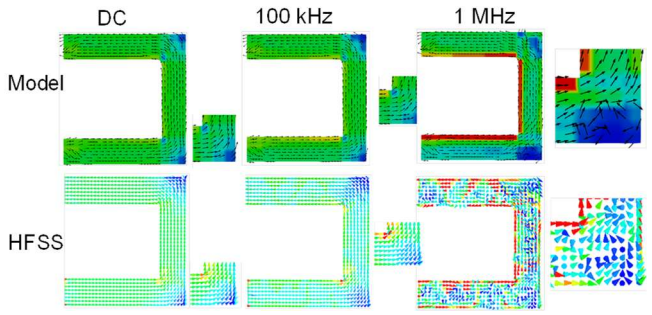

Fig. 10. Current density comparison.

agreement versus HFSS results. Table. I shows the evaluation time comparison between the approximate model and HFSS simulation where this model evaluates up to 6000 times faster.

B. *S-parameter Extraction for Coupling Validation*

In order to verify coupling between nets, a simple four-port PCB structure (Fig. 11) is designed and fabricated using 1 oz. copper on an FR-4 substrate. Four SMA connectors are used to interface with each port of the test structure. Fig. 12 shows the measurement setup for s-parameter extraction using a Keysight E5061B vector network analyzer (VNA). A Keysight ECAL N4431B is used to perform a necessary two-port calibration. One port is excited at a time with the other ports terminated with individual 50 Ω loads. Six measurements are carried out to collect all s-parameter data from 10 kHz to 1 GHz.

To extract s-parameters from the model, an iterative process has been designed to sweep through a frequency range from 10 kHz to 1 GHz. At each frequency point, a full netlist including R, L, C, and M is extracted from the model and evaluated in Synopsys HSPICE for s-parameter extraction. The simulated results are then converted to touchstone format where the data can be easily accessed and plot using the MATLAB-RF toolbox. The same test structure is modeled in ANSYS HFSS, where four lumped-ports are connected to the structure and s-parameter simulation is performed.

Fig. 13 shows the comparison among model, HFSS and s-parameter measurements. Overall, the results show good agreement between three sets of data. The results between model and HFSS match very well with less than 3 dB absolute error for all frequencies. Measurement results show some noise in the frequency range less than 100 kHz. This is because the intermediate frequency of 3 kHz in the measurement setup only has 75 dB dynamic range for the frequency region from 100 to 300 kHz. Also, the contact resistance between solder and SMA connector might also introduce some noise. However, the results fit very well in the high-frequency region (>100 kHz). This shows that the capabilities of the model allow it to accurately predict coupling between traces.

Table I. Evaluation Time Comparison

Method	Evaluation Time	#Mesh
Model	**30 ms**	120
HFSS	180 s	1371

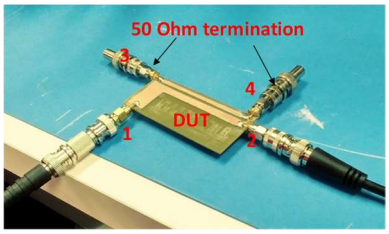

Fig. 11. Fabricated four-port PCB design.

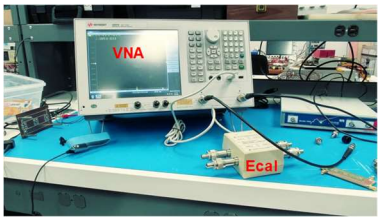

Fig. 12. Setup for S-parameter measurement.

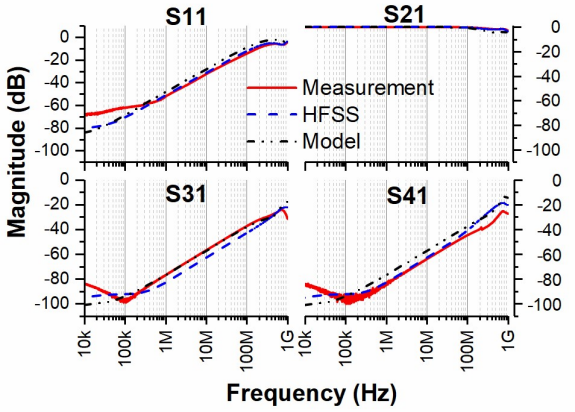

Fig. 13. S-parameters measurement versus simulation results.

C. *Loop RL Extraction*

Another capability of the model is handling components through hierarchical edges. As seen in Fig. 14, hierarchical edges and bond wire edges are connected to the uniform mesh of a half-bridge module. Parasitic extraction of this module has been performed in [1] using an HP16047A impedance analyzer for a frequency range from 10 kHz to 1 MHz. The results show good agreement among the previous method in [1], the new model, and measurements. Table II shows the speed and features comparison among the different models. While the new model is slower than the previous method in PowerSynth, it computes mutual inductance and current density, with capability to handle generic device connections. In addition, the matrix solution time for the new model is fast as seen in Table II, due to the small number of mesh elements. However, it includes the mutual inductance calculation step, which is very computationally expensive. This mutual calculation step can be sped up in the future through multi-threaded programming.

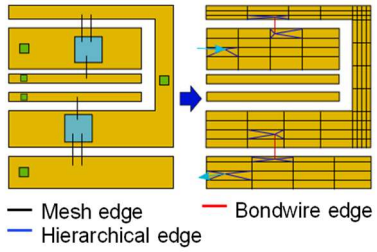

Fig. 14. Test vehicle half bridge module from [1].

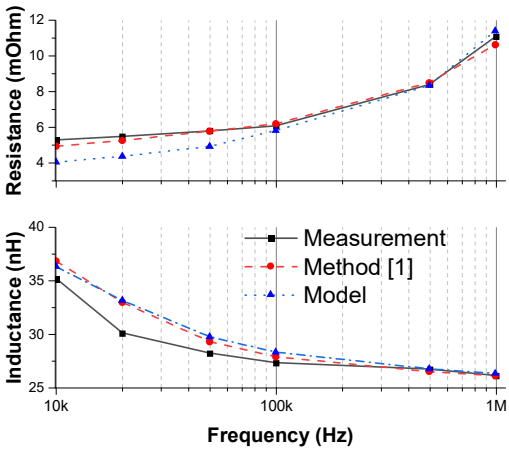

Fig. 15. Resistance and inductance loop validation.

Table II. Speed and Feature Comparison

	FastHenry	Previous Model [1]	Model without M	Model with M
Extraction Time	~300 s	~50 ms	~180 ms	~1.5 s
Speed-up Factor	1	x6000	x1071	x200
Mutual Inductance	Yes	No	No	Yes
I/V Distribution	No	No	Yes	Yes

IV. Conclusion and Future Work

Overall, the presented methodology has shown its capability for fast and accurate extraction for power circuit layout applications. Future work on this model will enable the parasitic extraction of more complicated 3D structures. More validation of 3D structures will be performed to further investigate the capabilities of this method. In order to increase the model speed, a multi-threaded programming strategy will be used to speed up the mutual inductance calculation. Also, it has been found that not all mutual inductance pairs have an impact on the accuracy of the loop evaluation. Hence, along with the new programming strategy, a classification method will be applied to calculate mutual inductance pairs with significant impact only. This would further speed up the calculation time for complex layouts while ensuring accurate extraction results.

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