Toward Partial Discharge Reduction by Corner Correction in Power Module Layouts

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***Abstract*—As spacing between traces in power modules is reduced to meet increasing power density requirements, partial discharge (PD) starts becoming a threat that can cause insulation breakdown, if not checked. For high voltage applications, PD awareness is particularly important, and this paper describes how various trace shapes play a critical role in the electrical reliability of modules with regard to electrical breakdown. Sharp corners of traces must be avoided, as is generally done for mechanical stability reasons, by filleting the corners. High voltage experiments were performed to confirm the detrimental electrical effects of sharp corners. The degree of improvement by completely avoiding sharp corners was quantified for various trace gaps. Simulations were performed to predict the improvement in terms of E-field concentration with respect to the radius of fillets. Preliminary fillets were implemented in a stand-alone in-house tool called PowerSynth, which is used for electrical and thermal optimization.**

Keywords—partial discharge, electric field, high voltage, electrical breakdown, hi-pot, power module, layout, PowerSynth, Maxwell, charge density.

I. INTRODUCTION

Partial discharge (PD) is defined by the International Electrotechnical Commission as a "localized electrical discharge that only partially bridges the insulation between conductors and which may or may not occur adjacent to a conductor." PD occurs due to "stress concentrations in the insulation" [1]. These normally occur at small voids or cavities inside a material where a high electrical field is applied across the gap between two conductors. Example voids could be gas bubbles in the potting compounds of power modules or gas bubbles in the liquid dielectric of a transformer [2]. These voids have electrical permittivity much lower than that of the surrounding material, causing electric field lines to concentrate in these regions. The voids in the material can grow over time as PD is repeated each cycle, and other voids can line up in the material along a path where there is a high electric field, eroding the material over time. Partial discharge can also occur in the form of corona, i.e. at the surface of a material interfacing air. PD can cause localized heating. High temperature at PD sites also cause further degradation of the material. This can eventually lead to reduced lifetime of an insulator and dielectric breakdown. PD effects are exacerbated at higher temperature, altitude, frequency, dryness of air and voltage levels.

This paper quantifies the improvement that can be expected toward partial discharge, when the shapes of adjacent traces on the same layer of a power module are modified. Most PD measurements for power modules previously researched involve detecting PD in the material stack, i.e. between the die and the layers of the substrate, instead of between adjacent traces of any individual layer [3-6]. The edges of the metallization layer are typical sites for partial discharge [6]. As a result, a lot of work has gone into improving the quality of the insulating material [3, 7-8]. Nevertheless, the occurrence of voids and interfacial defects are inevitable due to the current state of the manufacturing process [9]. Partial discharge can be mitigated by either improving the insulating material, reducing the potential difference across the electrodes, changing the spacing between traces, or changing the geometry of the traces. The operating voltage is usually based on the application and is fixed. Instead, a package that can withstand the specified

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operating voltage, is selected. Trace gap, or spacing, is typically a design rule constraint that is often a function of the power density requirement. With denser modules, there is higher propensity of partial discharge occurring. This means the geometry of the traces will be significant, which has not been researched as much in the context of partial discharge.

Trace geometry alteration is part of the layout design of a power module and can play the deciding role in determining the power density of a module as well as its reliability. PowerSynth is a tool that optimizes a given layout for electrical parasitics and thermal effects to provide various power-dense and thermally optimized layout options [10]. But it currently accommodates only 90° trace corner geometry. Incorporating variable trace corner geometries (chamfers, fillets, and curved traces) based on PD-related assessment as a post layout-optimization strategy, would make the resulting power modules more reliable.

PD detection has been a topic of research for a while. There are several standards, such as the IEC 1287, IEC 60270, BS EN 3475-307:2015, IEC TS 61934, etc. Many of these describe specific ways to measure PD inception voltage (PDIV), PD extinction voltage (PDEV), RPDIV (Repeatable PDIV), and Repeatable PDEV, but they are mostly about measuring PD between various layers of the module [7].

Some standards have been improved upon. Compared to IEC Standard Nos. 1287 and 60270, a new method tested by Lebey, *et al.* avoids several false positive results. For instance, while one of the standards recognized a module as safe to be operated at 5 kV, Lebey, *et al.* found that it is not safe to operate the equipment over 3.3 kV [11]. While Lebey, *et al,* did consider three cases where inter-trace surface discharge was considered, no studies were found that assessed the geometry of adjacent traces as a variable in the assessment of partial discharge.

Therefore, the contribution of this work to the area of PD awareness for power modules is a combination of the following:

1. The consideration of adjacent traces in a single layer, and how the corners of these adjacent traces affect PD-related quantities, as opposed to considering the layers between the routing layer and the baseplate and working on improving the insulation material.
2. The quantification of the expected improvement (in terms of the breakdown voltage in air, or the electric field) when the shape of a trace corner is changed, and the degree to which corner correction helps.
3. Integration of this corner correction method into a tool that already optimizes power module layouts for electrical and thermal requirements.

While the need for filleting is intuitive, the primary objective of this work is to quantify the improvement in electrical reliability with respect to the amount of filleting. Toward that objective, simulations were conducted, and preliminary experiments were done to collect evidence of the amount of improvement that can be expected. Here, improvement in electrical reliability was quantified in terms of the electric field strength for simulations and the air breakdown voltage of a trace for physical experiments. The simulations compared a variety of angles, spacings, and fillet radii, while the physical experiments compared the extreme cases of no fillets (i.e. sharp corners) to maximum fillet size (i.e. no sharp corners).

Partial discharge can be mitigated by either improving the insulating material, reducing the potential difference across the electrodes, changing the spacing between traces, or changing the geometry of the traces. The scope of this work encompasses key geometries of trace corners. The default geometry is a square that has four sharp corners. When these sharp corners are filleted, with increasing fillet radii, the result is a circular trace, where the filleting is maximum. Therefore, a circle and square were used to assess the maximum amount of improvement that can be expected from filleting, for a given trace gap.

Though electrical breakdown is not the same as partial discharge, partial discharge eventually leads to electrical breakdown, and thus, the breakdown voltage of one type of corner relative to another can be a way to model toward partial discharge. This paper has been organized into four sections: Simulations, Experiments, Design, and Discussion.

II. Simulations

It has been shown that charges accumulate at sharp corners [12]. This accumulation of charges over a small area creates an electric field concentration. Power modules often have trace corners that are 90° and should be avoided to reduce the E-field stress on the insulation materials.

The E-field in the layout of an example switching position of a power module was simulated in ANSYS Maxwell 3D. A voltage of 2 kV was applied between the DC+ and output leads (OFF mode). The gate was at the same potential as the output lead. The maximum electric field in this case was 6 kV/mm at the trace corner, and 1 kV/mm at other parts of the trace. A commercial dielectric gel was assigned as the insulating material [13]. Charge density simulations showed a maximum charge density at the same 90º corner to be 170 pC/mm^2 compared to 10 pC/mm^2 at the straight regions. Filleting lowers charge density at these corners, which then reduces the electric field intensity across the insulator. Fig. 1 shows the charge density map (pC/mm^2) and the E-field (kV/mm) for non-filleted and filleted traces. Fig. 1(a-c) shows there is high charge concentration at the sharp corners of the high voltage trace, and that filleting reduces the charge concentration from 170 pC/mm^2 to 140 pC/mm^2. Fig. 1(d) to 1(f) show the impact in terms of electric field strength. In this case, filleting reduced the maximum field in the gap to almost half of the original value (from 6 kV/mm to 3.1 kV/mm). Chamfers, as shown in Fig. 1 (b and e), offer an intermediate solution.

While the dielectric used as the potting material has a breakdown strength of 21 kV/mm in ideal conditions, over time it will be reduced. Maintaining a good safety margin can lead to increased reliability over the lifetime of the module. Filleting offers an additional safety margin over keeping 90º corners.

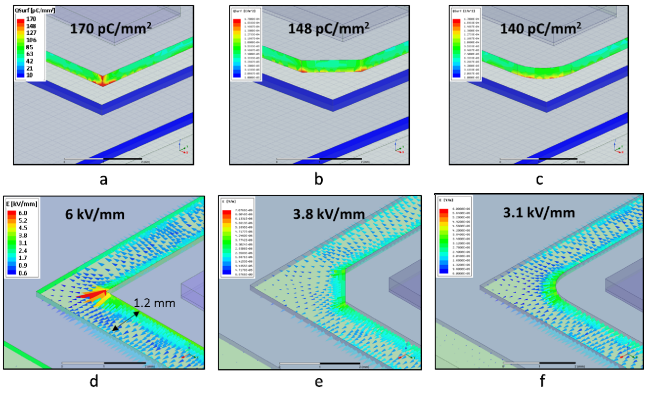

Fig. 1: Charge density map on drain trace with respect to source trace (a-c), and electric field distribution between drain, source, and gate traces in a power module layout

The trend in the simulations shown above is in agreement with the theoretical equations in [12], provided here as Equations 1 and 2. These represent the surface charge density (σ) and electric field (*E*) at a corner as a function of the distance from the corner (ρ) at which the E-field is observed, and the opening angle of the corner (β). α_1 is a constant.

$$\sigma(\rho) = \frac{E_\varphi(\rho, 0)}{4\pi} \cong -\frac{\alpha_1}{4\beta}\,\rho^{\left(\frac{\pi}{\beta}-1\right)} \quad (1)$$

$$E = \frac{-\alpha\pi}{\beta}\,\rho^{\left(\frac{\pi}{\beta}-1\right)} \quad (2)$$

Equation 2 was used to predict the electric field at sharp corners of simple 2D trace shapes as shown in Fig. 2. Angle β was varied, and E field was calculated at a point 0.01 mm (ρ) from the sharp corner. α_1 was calculated based on a parallel plate capacitor approximation where β = π, and E = V/d where V is the potential difference between the two plates and d is the gap between the plates. This was validated through simulation.

With α_1 established, the calculated E was tabulated as shown in Table I. Simulations were conducted to observe E at 0.01mm from the high voltage trace with a specified trace gap and corner angle. These values were compared to the theoretical model and are also shown in Table I. There was about a 15% difference and this is likely due to the assumptions made in determining the constant α_1.

The theoretical model as given does not work for rounded corners or fillets since the angle β is difficult to approximate. Hence a filleting radius component must be introduced. Simulations were performed to assess how E field varies with filleting radius. The amount of spacing between the two traces, and the fillet radius of the corner of the higher voltage trace were varied. Fig. 3 shows some of the trace shapes and Fig. 4 shows their simulated E-field values. The electric field was observed at a point very close to the corner (0.01mm away from the corner) in accordance to the assumption made in [12].

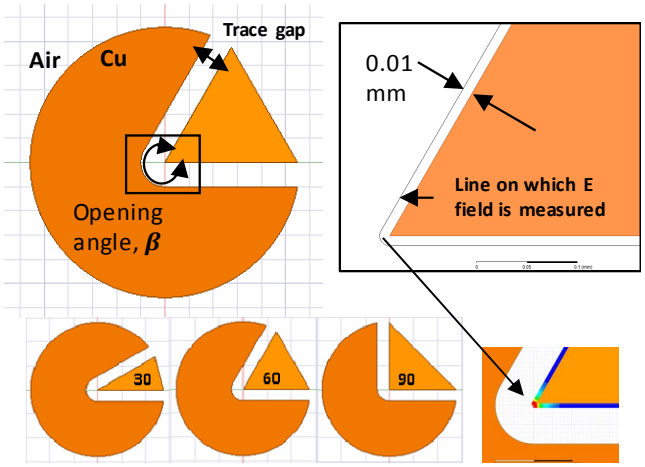

Fig. 2: Model to assess E-field at various sharp corners

TABLE I. CALCULATED AND SIMULATED E-FIELD VALUES

Acute angle (360°-β)	E (kV/mm) from Eq. 1	E (kV/mm) from sim	% Difference
10	4.82	5.77	16.6
20	4.62	5.53	16.4
30	4.42	5.27	16.0
40	4.22	5.00	15.6
50	4.01	4.73	15.3
60	3.79	4.45	14.9
70	3.56	4.15	14.3
80	3.33	3.86	13.8
90	3.09	3.57	13.2

The E-field comparison shows that while filleting provides significant benefits in reducing the electric field concentration at a corner, the greatest benefit is when replacing a sharp corner with a small fillet, in this case, a 1 mm fillet which gives about 50% reduction in E. The improvement from 1 mm to 2 mm is only an average of 10%, and from 2 mm to 3 mm is only 5%.

This trend of diminishing returns in E-field reduction as the size of a fillet is increased is important to be aware of, especially when filleting traces in high-density layouts. Fig. 5 shows examples of the increase in the overall footprint of a layout as adjacent traces are filleted or components are shifted to accommodate for the fillets.

To address the full impact that corner correction has on a layout, it is important to first quantify the expected positive impact of maximum filleting. Physical experiments were devised to achieve this objective.

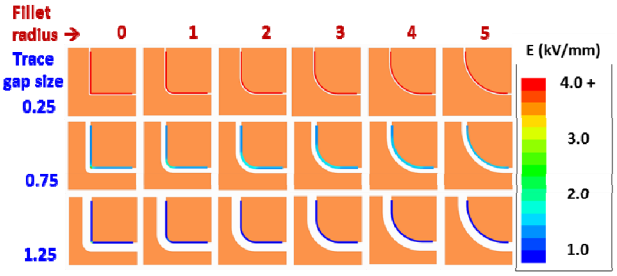

Fig. 3: Example coupon shapes, spacing and fillet sizes (in mm)

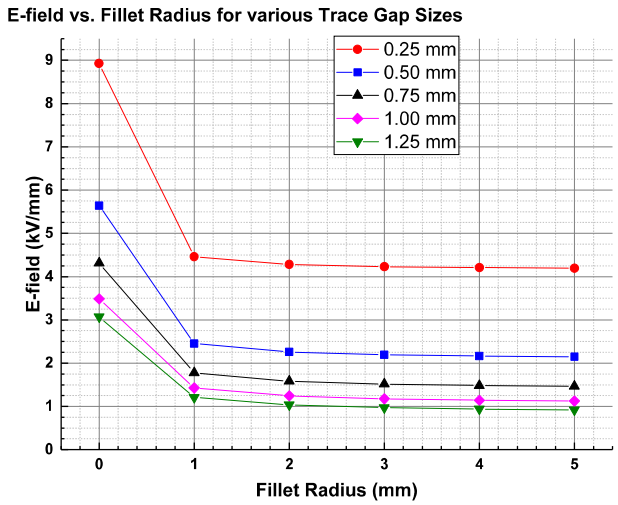

Fig. 4: E-field comparison for various trace gap sizes and fillet sizes

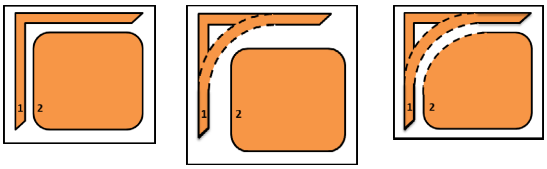

Fig. 5: Filleting impact on the size of a layout

III. High Voltage Experiments

To get a baseline of the expected improvement in the breakdown voltage when converting a sharp corner to a fillet, test coupons were designed such that a square would represent the worst-case scenario, while a circle would be the extent to which the square trace can be filleted, i.e. the best-case scenario. Similar sets were created for trace gaps ranging from 0.25 mm to 1.25 mm. These were milled out using a CNC machine with a minimum tool tip size of 127 µm (5.0 mil). A single-sided copper-clad FR4 substrate was used to make the test structures. An example set of test coupons after milling is shown in Fig. 6.

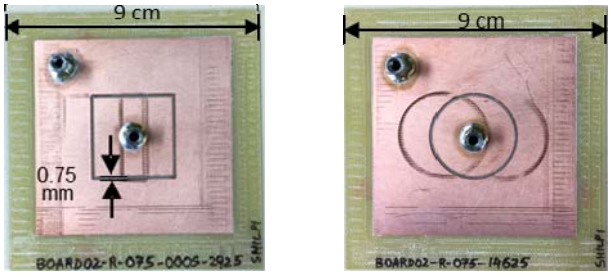

Fig. 6: A square trace and a circular trace after milling

The size of the test coupons was intentionally kept large to ensure the high potential terminals were far apart, significantly far compared to the trace-gap. Terminals were then soldered on using solder paste. A hi-pot tester (Valhalla Scientific's 5880A Dielectric Analyzer) capable of supplying up to 5 kVAC was used to supply high voltage AC (60 Hz) to the test structures. The test setup is shown in Fig. 7. A 15 kVDC cable was used to connect the hi-pot terminals and the test coupon terminals.

The ambient temperature in the room at the time of the tests was 24°C, and the relative humidity varied between 47% and 50%. The hi-pot was operated under the 'Automatic AC Dielectric Strength Function' setting with the following operating criteria:

- Voltage limit: variable depending on the test (typically between 1000 V and 2500 V)
- Voltage ramp rate: 10 V/s
- Current limit: 10 µA
- Minimum current 0.0 mA
- Dwell time: 10 seconds
- Operating frequency: 60 Hz
- Current sense: TOTAL (as opposed to real or apparent)

The voltage being supplied, the leakage current through the gap, and the time remaining of the test could be read off the hi-pot's display. Leakage current was plotted against the supplied voltage for each set of test coupons (both square and circle) and is shown in Fig. 8 – 12. There were five sets differentiated by trace spacing: 1.25 mm, 1.00 mm, 0.75 mm, 0.50 mm, and 0.25 mm.

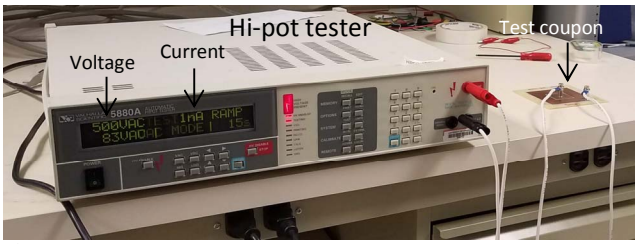

Fig. 7: Test setup

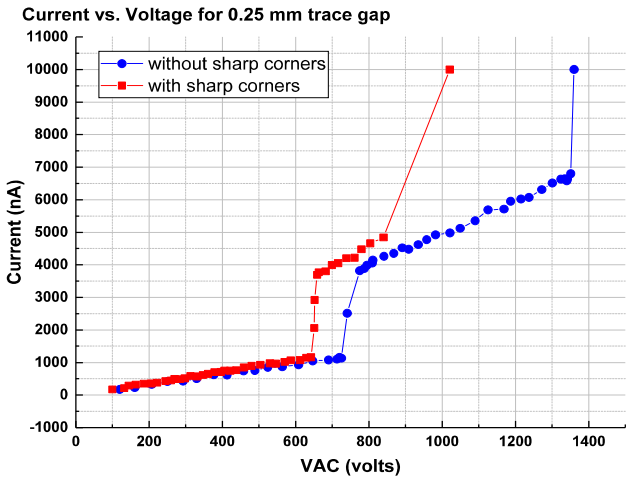

Fig. 8: 0.25 mm spacing

Note that the sudden rise of current from 1µA to 4µA occurred during all tests, and the authors attribute this to a likely change in the current sensing circuit within the hi-pot due to a change in the range of current being measured. The sudden rise was also accompanied by an audible click within the instrument.

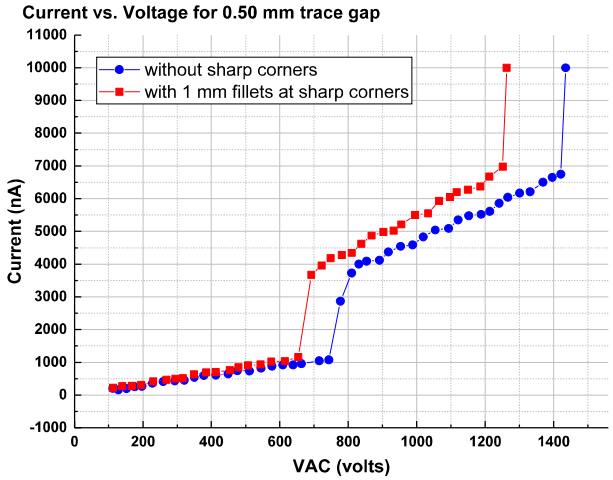

Fig. 9: 0.50 mm spacing

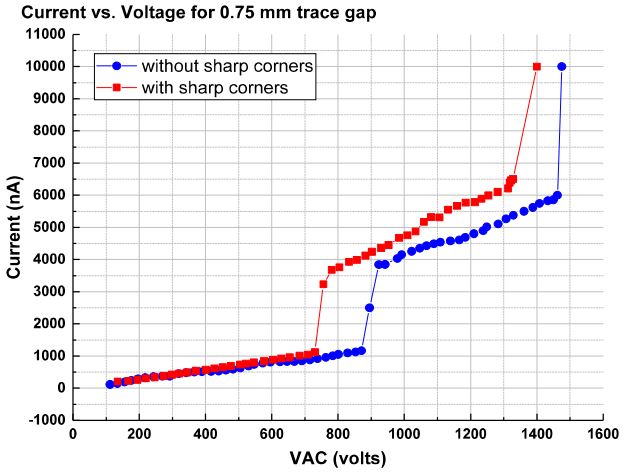

Fig. 10: 0.75 mm spacing

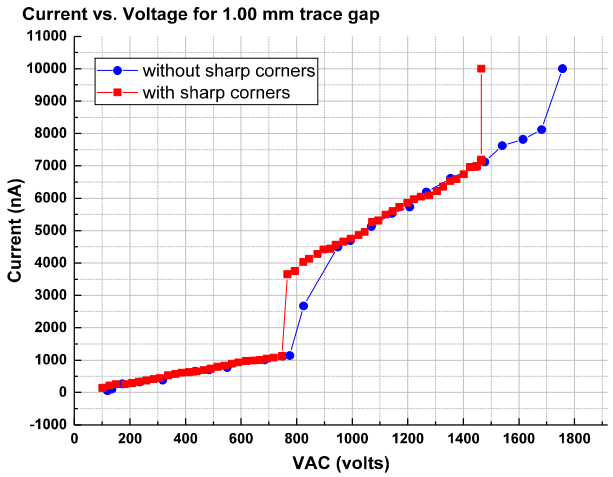

Fig. 11: 1.00 mm spacing

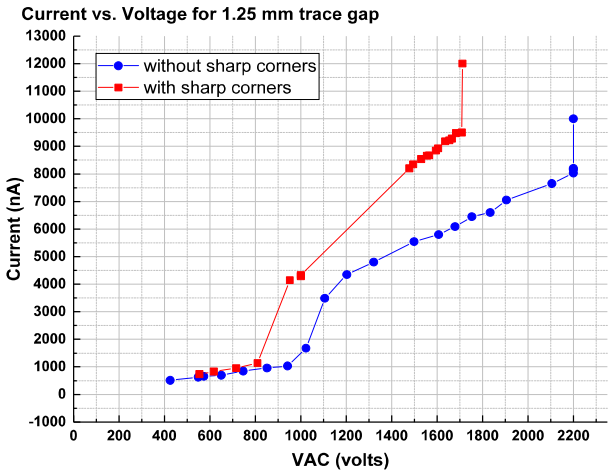

Fig. 12: 1.25 mm spacing

The more interesting data points are toward the higher end of the voltage range, where the sample being tested approaches breakdown in air. Since the current limit was set to 10 µA, the hi-pot test was terminated either when 10 µA was reached or when an arc was detected (default safety setting to prevent catastrophic damage to the test object). It can be observed that the circular trace performed better than the square trace for each set of test cases and performed significantly better than the square for most of the cases. The differences are quantified in Table II.

Going from a sharp-cornered trace to a maximum filleted trace shows a 14 to 33% increase in the breakdown voltage. For an application, if PD is the critical condition for avoiding higher voltages, filleting might allow operation at 14% higher voltage levels, adding to the safety margin, thus increasing reliability in terms of arc prevention. Note that there is minor difference between the breakdown voltages of the square and circular test coupons for the 0.75 mm spacing case. This is because the sharp cornered trace on the original test coupon was damaged in the machining process and had to be replaced by the 1.0 mm filleted coupon. Thus, the breakdown strength was affected. This exception also agrees with the simulations that show the diminishing returns of increasing fillet sizes.

TABLE II. SUMMARY OF BREAKDOWN VOLTAGE AND LEAKAGE CURRENT RESULTS

Voltage levels (V)		Test coupon spacing				
		0.25 mm	*0.50 mm*	*0.75 mm**	*1.00 mm*	*1.25 mm*
Arc or 10 µA	S	**1021**	**1263**	**1400**	**1465**	**1712**
	C	**1360**	**1435**	**1475**	**1757**	**2200**
	%	+33	+14	+5	+20	+29
5 µA	S	850	910	1050	1045	1080
	C	1030	1040	1250	1070	1380
	%	+21	+14	+19	+2	+27

S: Square trace; C: Circular trace; %: Percent increase in voltage
* 0.75 mm: The square trace had a 1.0 mm fillet as the sharp cornered coupon was damaged

For a different 0.75 mm set, fillet sizes were increased from 0 mm to 2 mm to 3 mm. 1293 V was the breakdown voltage of the sharp trace, 1495 V for the trace with 2 mm fillets, and 1539 V for the 3.0 mm fillet. The trend was as expected. Sparks for sharp cornered traces occurred first at the sharp corner. An example is shown in Fig. 13. A channel was formed between the traces during breakdown.

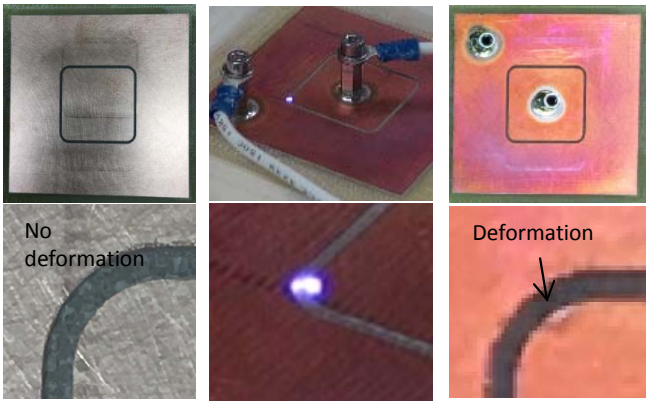

Fig. 13: Localized pitting of material at corner after an arc is discharged

IV. Design

Sharp corners were detected and fillets were applied to all the layouts generated in an in-house stand-alone CAD tool called PowerSynth [5]. Fig. 14 shows the example of a of a half bridge module layout. PowerSynth is used for electro-thermal optimization and is now being expanded to include partial discharge awareness after preliminary layout optimization.

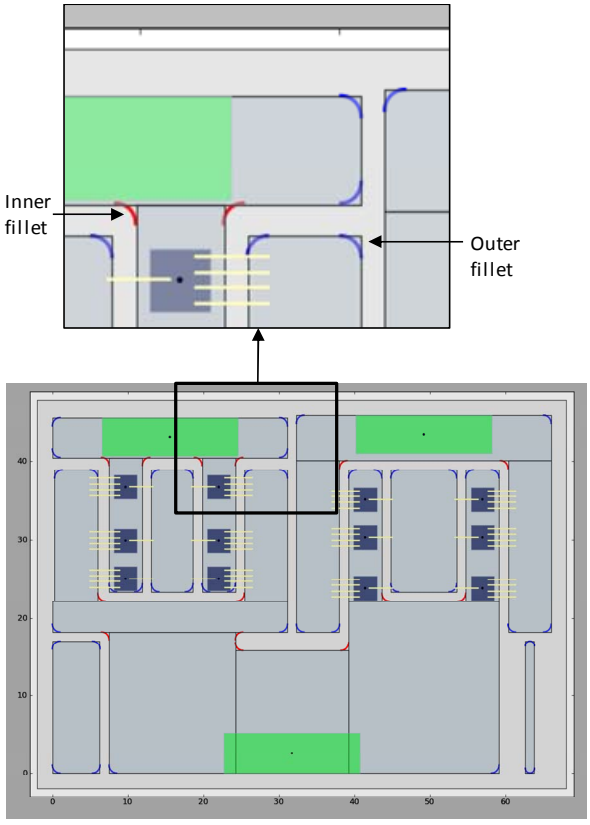

Fig. 14: Initial fillets implemented in CAD tool

Red curves in Fig. 12 represent inner corners that are mostly affected by current crowding and blue curves are affected either by electric field density or need filleting to avoid mechanical stress. Current filleting routine ensures there are no overlaps, and that fillets are sized within the limitations of the traces that are being filleted.

V. Discussion and Future Work

Partial discharge is a phenomenon where a spark, or an electrical breakdown occurs within only a part of an insulating material, but that does not bridge the whole gap between the electrodes. These localized discharges typically occur within voids inside an insulating material where the electric field lines concentrate due to a much lower electrical permittivity compared to the surrounding material. Partial discharge, or PD, worsens over time and even more so at higher frequencies, as the discharges repeat each cycle and deteriorate the material that surrounds the void.

One of the ways of mitigating PD is to use high quality insulating materials. Another, more economical way, is to alter the geometry of the electrodes where PD occurrence is predicted. This research was conducted to study the effect of trace corner geometries for two main cases: one for a sharp cornered trace with no intentional fillet, and another for a circular trace with no intentional sharp corner. The objective was to quantify the range of improvement that can be expected when filleting a sharp corner to a certain extent. The results are in terms of the voltage at which an arc would occur in air for each test case. While this is a test for electrical breakdown in air, it is indicative of the occurrence of PD at proportionately lower voltages. Key results from simulations and physical experiments are summarized as follows and leads for further investigation are also provided.

From simulations, a large benefit of 50% decrease in electric field was observed when converting a sharp corner to a 1 mm fillet. Successively lower benefits were observed switching from 1 to 2 mm fillets, 2 to 3 mm, and so on. The significance of this reduction is that while filleting is highly encouraged, too much filleting may not be required. This awareness becomes critical when correcting corners in high density layouts where one filleting operation may require moving components and adjacent traces, or co-filleting adjacent traces, which may result in a larger overall footprint of the entire module.

From experiments, an average of 20% increase in the breakdown voltage was observed when converting a square shaped trace into a circular-shaped trace with its diameter the same as the side length of the square. The smallest trace gap case showed the maximum impact (33%) in terms of increase in breakdown voltage, going from 1021 V for the square trace to 1360 V for the circular trace.

For the case of incremental fillet sizes, there is an upward trend going from 1293 V for a sharp-cornered trace, to 1495 V for a 2.0 mm fillet and 1539 V for a 3.0 mm fillet. However, this test was not repeated. More test coupons need to be fabricated to assess if the upward trend continues at the same rate, or approaches diminishing returns as fillet size is increased beyond a certain point.

For future investigations several improvements are planned:

A. Sample Preparation

The milling machine used to create the test coupons for this experiment were limited by

- the size and shape of the machine tool tip which created V-shaped groves instead of right angled groves.
- the highly abrasive machining process that results in asperities in the conductor edges that can be concentration sites for charges,
- the lack of cleanliness of the machining process that can leave behind particles that inadvertently bridge the gap between traces,
- the oxidation of the copper surface during solder reflow process that may change the material's properties,
- improper soldering that can cause partial discharge at the interconnect interfaces.

Higher fidelity fabrication techniques such as photolithography and wet etching processes will be used to eliminate the limitations of the milling machine. A direct bonded copper material will be used as the substrate instead of Cu-clad FR4 boards. More care will be taken to ensure cleanliness of samples so that dust does not bridge the gap between the traces.

Other effects that will be considered include temperature, pressure, and ground plane effects. Charge distribution varies with temperature and this will affect PD. Low pressure exacerbates PD. And conducting planes on either side of the traces in the z-dimension can focus the electric field further, resulting in earlier inception of partial discharge.

B. Partial Discharge Detection

This study has been about E-fields and electrical breakdown thus far. True partial discharge happens well in advance of breakdown and is difficult to detect. A hi-pot tester provides AC or DC voltage with a certain slew rate. The instrument stops if it detects an arc, and reads out the voltage at which the arc occurred. The current reading and voltage reading of the instrument are not necessarily synchronous. For this test setup, data collection interface was limited resulting in a lack of sensitivity in measuring current surges. As mentioned earlier, the hi-pot instrument had an audible click each time the current passed a certain threshold and it is suspected that the internal current measurement circuit goes through a switching process to accommodate a change of range in the current being measured. This shows up as the sudden increase in slope in the I-V curves shows in Fig. 8-12 around the 1-5 μA threshold. This instrument does not detect partial discharge.

Partial discharge results in an energy exchange and can take the form of sound (noise), light (electromagnetic waves), dielectric losses, chemical reactions, current impulses, and gas pressure [14]. For the next iteration of this study, electrical methods such as current impulses, electromagnetic interference and dielectric losses, will be explored. The non-destructive methods will allow repeatability of tests. Remote sensing methods using antennae will also be beneficial as they are safer methods. A transparent gel will be used as the dielectric.

True PD quantification is challenging since a very small magnetic field needs to be detected in the presence of a strong electric field. Separating the noise generated by the presence of PD from the ambient noise is difficult. SPS Electronic [15] and OMICRON [16] are two examples of manufacturers that make PD detection equipment. Both instruments have the sensitivity to detect pico coulombs of charge that are transferred during a PD process. Capacitance measurements will be used in conjunction with the above to better predict leakage current levels at any given voltage, and model equivalent circuits for various trace geometries.

C. PD Model and Post Layout Optimization

For implementation in the CAD tool, it is important to identify which corners offer the highest impact due to filleting. These corners will then be appropriately filleted, and all affected adjacencies will be modified to accommodate for the essential fillets. This will require a model that predicts the likelihood and quantity of PD at any given corner and voltage level. To develop a model for the same, accurate measurements are required to empirically determine which corners need filleting and how much filleting is required. For very high voltage applications, filleting may not be sufficient. Layout design rules may need be relaxed to accommodate for the operating voltage specification. Current crowding is another issue that needs to be accounted for for filleting corners to avoid hot-spots. Post layout optimization, the final layouts will be exported to ANSYS Electronics Desktop and SolidWorks for fine-tuning layout details.

VI. Conclusion

In conclusion, partial discharge poses a serious threat to power modules operating at high voltages, especially when the spacing between conductors with high potential difference is limited. A PD-aware model for designing power module layouts is needed for electrical reliability. This work has uniquely considered the effect of corner correction of traces on the same layer, quantifying the degree to which filleting helps, and the expected improvement if the fillet radius of a corner is maximized. The filleting method has been incorporated in an EDA tool and is being improved. PD detection methods and models are being investigated further. PD-aware module design foresight can allow engineers to push the limits of high voltage operation by allowing a larger safe operating area. For future work, models will be created based on experimental results that will help determine critical corners to be filleted and the degree of filleting required.

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