Die-to-Package Coupling Extraction for Fan-Out Wafer-Level-Packaging

Yarui Peng[1], Dusan Petranovic[2], and Sung Kyu Lim[3]
[1]University of Arkansas [2]Mentor Graphics Corporation [3]Georgia Institute of Technology
yrpeng@uark.edu

***Abstract*—In fan-out wafer-level-packaging, the package interconnection layers are fabricated similar to the back-end-of-line interconnect stack where multiple dies are tightly integrated with dense package routing for higher performance and lower power. However, electrical and magnetic field interactions may introduce significant uncertainties in system power and performance. For the first time, we provide two CAD flows for extracting coupling capacitance between the die and package. In particular, we first analyse the E-field interactions using field solvers and demonstrate their impacts on die-to-package coupling. We then propose a holistic extraction flow which integrates all layers from the chip and package and extracts all coupling elements for the maximum accuracy. We also propose an in-context extraction flow for chip designers, which only includes necessary regions of the redistribution layer and still captures the E-field impact from the package. Our in-context extraction requires less computing resources, allows heterogeneous integration, and is still highly accurate compared with the holistic extraction. Final, we demonstrate our flow using detailed package and multi-chip layout.**

I. Introduction

Fan-out wafer-level-packaging (FOWLP) is a low-cost multi-die packaging solution and allows multiple heterogeneous dies to be integrated in the same package [1]. Compared with chip-to-wafer bonding, FOWLP can achieve a high throughput thus reduce the package cost. Compared with wafer-to-wafer bonding, individual dies in FOWLP are well-tested before known-good-dies are packaged [2]. In additional, multi-die 2.5D solutions using FOWLP overcome a series of electrical and thermal challenges in 3D ICs.

Further, the die-to-package distance is significantly reduced. A package road map from Amkor demonstrates a clear path to vertical stacking with a finer interconnection pitch and a closer die-to-package distance. Traditionally, CAD tools for silicon chips and packages are isolated in their respective design flows. Chip designers ignore the existence of the package and only route signals to predefined IO pads, while package designers connect these pads to the PCB unaware of chip routing. However, with advanced packaging techniques and tighter integration between chips and packages, D2P co-design is required to maximize performance and power savings.

In FOWLP, new parasitics are introduced in the interface layers between the die and the package. These additional coupling elements can compromise the signal integrity of the whole system, but are ignored in the traditional CAD flow, simply because chip and package design tools use different algorithms and layout databases, and have different targets. While chip tools are often designed to meet tight timing and power constraints, and must be able to handle billions of devices in a limited time, package tools often look across a wider frequency domain, but only handle thousands of wires with much larger dimensions. To the best of our knowledge, no existing tool extracts coupling capacitance with detailed layouts for FOWLP.

Traditional package extraction tools, such as HyperLynk and Sigrity, have limitations of only considering package traces. Field solver based extraction is used to perform frequency dependent extraction by first calculating the S-parameter of package trace and then perform curve fitting using capacitance and inductance. It also cannot generate a true distributed RLC network, and most of existing tools simply divide the extracted RLC components equally into a uniform parasitic network. Not to mention that it is extremely time-consuming to perform holistic extraction with field solving. Therefore, it is unattractive to chip designers since accurate parasitic extraction is required even in an early design stage.

On the other hand, existing parasitic extraction tools for chip designers cannot be used for extraction on D2P interface layers either. The first reason is assuming all wires have similar widths and their routing directions on the same layer are parallel is not true on package layers. The traditional way of performing extraction on wide traces is by dividing the traces into smaller mesh cells, but this method is computationally expensive. Also, package layers filled with traces routed in non-Manhattan styles and the hatch ground planes are also difficult to compute using chip extraction tools, which are generally designed for long and thin parallel wires. In this paper, we provide a first-of-its-kind comprehensive CAD methodology for D2P coupling capacitance extraction with detailed chip and package layouts.

II. Field Solver Analysis

A. Technology Setting and Benchmark

We use a 45nm technology with seven metal layers for our designs. M6 has a wire width and spacing of 0.4µm, respectively, while M7 has 2µm. The wire dimension and metal stack technology settings are shown in Figure 1(a). We include three RDLs from the package, all with the same 10µm width and spacing. Package layers have a thickness and separation distance of 5µm, and the D2P distance is 5µm as well. As the thinnest chip wires on M1 are only 65nm in width while package wires are 10µm wide, there is a huge dimension gap that makes it extremely challenging to handle both wires simultaneously. However, since the majority of chip wires for intra-die communication are located in lower metal layers, they are protected from package E-field impacts because of shielding from the top metal layers.

We create three FOWLP designs with detailed layouts for testing and analysis. An FFT256 design with 1.15M gates and 78 signal pins is used as the chip die. The die area is 1.5×1.5mm. We also design the FOWLP package to be 4×4mm in size, with a 12×12 BGA array. We mount the chip in the center of the package to form an FFTx1 design. Two 2.5D designs are created by mounting multiple FFT256 chips on the same package. The FFTx2 has dual FFT chips, located left and right on the center line, and the FFTx4 has quad FFT chips, forming a 2-by-2 array. The size of all packages is the same as FFTx1, and each chip's ports are connected through the package RDLs. Figure 1(b) shows our FFTx2 design and Figure 1(c) shows the full layout of FFTx4 design. With detailed layouts and routing from both chip and package, our tools are designed to handle both high complexity from tiny but many chip wires and large dimensions from package wires.

This work is supported by Mentor Graphics Corporation.

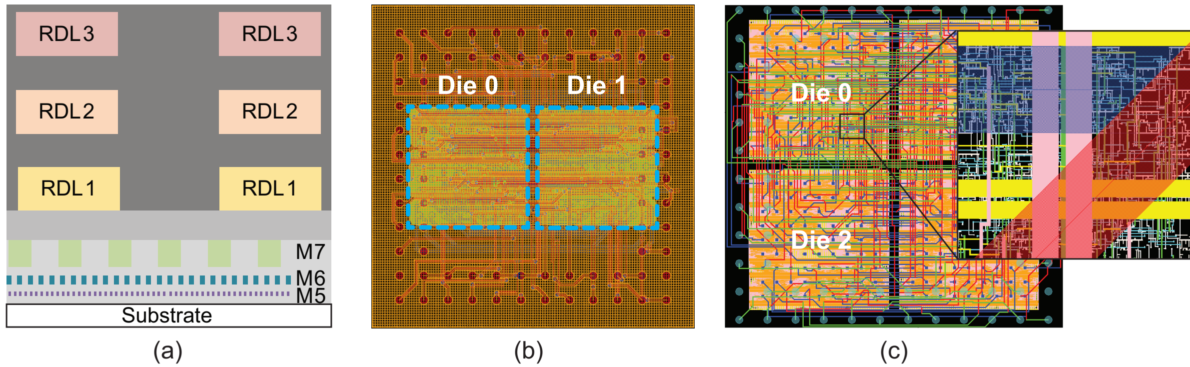

Fig. 1. (a) Cross-section view of our FOWLP metal stack. (b) our two-die FFTx2 design. (c) our four-die FFTx4 design with hatched ground plane removed.

TABLE I
D2P COUPLING CAPACITANCE WITH VARIOUS D2P DISTANCE.

Top Layer	CCap (fF)	D2P distance (μm)			
		2	5	8	10
M7	M7-to-RDL1	15.06	7.155	4.746	3.880
	M6-to-RDL1	0.005	0.002	0.002	0.002
M6	M6-to-RDL1	4.330	3.319	2.691	2.388

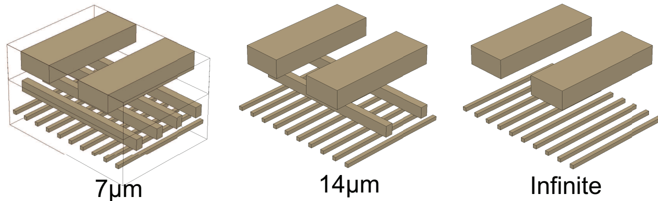

Fig. 2. Raphael structure with various M7 pitch.

B. D2P E-field Interface Analysis

To understand the E-field coupling within interface layers, we build several structures and use Raphael to obtain parasitic capacitance. We change the D2P distance while keeping the minimum width and spacing for all wires. As shown in Table I, all the D2P coupling is very sensitive to the D2P distance. Since current D2P distance is still larger than the wire pitch of the chip layer, the D2P interface coupling is weaker than both intra-die and intra-package coupling. However, we predict this capacitive coupling will increase with the advanced packaging techniques, with a 2μm D2P distance using a BEOL technology for RDL fabrication. Therefore, it is critical to have the CAD extraction tools ready by then.

Further, we study the impact of E-field shielding of the top metal layer. Several Raphael simulation structures shown in Figure 2 with various M7 metal pitch is created. As shown in Table II, when M7 is the top metal layer of the die, M6-to-RDL coupling is negligibly small, because of heavy E-field shielding from M7. However, if M7 is removed, M6-to-R1 becomes much larger. We also study the E-field shielding impact from the package side. Raphael structures with various number of package layers are extract and results are shown in Table III. Though multiple RDL layers affect the coupling distribution, most of the coupling is only limited between the top layer of the chip and the bottom layer of the package. Less than 3% of the coupling capacitance is formed between non-neighbouring layers. Therefore, for capacitive coupling between die and package, considering the top metal of the chip and bottom layer of the package is accurate enough.

TABLE II
METAL LAYER E-FIELD SHIELDING IMPACT ON D2P COUPLING.

M7 spacing	7μm	14μm	Infinite
M6-M7	6.767	4.372	0.000
M6-R1	0.131	0.736	2.067
M6-R1	3.447	2.314	0.000

TABLE III
RDL E-FIELD SHIELDING IMPACT ON D2P COUPLING.

Total RDL#	1 RDL	2 RDL	3 RDL
M7-R1	7.155	6.960	6.953
M7-R2	-	0.201	0.195
M7-R3	-	-	0.005

III. CAPACITANCE EXTRACTION METHODOLOGY

A. Holistic Extraction

Traditionally, chip routing and package routing are extracted separately. Die extraction engines cannot handle large wires on package since the pattern matching algorithm is inaccurate with non-manhattan routed wires with a large difference in dimensions. Conversely, package extraction tools cannot handle small chip wires because full-wave-solver-based tools cannot efficiently solve structures with millions of wires. Our solution of holistic extraction [3] is to extend the functionality of Calibre xACT 3D, which is a fast field-solver-based die extraction engine to handle package wires with improved methodologies to reduce time complexity.

We first create a new metal stack configuration that includes all seven chip layers and three package layers. We then design a holistic die-package layout by merging the geometries from the die and package. Next we run Calibre xACT 3D to obtain the detailed SPEF netlist and analyze the output. We run our flow on FFTx1, comparing the interface extraction results returned with or without detailed layouts of the chip metal layers. As shown in Table IV, without detailed die layouts, interface coupling is overestimated by more than three times. This result demonstrates that simply assuming the die as the ground plane is not accurate for D2P extraction.

Holistic extraction is highly accurate since it contains all layers from both the die and the package. However, it is computationally expensive to include every structure and layout object in the memory. Since the package layout is much larger than the chip layout, this extraction requires in a significant increase in both runtime and memory increase to handle the complicated structures on the package layers. For example, extracting a full system containing two 10nm chip with 12 metal layers and a three-layer package with a dimension of 20mm-by-10mm requires more than 700GB of DRAM space, and more than three days to complete on a 32-node computing grid. Such

TABLE IV
D2P COUPLING CAP ERROR WITH GROUND PLANE APPROXIMATION.

	Ccap	Mtop	Via	RDL1	RDL2	RDL3
GND	Mtop	0	0	4.669	0.011	0.000
	RDL1	**4.669**	0	0.782	41.44	0.145
Real die	Mtop	60.92	2.793	1.019	0.075	0.055
	RDL1	**1.019**	0.006	0.710	42.65	0.056

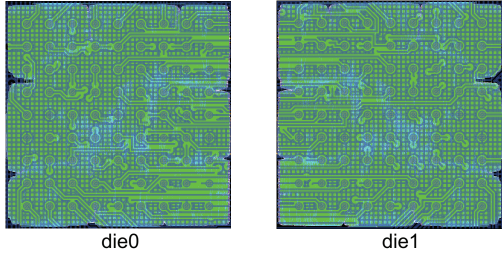

Fig. 3. Created In-context die with RDL1 layer.

a large resource requirement is unattractive to designers, especially during early design stages when a quick evaluation is needed.

B. In-Context Extraction

Instead of considering all layers from the package simultaneously, in-context extraction [3] can be used to accelerate the extraction process. Instead of including all chip layers and the full package layers, we extract each chip separately with a few interface layers from the neighboring component. The advantage of in-context extraction is reducing the extraction complexity and memory requirement, and it allows to reuse most of the existing 2D LVS rule decks with some minor extensions for interface layers. Therefore, in-context extraction greatly simplifies the process of validating a heterogeneous design flow and eliminates the need for maintaining a holistic PDK. Further, in-context extraction eliminates the need for sharing intellectual properties across different design houses. Only layouts and connections for interface layers are needed without revealing critical lower metal and device layers. As a result, it greatly enhance the application of heterogeneous designs where multiple chips comes different vendors and foundries.

Using in-context extraction, we only include one addition interface layer from both package and chip side during extraction and then emerge the parasitic database with post processing. Also, multiple dies are extracted separately, which significantly reduces memory requirement to less than 150GB with a more efficient runtime of less than 1.5 days. We compare the extraction accuracy of holistic extraction to in-context extraction using one interface layer from the package with results shown in Table VI. Since the package layer is mostly covered by the ground plane, the coupling depth is limited to one layer. Therefore, we conclude that for die-to-package capacitance extraction, in-context extraction is highly efficient and accurate compared with holistic extraction.

C. Full-System D2P Extraction Comparison

We perform a full-system D2P interface extraction on all three benchmark designs. Figure 4(a) shows the interface capacitance extraction results. With much denser RDL1 routing and larger overlapping areas with the chip, FFT256x4 has significantly larger D2P coupling capacitance. Because of E-field shielding, coupling between non-neighbouring interface layers is small. Figure 4(b) shows the extracted capacitance distribution of the FFTx2 design. Even though the absolute value of total coupling interface capacitance is small compared to intra-die coupling, these parasitics elements may affect some critical nets such as clock and high speed data bus, especially on long wires in parallel with package routing.

TABLE V
D2P COUPLING CAPACITANCE EXTRACTION RESULT.

Method	In-Context			Holistic		
Layer	M7	Via	R1	M7	Via	R1
GCap	29.87	3.529	5.726	29.78	3.454	28.124
CCap	M7	Via	R1	M7	Via	R1
M7	121.8	6.061	2.202	121.9	5.612	2.187
Via	6.061	0.000	0.000	5.612	0.000	0.000
R1	2.202	0.000	1.281	2.187	0.000	2.143

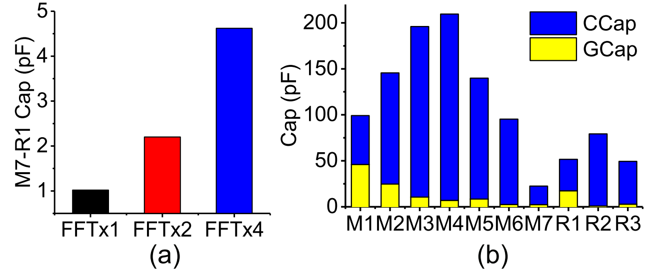

Fig. 4. (a) Interface coupling cap comparison, (b) ground cap (GCap) and coupling cap (CCap) distribution of FFTx2.

TABLE VI
D2P INTERFACE CAPACITANCE DISTRIBUTION OF FFTX2 DESIGN.

Layer	M6	M7	RDL1	RDL2	RDL3
GCap	2486.59	2316.71	17388.6	898.31	2833.76
CCap	M6	M7	RDL1	RDL2	RDL3
M6	18708	16623	354	410	2.71
M7	16623	257	2519	47.05	0.23
RDL1	354	2519	134	31207	11.57
RDL2	410	47.05	31207	461	46256
RDL3	2.71	0.23	11.57	46256	231

IV. CONCLUSION

In this paper, we performed a comprehensive study on D2P interface parasitic extraction using both holistic and in-context extraction flows. We observed a strong E-field interaction between chip and package layers with significant E-field shielding from interface layers. We proved that using ground plane approximation in capacitance extraction is not accurate enough for signal integrity analysis and using detailed layouts for both die and package is the key to accurate extraction. We further demonstrated that both holistic and in-context extraction can be used to capture D2P E-field interaction accurately in a multi-chip FOWLP package system. The D2P coupling capacitance is observable and needs to be considered with a closer D2P distance. Further, in-context extraction can be used to accelerate the adoption of heterogeneous integration in FOWLP with less requirements on computing resources and better IP protection.

REFERENCES

[1] C. C. Liu *et al.*, "High-performance integrated fan-out wafer level packaging (InFO-WLP): Technology and system integration," in *International Electron Devices Meeting*, Dec 2012, pp. 14.1.1–14.1.4.

[2] K. L. Wang *et al.*, "Test Cost Reduction Methodology for InFO Wafer-Level Chip-Scale Package," *IEEE Design Test*, vol. 34, no. 3, pp. 50–58, June 2017.

[3] Y. Peng *et al.*, "Full-chip Inter-die Parasitic Extraction in Face-to-Face-Bonded 3D ICs," in *Proc. IEEE Int. Conf. on Computer-Aided Design*, 2015, pp. 649–655.