Response Surface Modeling for Parasitic Extraction for Multi-Objective Optimization of Multi-Chip Power Modules (MCPMs)

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***Abstract*—In our tool, PowerSynth, fast calculation of electrical parasitics is of paramount concern when evaluating the layout of an MCPM during multi-objective optimization. To this end, this work extends the current capabilities of PowerSynth to quickly and more accurately extract lumped RLC parameters by utilizing a response surface model. An MCPM is represented as a series of layers forming a stack corresponding to their physical dimensions and material properties. FastHenry is employed to run frequency sweep simulations on this layer stack with both rectangular traces and 90-degree corners with varying sizes, spacing, and positioning. The results of these simulations are then used to build a response surface model accounting for frequency dependence and current crowding effects. This model is then used in the MCPM optimization engine to evaluate loop parasitics for a given layout. The results of this model are then compared with FastHenry simulations and measurements using an LCR meter and Time Domain Reflectometry (TDR) of a fabricated prototype.**

Keywords—Multichip Power Module; Response Surface Methodology; Parasitic Extraction

I. INTRODUCTION

Recent advances in wide bandgap semiconductor technologies have allowed more practical applications for high voltage, high temperature and fast switching Multichip Power Modules (MCPMs) [1]–[3]. Under fast switching conditions, minimizing interconnect parasitics–especially parasitic inductance–becomes one of the main challenges. Parasitic inductance results in higher voltage overshoot, increased switching losses, and electromagnetic interference and compatibility issues [4]–[6]. These problems can be mitigated with a better prediction of electrical parasitics in the layout synthesis stage. In some previous studies, state-of-the-art methodologies such as PEEC [7], and FEA [8] have been used to extract the electrical parasitics at the design stage. While these techniques provide high fidelity solutions, they are usually computationally expensive. This has reduced the freedom of the designer to synthesize multiple MCPM layouts in search of an optimized solution.

To overcome the extensive computation time in the previously mentioned, state-of-the-art parasitic extraction methods, PowerSynth [9] has been programmed to quickly estimate the electrical parasitics of different MCPM layout solutions, utilizing both lumped element circuit methodology along with analytical microstrip equations [10]. This has efficiently reduced the computation time from a few minutes using PEEC and FEA techniques, to a few milliseconds, allowing the user to compare thousands of layout solutions within a few minutes to an hour.

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In this paper, a simple half-bridge topology is generated by PowerSynth to study different parasitic extraction techniques in MCPMs. To begin with, an abstract layout representation, referred to here as a "Symbolic Layout," is built up in PowerSynth (Fig. 1). A detailed description of this concept has been articulated in [9] and, therefore, omitted in this discussion. An example layout (Fig. 2) is then generated by assigning width and length values for each trace, along with the coordinates of each device. The bond-wire lengths are then automatically defined by device positions and standard design rules entered into the software database. Once the layout in Fig. 2 is generated, a PowerSynth-FastHenry interface is used to export the FastHenry [11] simulation file. This can later be used to validate the parasitic extraction models against the PEEC solver in FastHenry. As previously mentioned, to leverage the computation speed in PowerSynth, microstrip formulae have been used to assess the parasitics of rectangular traces. While these models are computationally attractive, they have shown some limitations in prediction accuracy for MCPM applications. This will be shown in Section II below. Therefore, in this paper, a new method using a response surface model is shown to improve the fidelity of the parasitics extraction while maintaining the same computational effort.

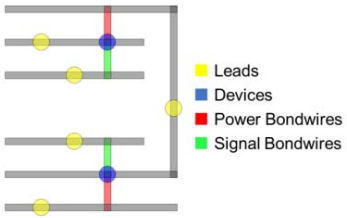

Fig. 1. Symbolic layout representation of the MCPM.

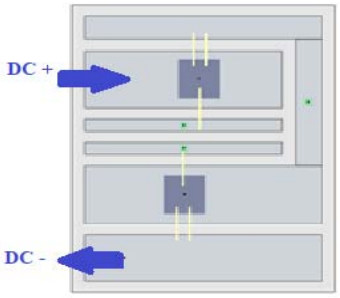

Fig. 2. Example MCPM layout from PowerSynth.

Parasitic extraction is performed on the above-mentioned layout using both the existing and new modeling techniques developed in this work. This module is then fabricated and measured to validate the extraction results. An HP 4284A LCR meter is used to measure the electrical parasitic values at different frequency points. The test frequency range has been selected to be 10 kHz - 1MHz with three frequency points per decade for the LCR meter. TDR measurement using a Tektronix 11801B is also performed to validate the high frequency results.

This paper is organized as follows: Section II describes some limitations with microstrip formulae for resistance and inductance extraction of MCPM layouts. Since our capacitance calculation has shown good results compared to measurements, response surface techniques introduced in Section III are used to improve the extraction fidelity for inductance and resistance only. Section IV presents the measurement results of the test vehicle compared to LCR extraction from PowerSynth. Then, Section V shows optimization results using this new model. Finally, Section VI discusses some possible improvements for the response surface technique.

II. Analatical Model Based on Microstrip

A. Microstrip based formulas for resistance and inductance

A microstrip is a simple electrical structure that consists of one single reference plane, an isolation layer, and a thin transmission line running atop. This model has been widely used in high-speed PCBs to form connection paths between electrical components [10]. Given their similar structures, as shown in Fig. 3, the microstrip formulation is a natural approach to MCPM parasitic extraction within PowerSynth [12].

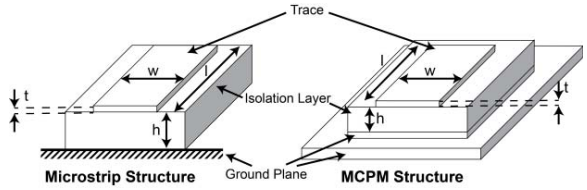

Fig. 3. Microstrip vs MCPM structure.

Equations (1), (2), and (3) below show the how resistance and inductance are modeled in PowerSynth using the microstrip model.

Effective resistance is defined as

$$R_{eff} = \sqrt{R_{ac}^2 + R_{dc}^2} \tag{1}$$

where

$$R_{ac} = \alpha \frac{l}{2\pi^2 w} \sqrt{\frac{2\pi f \mu_0}{\sigma}} \left(\pi + ln\frac{4\pi w}{t}\right)$$

and

$$R_{dc} = \frac{l}{\sigma w t}$$

A curve fitting parameter α, is then defined as

$$\alpha = 0.94 + 0.134\frac{w}{h} - 0.0062\left(\frac{w}{h}\right)^2 \quad \left(\frac{1}{2} \le \frac{w}{h} \le 10\right)$$

Inductance is calculated in two parts as

$$L'' = l\frac{Z_0}{c_a}\sqrt{\mu_r \epsilon_{eff}} \tag{2}$$

$$L' = \frac{\mu_0 l}{2\pi}\left[\log\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{2}{9}\left(\frac{w+t}{l}\right)\right] \tag{3}$$

where L' is a simplified expression for the inductance without accounting for an infinite ground plane while L'' does. The average of these two values is used to approximate inductance in an MCPM with a finite ground plane.

In the above equations, *w*, *l*, *t*, and *h* represent width, length, trace thickness and isolation thickness (mm), respectively. *f* is frequency (kHz), σ is the conductivity of the trace (S/m), μ_0 is permeability of free space ($4 \times \pi \times 10^{-7}$ H/m), Z_0 is the characteristic impedance (Ω), ϵ_{eff} is effective dielectric permittivity, and c_a is capacitance per meter (pF/m).

B. Limitations of microstrip model in power modules

While Eq. (1) has some boundary conditions to ensure the highest accuracy, this equation actually shows good resistance extraction results for MCPMs applicationand has been verified in the next section. The inductance model in Eq. (2) assumes an ideal infinite ground plane. To estimate the finite ground plane effect, Eq. (2) is averaged with an equation without a ground plane (Eq. (3)). This has been proven in [12] to yield a better estimation for MCPM inductance extraction. However, inductance is a frequency dependent value. At low frequency, inductance values are normally higher. Conversely, at high frequency, these inductance values are generally much lower than what is obtained. This is because at high frequency, due to the skin depth effect, current tends to concentrate at the surface of the conductor. This in turn creates a smaller current loop, thus the resulting inductance value is smaller. Eq. (2) above does not account for frequency. Therefore, this will result in inaccurate prediction when the frequency input is varied.

C. Extraction results with microstrip based formulas

Using the above-mentioned models, electrical parasitic values for the DC^+ to DC^- loop (Fig. 2) are then extracted and compared to the numerical results from FastHenry at 10, 20, 50, 100, 500 kHz, and 1 MHz. Figs. 4 and 5 below show the RL extraction comparison between FastHenry and the microstrip model. As can be seen in Fig. 4, the resistance results from microstrip formulae show small underestimation to the numerical results from FastHenry at low frequency region, while have a good match at high frequency region.. Overall, this model shows good approximation to the FastHenry simulation with the maximum errors of only 8%. The inductance results from Fig. 5 show a good approximation for the higher frequency region. The relative error fluctuates between 11% and -7%. However, this model is frequency independent, thus yielding higher errors in the low frequency region.

It is worth mentioning that the approximate extraction time for FastHenry is about 300 seconds for this layout, while it is only 26-30 milliseconds using the microstrip formulae (Intel core i7 CPU clocked at 3.40 GHz). Even though the above-mentioned analytical formulas are quite attractive for fast approximation and yields good approximation for effective resistance, it does not capture the frequency dependent for trace

inductance. While inductance extraction has larger impacts in MCPMs application, a better model is required for MCPM parasitics extraction to overcome this limitation.

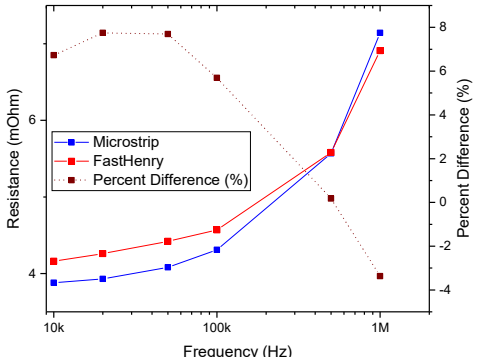

Fig. 4. FastHenry and microstrip resistance extraction for the example layout.

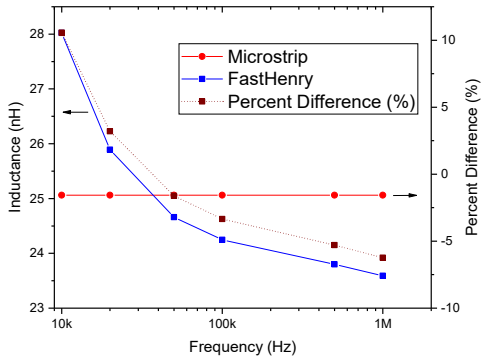

Fig. 5. FastHenry and microstrip inductance extraction for the example layout.

III. Response Surface Modeling

The main challenge of this work is increasing the accuracy of parasitic extraction over a wide frequency range without increasing computational effort. To predict interconnect parasitics more efficiently and accurately, a new modeling technique is required to overcome the aforementioned problems. To the best of our knowledge, closed-form formulae are not available for MCPM applications. Regardless, similar modeling techniques can be derived from previous work in [10], [13], and [14] to construct suitable models for MCPMs. Commonly, numerical solutions using method of moments (MoMs) or finite element analysis (FEA) in the work above are used along with interpolation techniques to generate proper formulae, assuming fixed frequency and dimension ranges. In this paper, it is shown that a model for MCPMs can be built from PEEC simulation results from FastHenry along with response surface modeling techniques.

A. Response surface formulation for rectangular traces

Response surface modeling is a mathematical model used to develop a relationship between selected design parameters $x_1, x_2, \ldots x_k$ to a chosen response y. This is normally applied when the responses are hard to obtain due to computationally expensive numerical simulations [15]–[17]. In an optimization framework, this method provides a fast and accurate cost function. Generally, there are three main steps to build a response surface. First, some design parameters are selected—which can be accomplished using design of experiment methods. Then, the simulations are run for these different design configurations. Finally, this mathematical model can be used to map the parameter space to the responses.

1) Parameter design space

In an MCPM structure, there are many parameters that impact the parasitic results of an individual rectangular trace. These include the width and length of each trace, spacing between traces, operating frequency, thickness of the isolation material, and thickness of the metal layers. As mentioned above, some previous modeling attempts in [12] also found that different sizes of the backside metallization have some significant effects on the extraction results. Thus, to correctly model the parasitics of rectangular traces in MCPMs, at least six design parameters are needed.

This increases the number of simulations needed which is challenging for the response surface algorithm to create an accurate and smooth function. In the MCPM optimization loop, while all parameters above are accounted for, only the widths and lengths of the traces are used to optimize the layout. Therefore, a response surface model can be built considering two design parameters: the width and length of each rectangular trace. Since other parameters can be treated as constants in the optimization loop, a library can be built based on standard DBC/DBA substrates and standard footprints of MCPMs available on the market. A Manufacturer Design Kit (MDK) interface in PowerSynth [18] allows users to input different power module layer stack files containing material and dimension information. This information is used for both thermal and electrical analysis in the software. To start with, a layer-stack file is imported into PowerSynth through this interface (Fig. 6). Then, a simple 2D parameterization of 10x10 width and length values is created as in Table I below, which shows the boundary for each parameter based on the imported substrate sizes (A × B) (Fig. 7). The minimum width value is based on the user-defined standard design rule available in our software database, while minimum length value is estimated based on the substrate sizes.

Table I. Parameter choices range

Parameter	Range (mm)
W	Design rule minimum to max (A, B)/2
L	max (A, B)/4 to max (A, B)

2) Simulation setup

The simulations are then automatically setup based on the above data points. A frequency range is also provided for frequency sweep simulation in FastHenry. Due to the skin depth effect [10] at high frequency, current tends to concentrate at the surface of the conductor. Therefore, care must be taken in the simulation to create a correct mesh. Eq. (4) is used to estimate the skin-depth value, where δ is the skin depth (in m), σ is the conductivity of the material (S/m), ω is angular frequency, and μ is permeability of the isolation material ($4 \times \pi \times 10^{-7}$ H/m).

$$\delta = \sqrt{\left(\frac{2}{\omega\mu\sigma}\right)} \tag{4}$$

The skin depth value is first computed based on the maximum frequency of the given frequency range. This value is then assigned to the smallest filament, the basic element in FastHenry, to form the mesh for traces and DBC backside metallization. This ensures accurate extraction over the desired frequency range. In the FastHenry mesh, the center filament of the trace is the largest, while the smallest filaments are located at the outermost region. Starting from the boundary of the trace, the next filament going toward the center will double the size of the previous one (Fig. 7). Therefore, the number of filaments can be calculated based on the width and length of any given rectangular trace, and the computed skin depth value. To accurately simulate the image current on the DBC backside metallization, the mesh of this plane is designed to be finer below the rectangular trace. This guarantees good extraction accuracy for resistance and self-inductance for each individual rectangular trace.

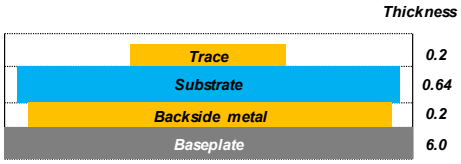

Fig. 6. Layer stack imported into PowerSynth.

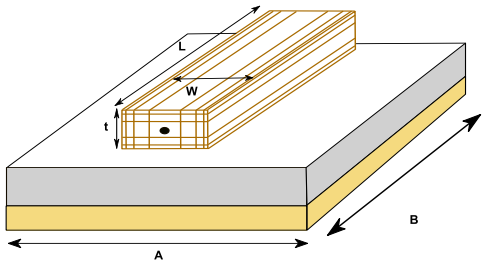

Fig. 7. Example mesh for a rectangular trace in FastHenry.

A Python script is used to automatically compute the skin depth value for every different width and length. Then, a FastHenry script is written to automatically run a batch simulation for each different configuration. To properly capture frequency-dependent effects, the simulation for each width and length configuration is run at five frequency points per decade. The SciPy [19] package in Python is then used to form interpolated functions for self-inductance and resistance over frequency. Then, a finer frequency sweep data can be collected for each width and length. The data is then collected to fit the response surface model. This forms a look-up table for each different frequency choice.

3) Data interpolation

Several techniques are available for fitting the data such as support vector regression (SVR), kernel ridge (KR), ordinary kriging, etc. Ordinary kriging [20] has been chosen to build the response surface model. Generally, support vector regression and kernel ridge are suitable for very large design spaces consisting of more than four design parameters. This would increase the number of simulations needed to guarantee high prediction accuracy. While ordinary kriging methods only allow for 2-3 design variables, this is still sufficient to ensure a high prediction accuracy and a smooth surface. Fig. 8 and Fig. 9 below show the response surfaces for the resistance and self-inductance, respectively. Once the response surface model is created based on the given simulated points, it can be used to predict the parasitic results for any trace widths and lengths within the design space. It can be saved in the model library for different DBC/DBA types available on the market.

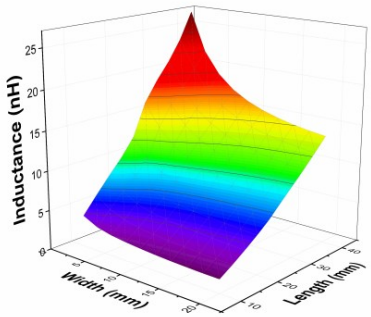

Fig. 8. Response surface for trace self-inductance.

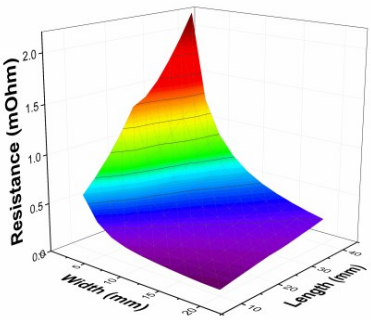

Fig. 9. Response surface for trace resistance.

B. *Response surface fomulation for 90-degree corners*

Adding two traces at 90-degree corners results in overestimation of inductance. This is because current usually concentrates at the inner corner, thus creating a smaller current loop. This, in turn, reduces the overall loop inductance value of the module. Some previous studies regarding 90-degree corner inductance overestimation correction are available for RF applications [21]-[22]. Since trace widths in RF applications are usually fixed, these models compute the correction over a unit length only. In MCPMs, however, traces widths are often variable. Therefore, a different technique needs to be applied to estimate the correction values. Fig. 10 shows how 90-degree corners are represented in both PowerSynth and FastHenry. To connect the rectangular trace pieces in PowerSynth (Fig. 10(a)), half of the width values of the two connecting traces are incorporated in the length values of the other traces. To prevent overestimation, a representation with finer corner meshing in FastHenry (Fig. 10(b)) is designed to correct for this effect. As

can be seen in Fig. 10(b) two rectangular traces (Section III.A) are connected at a right angle. The mesh of each piece is designed as mentioned in Section III.A. Finely meshed rectangular pieces at the corner are considered to capture the current crowding effect. The extracted inductance result from this representation is subtracted from the result of adding two conductors in PowerSynth. Thus, this correction value can be evaluated later as a function of trace widths W1 and W2. The third design parameter L can be estimated based on the size of the substrate. This ensures the structures lie within the substrate boundaries. The ordinary kriging method is then performed as mentioned in Section III.A to form the correction model.

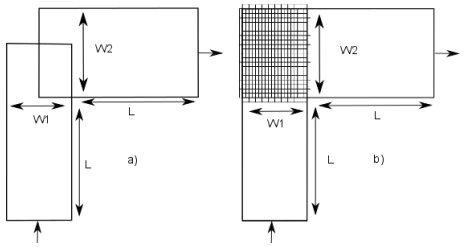

Fig. 10. (a) 90-degree corner approximation in PowerSynth, (b) 90-degree corner simulation in FastHenry.

The correction values from the response surface model are then applied to two 90-degree corners in the example layout. For this layout, the correction has been applied on a 4x4 (mm) and a 4x10 (mm) corner. By applying this correction model along with the traces parasitic extractions using response surface in Section III.A, the loop parasitic inductance and resistance can be extracted and compared to FastHenry PEEC solver.

C. Response surface validation against FastHenry

Accurate parasitic inductance and resistance of bondwires is first obtained by running FastHenry simulation for each bondwire group. This captures both the mutual inductance effect of two parallel wires as well as the proximity effect between them [23]. Since the distance between two bondwires is typically fixed for a device, only the length of the bondwire group is changed during the optimization process. Thus, an interpolation between the length of a bondwire group and its parasitic values can be easily formed. While there are many possible bondwire diameters, arrangements, and spacings to consider, this work is primarily focused on improving the parasitic extraction of the layout traces. Therefore, the design variables associated with bondwire groups are considered fixed in this study. Future work will focus on more accurate bondwire modeling to incorporate with the response surface modeling here. For this layout, the bondwire resistance and inductance values are 1.25 $m\Omega$ and 2.73 nH, respectively. Since the bondwire diameters (0.3 mm) are close to skin depth value in this case, these values are practically independent with respect to frequency. Finally, the response surface model for both traces and corners along with the interpolated equation for bondwire groups are used to replace the existing formulas in PowerSynth.

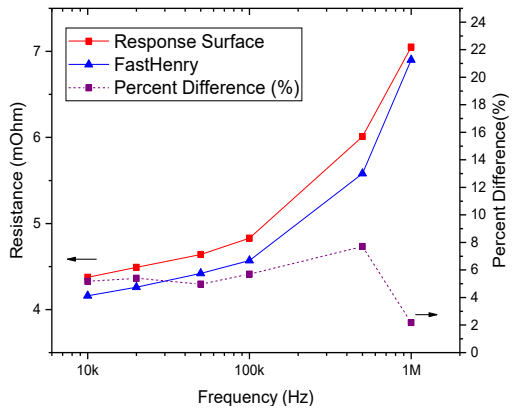

Fig. 11. FastHenry vs. response surface resistance comparison.

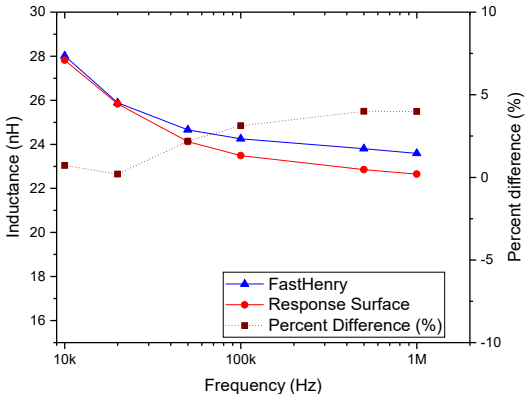

Fig. 12. FastHenry vs. response surface inductance comparison.

Fig. 11 above shows the comparison results between FastHenry resistance extraction and PowerSynth prediction using the response surface model. According to these results, the highest error of 7.8% occurs at 500 kHz, while the lowest is 2.1% at 1 MHz. Fig. 12 above shows the comparison between FastHenry and the response surface inductance extraction with corner correction. Overall, the inductance extraction results using response surfaces with corner correction have shown a maximum error of 3.98 % when compared to FastHenry. Table II below shows the time comparison between response surface parasitic extraction, and PEEC simulation in FastHenry. This has shown a nearly 6000 times improvement in extraction speed, while ensuring high extraction fidelity. Therefore, this model is suitable for use in the optimization loop to improve the prediction accuracy of PowerSynth. The parasitic extraction from microstrip, response surface, and simulation in FastHenry are compared in Fig. 13 and Fig. 14. For parasitic resistance, both response surface and microstrip model shows less than 8% of extraction errors in compared to FastHenry. For parasitic inductance, the frequency dependent effect has been correctly captured, while a prediction error of less than 5% is achieved over the entire frequency range.

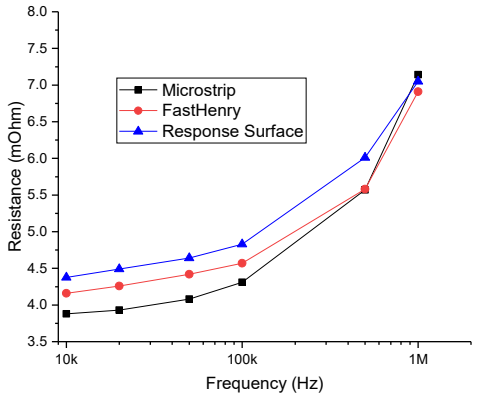

Fig. 13. Parasitic resistance comparison for three different models.

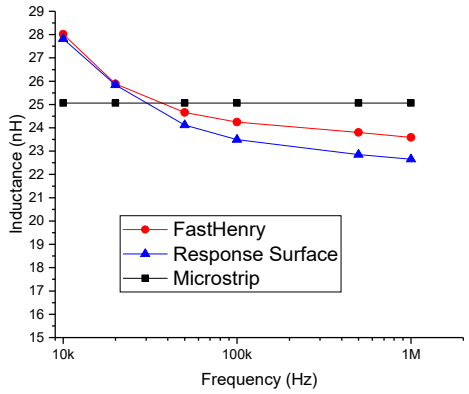

Fig. 14. Parasitic inductance comparison for three different models.

Table II. Extraction Speed Comparison

	FastHenry	Response Surface	Speed up
Extraction Time	~300 s	~50 ms	x6000

IV. Measurement Results and Model Validation

A. Measurement setup with LCR metter

The test vehicle is built upon an aluminum nitride DBC substrate. Copper layers are 8 mils thick and the ceramic is 25 mils. Then, the abovementioned layout is etched into the topside copper layer. As shown in the setup in Fig. 15, two copper connection wires are soldered to the positive and negative sides of the half-bridge, which are then connected to the HP 4284A LCR meter (Fig. 16) through an HP16047A test fixture. The RL results are taken at test frequencies between 10kHz and 1MHz for three frequency points per decade. To measure the capacitance, another test vehicle is used where two connection wires are taped to the top and bottom side of the DBC substrate (Fig. 16).

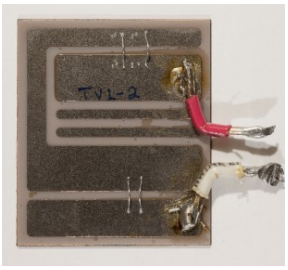

Fig. 15. Fabricated test vehicle.

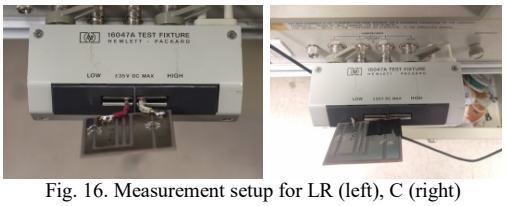

Fig. 16. Measurement setup for LR (left), C (right)

B. Measurement setup using Time Domain Reflectometry

To increase confidence in our extraction results, measurement using Time Domain Reflectometry (TDR) is also setup to validate the inductance and capacitance values at very high frequency. The same test vehicle is connected to a 50 Ω coax cable, which is then interfaced with the sampling oscilloscope, model Tektronix 11801B. The inductance is calculated by first shorting the leads with a copper plate. Then the reflected waveform is sampled after the plate is removed. Eqs. (5) and (6) below are used to calculate the inductance and capacitance.

$$L_{self} = \frac{Z_0}{2V}\int_0^{\infty}(W_{TDR} - W_{Short})dt \quad (5)$$

$$C_{total} = \frac{1}{2Z_0V}\int_0^{\infty}(W_{Open} - W_{TDR})dt \quad (6)$$

where Z_0 is the characteristic impedance, V is the pulse amplitude, W_{TDR} is the reflected waveform, and W_{Short} is the short circuit waveform. The result in Fig. 17 below shows the inductance value as 24.86 nH. The capacitance result is also shown in below.

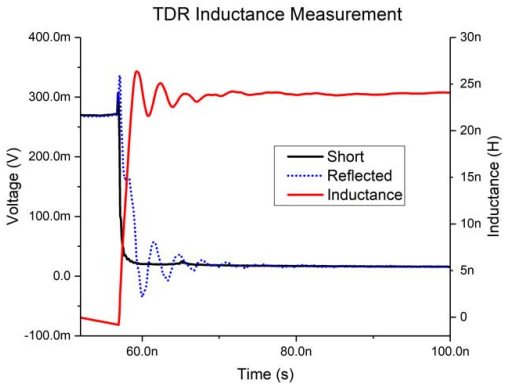

Fig. 17. TDR inductance measurement results.

C. *Model validation*

As previously mentioned, the capacitance model in PowerSynth yields good approximation of the measurement results. The results from PowerSynth capacitance extraction and measurement are shown in Table III below. This has shown only 5.41% and 0.85% error against LCR and TDR measurements, respectively.

Table III. Capacitance Model Comparison

PowerSynth Cap	Measurement (LCR)	Measurement (TDR)
169.5 pF	160.8 pF	170.95 pF

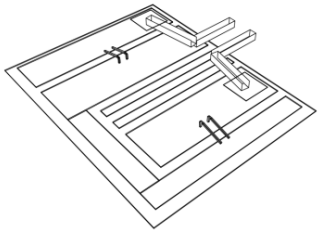

Fig.18 Exported layout from FastHenry

To validate the model against measurement results, another FastHenry layout with connection wires (Fig.18) at DC+ and DC- terminals is created. Both the connection wire and its solder materials are modeled to replicate the real layout. Then, this is used to estimate the contribution of the connection wires and solder to the parasitics results of the half-bridge module. Finally, these contributions are added to the existing response surface results. Fig. 19 and Fig. 20 compare the parasitic extractions from the response surface with the measurement results. For inductance (Fig. 19), this yields a maximum error of 9.5%, while the maximum error for resistance extraction (Fig. 20) is only 7.1%. Additionally, the inductance result at 1 MHz (26.1 nH) is also very close to the TDR measurement above (24.86 nH). While these results have shown less than 10% error overall, the sources of error might come from bondwire contacts as well as wire connection contacts. Future studies will be performed on these contacts to improve the parasitic extraction accuracy.

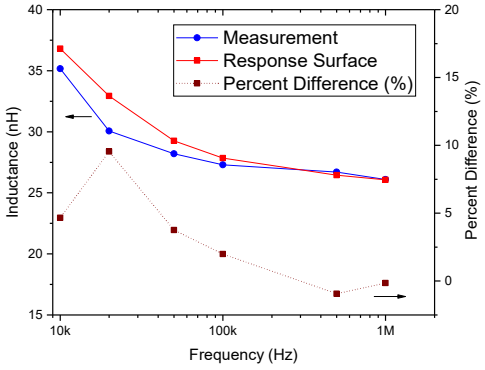

Fig. 19. Response surface vs LCR measurement inductance.

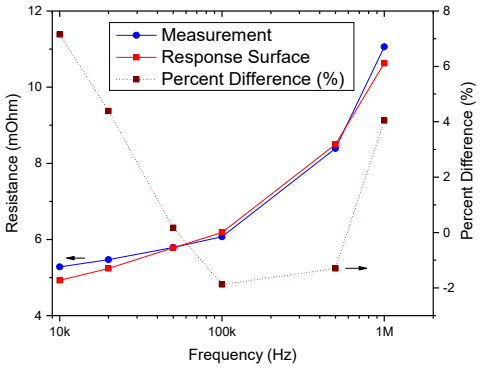

Fig. 20. Response surface vs LCR measurement resistance.

V. LAYOUT OPTIMIZATION WITH RESPONSE SURFACE

A multi-objective optimization for R, L, and C has been performed employing NSGA-II algorithm [24] and the response surface models at 100 kHz in PowerSynth. The results form a Pareto front, where users can select between multiple layouts (Fig. 21). The layout (Fig. 22) shows the most optimized module for parasitic resistance and inductance (red circle in Fig. 21). This layout has shown parasitic inductance and resistance reduction of nearly 54.5% and 36.6%, respectively. On the other hand, there is a trade-off of only 9% increase in capacitance. With a reduction of 54.5% of inductance, which has a higher impact to MCPM performance, the increment in capacitance is negligible. It is worth mentioning that 3768 layouts have been synthesized in the total optimization time of 282 seconds. Doing the same work using FastHenry for cost function evaluation is estimated to take approximately 14 days to finish.

Table IV. Optimized Layout RLC Extraction Results at 100 kHz

	R (mOhm)	L (nH)	C (pF)
Example Layout	4.83	23.49	169.5
Optimized RL	3.06	10.69	185.79
Improvement (%)	36.6	54.5	-9

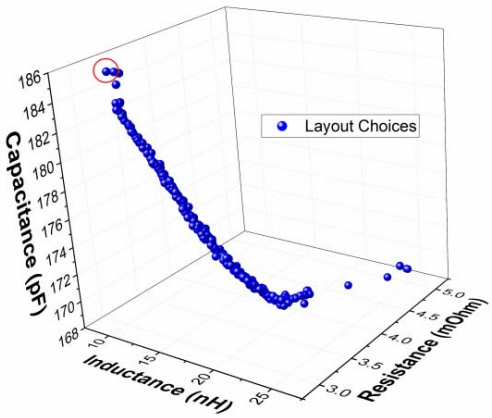

Fig. 21. Pareto fronts representation in PowerSynth.

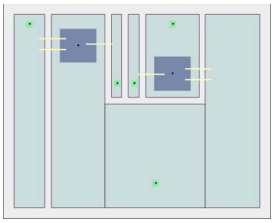

Fig. 22. Optimized layout for resistance and inductance.

VI. Conclusion and Future Works

In conclusion, the parasitic extraction results using response surface models have shown improvements in extraction accuracy with only a slight increase in computation speed when compared with the previously employed microstrip formulation. This is because high fidelity simulations can be run prior to optimization process to create these reduced order models. Therefore, these models are suitable for our optimization loop in PowerSynth. Observed overestimation at 90-degree corners and attempts to correct this inductance value have greatly improved the prediction accuracy. However, this is only true for simple layout cases, where uniform current distribution can be assumed. Future study will allow response surface models to predict more complicated structures. This would require forming multi-port unit cells (traces) rather than a set of two-port rectangular traces. In this way, the optimization algorithm in the backend of the software will be able to synthesize more complicated and interesting layout structures.

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References

[1] D. Grider *et al.*, "10 kV/120 A SiC DMOSFET half H-bridge power modules for 1 MVA solid state power substation," in *2011 IEEE Electric Ship Technologies Symposium, ESTS 2011*, 2011, pp. 131–134.

[2] F. Xu *et al.*, "High temperature packaging of 50 kW three-phase SiC power module," *8th International Conference on Power Electronics - ECCE Asia: "Green World with Power Electronics", ICPE 2011-ECCE Asia*. pp. 2427–2433, 2011.

[3] Z. Chen *et al.*, "A 1200-V, 60-A SiC MOSFET multichip phase-leg module for high-temperature, high-frequency applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2307–2320, 2014.

[4] Y. Ren *et al.*, "Voltage Suppression in Wire-bond Based Multichip Phase-leg SiC MOSFET Module using Adjacent Decoupling Concept," *IEEE Trans. Ind. Electron.*, vol. 46, no. c, pp. 1–1, 2017.

[5] Y. Shen *et al.*, "Parasitic inductance effects on the switching loss measurement of power semiconductor devices," in *IEEE International Symposium on Industrial Electronics*, 2006, vol. 2, pp. 847–852.

[6] A. Domurat-Linde and E. Hoene, "Analysis and Reduction of Radiated EMI of Power Modules," in *Integrated Power Electronics Systems (CIPS), 2012 7th International Conference on*, 2012, vol. 9, pp. 1–6.

[7] D. Cottet and A. Hamidi, "Numerical Comparison of Packaging Technologies for Power Electronics Modules," in *IEEE 36th Power Electronics Specialists Conference*, 2005, vol. 41, no. 0.

[8] F. Luo *et al.*, "Design Considerations for GaN HEMT Multichip Half- bridge Module for High-Frequency Power Converters," in *APEC*, 2014, pp. 537–544.

[9] B. W. Shook *et al.*, "Multi-objective layout optimization for multi-chip power modules considering electrical parasitics and thermal performance," in *2013 IEEE 14th Workshop on Control and Modeling for Power Electronics, COMPEL*, 2013.

[10] S. H. Hall and H. L. Heck, *Advanced Signal Integrity for High-Speed Digital Designs*. New Jersey: A John Wiley & Sons, INC, 2009.

[11] M. Kamon, M. J. Tsuk, and J. K. White, "FASTHENRY: a multipole-accelerated 3-D inductance extraction program," *IEEE Trans. Microw. Theory Tech.*, vol. 42, no. 9, pp. 1750–1758, 1994.

[12] Z. Gong, "Thermal and electrical parasitic modeling for multi-chip power module layout Synthesis," University of Arkansas, 2012.

[13] A. R. Djordjevic, M. Stojilovic, and T. K. Sarkar, "Closed-form formulas for frequency-dependent per-unit-length inductance and resistance of microstrip transmission lines that provide causal response," *IEEE Trans. Electromagn. Compat.*, vol. 56, no. 6, pp. 1604–1612, 2014.

[14] S. H. Lee, K. Mao, and J. M. Jin, "A complete finite-element analysis of multilayer anisotropic transmission lines from DC to terahertz frequencies," *IEEE Trans. Adv. Packag.*, vol. 31, no. 2, pp. 326–338, 2008.

[15] W. Chen and S. K. Sitaraman, "Response Surface and Multiobjective Optimization Methodology for the Design of Compliant Interconnects," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 4, no. 11, pp. 1769–1777, 2014.

[16] X. Song *et al.*, "Surrogate-Based Analysis and Optimization for the Design of Heat Sinks With Jet Impingement," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 4, no. 3, pp. 429–437, 2014.

[17] L. Xia *et al.*, "Modeling of 3-D Vertical Interconnect Using Support Vector Regression," *IEEE Microw. Wirel. Components Lett.*, vol. 16, no. 12, pp. 639–641, 2006.

[18] J. Main, "A Manufacturer Design Kit for Multi-Chip Power Module Layout Synthesis," University of Arkansas, 2017.

[19] E. J. and T. O. and P. P. and Others, "SciPy." [Online]. Available: http://www.scipy.org/[Online; accessed 2017-08-27].

[20] W. C. M. van Beers and J. P. C. Kleijnen, "Kriging for interpolation in random simulation," *J. Oper. Res. Soc.*, vol. 54, no. 3, pp. 255–262, 2003.

[21] L. K. Warne, "Eddy current power dissipation at sharp corners," *IEEE Trans. Microw. Theory Tech.*, vol. 42, no. 2, pp. 283–290, 1994.

[22] T.-S. Chen, "Determination of the Capacitance, Inductance, and Characteristic Impedance of Rectangular Lines," *IEEE Trans. Microw. Theory Tech.*, vol. 8, no. 5, pp. 510–519, 1960.

[23] G. S. Smith, "Proximity effect in systems of parallel conductors," *J. Appl. Phys.*, vol. 43, no. 5, pp. 2196–2203, 1972.

[24] K. Deb *et al.*, "A Fast and Elitist Multiobjective Genetic Algorithm: NGSA-II," *IEEE Trans. Evol. Comput.*, vol. 6, no. 2, pp. 182–197, 2002.