# Fast and Accurate Full-chip Extraction and Optimization of TSV-to-Wire Coupling

Yarui Peng[1] Dusan Petranovic[2], and Sung Kyu Lim[1]
[1]School of ECE, Georgia Institute of Technology, Atlanta, GA, USA
[2]Mentor Graphics, Fremont, CA, USA
yarui.peng@gatech.edu, limsk@ece.gatech.edu

***Abstract*—In this paper, for the first time, we model and extract the parasitic capacitance between TSVs and their surrounding wires in 3D IC. For a fast and accurate full-chip extraction, we propose a pattern-matching-based algorithm that considers the physical dimensions of TSVs and neighboring wires and captures their E-field interactions. Our extraction method is accurate within 1.9% error for a full-chip-level design while requiring negligible runtime and memory compared with a field solver. We also observe that TSV-to-wire capacitance has a significant impact on the noise of TSV-based connections and the longest path delay. To reduce TSV-to-wire coupling, two full-chip optimization methods are presented. We increase the minimum distance between TSV and wire and use grounded guard ring around TSV for noise reduction and protection. Results show both optimization methods are highly effective in noise reduction with minimal overhead in routing congestion and delay increase.**

## I. Introduction

Through-silicon-via (TSV) is widely used for vertical interconnection in 3D IC. Figure 1 shows the 3D IC structure where two dies are bonded in face-to-back fashion with via-first technology. TSV parasitics in 3D IC are not fully extracted using current parasitic extraction tools, but only wire-to-wire capacitance for each die are extracted separately. Tools like StarRC and Calibre xRC can extract TSV-to-TSV coupling, but TSV-to-wire capacitance is ignored. In addition, TSVs are often used as interconnecting components in silicon interposer, the capacitance between TSV, microbumps and redistribution layer (RDL) needs to be considered in packaging level as well. The parasitic extraction using a field solver can handle small designs, but this requires huge computing resources and runtime, which is not feasible for full-chip design. Some previous works investigated TSV-to-TSV coupling parasitics [1], and TSV with RDL connection is studied in [2], but TSV-to-RDL coupling capacitance is ignored. TSV-to-wire parasitic extraction using a field solver is discussed in [4], however, its impact on the full-chip level remains unknown. Therefore, a fast and accurate TSV-to-wire capacitance extraction tool is desired for both layout optimization and accurate analysis of timing, power, and signal integrity.

## II. Modeling of E-field Sharing

### A. Effect of Multiple Wires

Traditional models only consider one pair of TSV and wire at one time. However, if multiple wires are located around TSV, the E-field will be shared among the wires. Traditional modeling method overestimates the capacitance as no neighbors are considered. We use a structure shown in Figure 2(a) to study the multiple wire effects. Figure 2(b) shows the E-field distribution simulated using a field solver (HFSS) when four wires are considered. The E-field between the nearest neighbor and TSV is the strongest, which forms the largest capacitance. If there is no outer wires, the outer-most wire also shows a large total capacitance since the E-field sharing is smaller. Wires between inner-most and outer-most wire show relatively small coupling capacitance.

This research is supported by the Semiconductor Research Corporation under CADTS Task 2239.

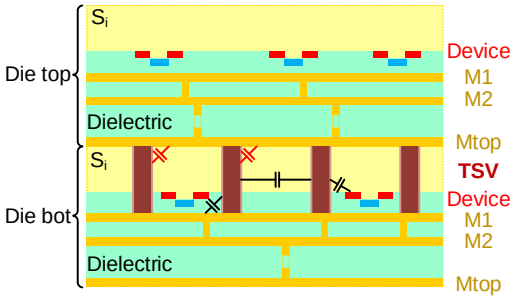


Fig. 1. Structure of 3D IC with 2 dies, the capacitance in red is the TSV-to-wire capacitance extracted in this work.

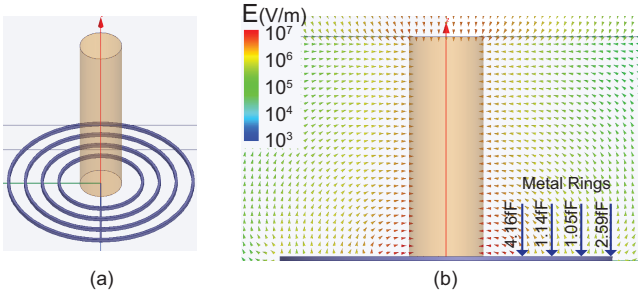


Fig. 2. Multi-wires effects. (a) TSV-ring structure. (b) E-field distribution around TSV.

### B. Corner Segment Effect

The E-field sharing effect is also observed in different parts of a wire. We use one TSV-wire pair as an example and extract the capacitance using a field solver (Synopsys Raphael). Figure 3(a) shows our simulation structure. We break the wire into several segments, and each segment is $0.5\mu m$ in length. We observe that the corner segment shows

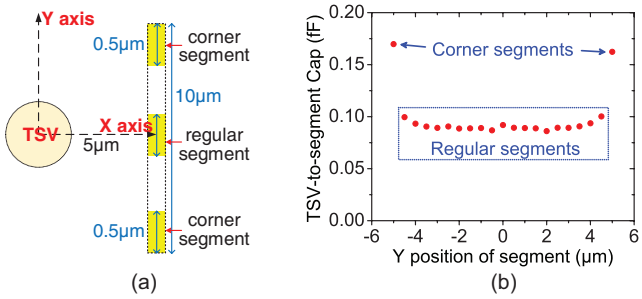


Fig. 3. Corner segment impact. (a) Simulation structure with wire segment in $0.5\mu m$ length. (b) Extraction result for each segment.

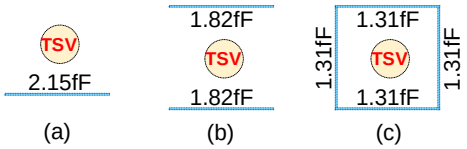


Fig. 4. Impact of wire coverage around TSV on coupling capacitance.

much larger (1.8×) capacitance than the regular segment. This is because the corner segment is connected with the neighboring segment only at one side. This corner segment has larger capacitance even though it is located further away from the TSV. Therefore, for accurate extraction, corner segments need to be considered separately, especially for short wires. Otherwise, the extraction result will be underestimated.

### C. Wire Coverage Effect

The E-field sharing effect also depends on how much part of a TSV is surrounded by metal wires. As shown in Figure 4, due to the E-field sharing, the coupling capacitance is evenly distributed among all the surrounding wires. Therefore, the unit length capacitance is larger when a TSV is only surrounded on one side. When the wire coverage around a TSV is high, even though the total capacitance increases, the unit length capacitance decreases. Therefore, the wire coverage effect also needs to be taken into account for an accurate TSV-to-wire capacitance extraction.

## III. Extraction and Verification

In this section, we discuss how we build our TSV-to-wire coupling capacitance libraries in which multiple wires with all the aforementioned effects are considered. We build two libraries for regular segments, i.e., line library and ring library, and one library for corner segments.

### A. Line Library

We build a line library for TSVs covered by wires on one side. As shown in Figure 5(a), the line library is built by dividing the metal wires into segments and extract all the capacitance at the same time. The wire segment length is different depending on its distance from the TSV and the location angle to the TSV. For example, wire segments far from TSV with large location angle will be longer. Thus, a coarse grid structure can be applied to wires farther away from the TSV, while a finer grid structure can be used for closer wires. This helps to reduce library generation time using a field solver without sacrificing the extraction accuracy.

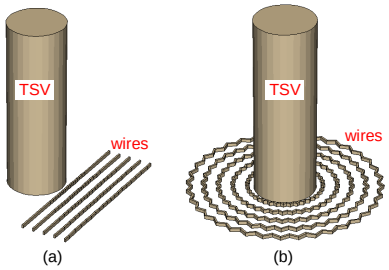


Fig. 5. Test structures for library generation. (a) Structure for line library. (b) Structure for ring library.

The line library assumes that only one side of TSV is surrounded by metal wires. In general, when TSV is surrounded by wires on multiple sides, the line library will give larger coupling capacitance, since it assumes there is less E-field sharing among wires. As the line library needs less complicated geometries, it helps reducing library generation time and memory space. In addition, we can extract several entries at the same time.

### B. Ring Library

We build a ring library for TSVs covered by wires from all sides. As shown in Figure 5(b), we pick one test segment and duplicated it to form a ring around TSV. Then we extract the total capacitance of the ring and divide it by the total number of the ring segments. To simulate multiple wires, multiple rings are added around TSV. We perform this on all test structures and save extraction results into the library. The ring library is built assuming a heavy E-field sharing around TSV. Thus, in general cases, when TSV is covered by fewer metal wires, it will underestimate the coupling capacitance. Although, the ring library needs to extract only one capacitance at a time, the overall simulation time is the longest due to the complex geometries elements such as polygons used to form a ring.

### C. Corner Library

Since the corner segment has only a neighbor on one side, and its side wall also contributes to the coupling, it shows much larger capacitance compared with regular segments. The test structure is similar to the one used in the line library. However, we merge all the regular segments and only extract the capacitance of the corner segment. Compared with other libraries, it has the largest capacitance value. The geometry complexity for corner library is smallest, but unlike the line library where many entries can be extracted in parallel, corner library needs longer runtime to build.

### D. Pattern Matching Algorithm

We develop an algorithm for pattern-matching-based TSV-to-wire coupling capacitance extraction. The extraction is conducted on each TSV one by one. Wires shorter than $2\mu m$ is ignored. After one TSV is picked, we divide the space into

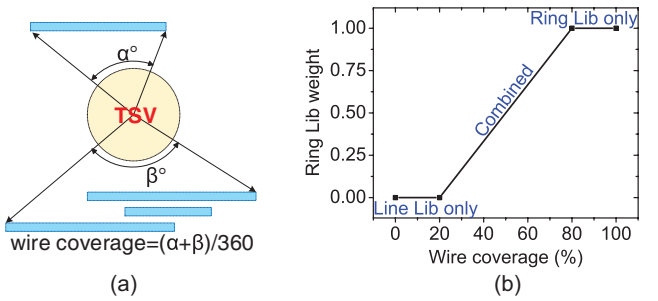


Fig. 6. Our combined method. (a) shows the calculation of wire coverage, (b) shows the calculation of weighted average.

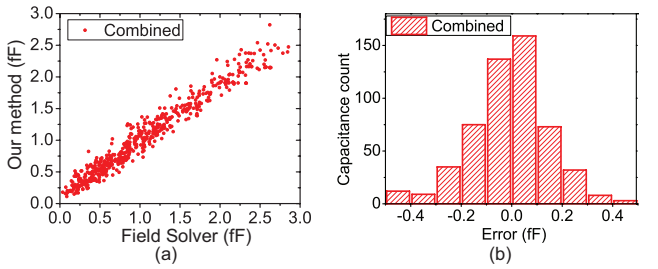


Fig. 7. Full-chip Verification using combined method. (a) shows extraction result comparison, (b) shows error histogram.

72 circular sectors, each with 5° in central angle. Wires are cut into segments at the sector boundary. Then we exclude segments beyond the distance threshold and gather segments with the same location angle into a list. Each TSV has 72 lists and each list contains the segments with the same location angle to the TSV. The look-up procedure is applied to each segment in the list and it looks for the closest entry that matches the segment. For corner segments, results from corner library is used. For regular segments, we combine the line library and ring library based on wire coverage around the TSV. If the wire coverage is above 80%, we use the ring library only. On the other hand, if the coverage is below 20%, we use the line library only. Otherwise, we use a weighted average from both libraries. Wire coverage calculation is shown in Figure 6(a) and the ring library weight is shown in Figure 6(b). Finally, the capacitance for the same net will be added and annotated into SPEF file and used for full-chip analysis.

### *E. Validation Against a Field Solver*

For full-chip verification, we implement a two-die 3D design and apply our method to all TSVs. The TSV influence region for our extraction is $10\mu m$. We run Raphael simulation on each TSV with $10\mu m$ as simulation window size. Using a single ring library gives a 8.3% underestimated total capacitance, while using a single line library gives a 5.3% overestimated total capacitance. However, both of them are accurate enough: an average error of 0.171fF for the ring library only case and 0.163fF for the line library only case. Full-chip extraction result is shown in Figure 7. We conclude that both ring and line libraries are accurate for multiple wires, and our combined method considering wire coverage effect is very fast and highly accurate.

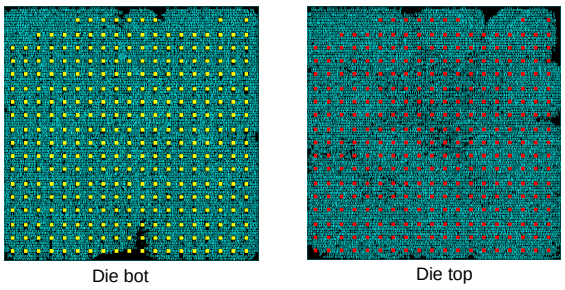


Fig. 8. Placement layout shots of FFT64. The footprint is $380\mu m \times 380\mu m$.

TABLE I
TSV-TO-WIRE COUPLING FULL-CHIP IMPACT.

| Is TSV-to-wire included? | no | yes |
|---|---|---|
| Longest path delay (ns) | 4.48 | 5.08 (+13.4%) |
| Total power on TSV net (mW) | 0.303 | 0.356 (+17.6%) |
| Total net switching power (mW) | 2.42 | 2.50 (+3.3%) |
| Total noise on TSV net (V) | 32.5 | 78.2 (+104%) |

## IV. FULL-CHIP TSV-TO-WIRE IMPACT

### *A. Design Specification and analysis flow*

We use a 64 point FFT design based on 45nm technology. There are 47K gates in this design and it is partitioned into two dies. The TSVs are $15\mu m$ in height and $2.5\mu m$ in radius. The bottom die has 330 TSVs with the landing pad on M1. TSVs are evenly distributed on the bottom die with about $18\mu m$ spacing to each other. Therefore, we pick $18\mu m$ as our extraction distance threshold to avoid other TSVs while ensure all wires within TSV influence region is extracted.

Full chip placement results are shown in Figure 8. The top die has TSV landing pad on its top metal layer to connect TSVs from the bottom die. For our study, only the capacitance between TSV and metal wires on top metal layer is extracted since other metal layers are blocked by either device layer or metal layers. We assume the wires are routed in preferred direction. Since the metal layer M4 to M6 have the same wire dimension, our library can handle design with M4 to M6 as their top metal layer. We present our design up to M4 in following sections. With the usage of more metal layers, the wire length on top metal layer is reduced.

We apply our pattern matching method to FFT design and then use Primetime to merge all the parasitic file, e.g., TSV-to-wire coupling, wire-to-wire coupling and TSV-to-TSV coupling using the extraction method proposed in [3]. Then we use Primetime for full-chip timing and power analysis and use HSPICE for worst case noise analysis.

### *B. Full-chip Analysis*

The full-chip analysis result is shown in Table I. The critical path starts from a register in the top die, goes to the bottom die through TSV274, then goes back to the top die through TSV89 and ends on another register. As TSVs are on the critical path in this design, TSV parasitic affects the Longest-Path-Delay (LPD) of the whole design.

TSV coupling elements are the major part of TSV parasitics. However, if TSV-to-wire capacitance is ignored, there will be a large underestimation in TSV net capacitance and

TABLE II
KEEP-OUT-ZONE IMPACT ON FULL-CHIP DESIGN.

| KOZ size ($\mu m$) | 0.5 | 2.5 | 5 |
|---|---|---|---|
| Longest path delay (ns) | 5.08 | 4.95 | 4.77 |
| Total power on TSV net (mW) | 0.356 | 0.342 | 0.327 |
| Total net switching power (mW) | 2.50 | 2.47 | 2.45 |
| Total noise on TSV net (V) | 78.2 | 67.0 | 42.9 |

TABLE III
GUARD RING IMPACT ON FULL-CHIP DESIGN WITH $2.5\mu m$ KOZ.

| Guard ring width ($\mu m$) | 0 | 0.5 | 1.5 |
|---|---|---|---|
| Longest path delay (ns) | 4.95 | 4.98 | 5.01 |
| Total power on TSV net (mW) | 0.342 | 0.351 | 0.358 |
| Total net switching power (mW) | 2.47 | 2.475 | 2.479 |
| Total noise on TSV net (V) | 67.0 | 58.0 | 53.6 |

TSV-induced delay and noise. Without TSV-to-wire coupling capacitance, there is a 2.01pF underestimation on total TSV net capacitance and a 0.6ns underestimation on LPD. After TSV-to-wire capacitance is considered, the total power on TSV net also increases by 17.5% due to larger capacitance. And there is also a noticeable change on total net switching power though its impact on total power is negligible. The result shows that total noise on TSV net doubled in worst case after the TSV-to-wire coupling is plugged in. Therefore, TSV-to-wire coupling needs to be accurately extracted and analyzed in the full-chip level.

## V. COUPLING MINIMIZATION

### A. Impact of Keep-Out-Zone

For TSV-to-wire coupling reduction, minimizing the total wire length on top metal layer while increasing the minimum distance between TSV and nearest wire help reducing TSV-to-wire coupling. We define this minimum distance as Keep-Out-Zone (KOZ) of the top metal layer routing. We designed our FFT with different KOZ size. The original design has a KOZ of $0.5\mu m$. With larger KOZ, the capacitance between nearest wire and TSV will reduce. Also, larger KOZ reduces routing resources on top metal layer. Therefore the total wire length on the top metal layer decreases with larger KOZ. We re-designed our top die with a KOZ size of $2.5\mu m$ and $5\mu m$ while we kept the placement result. Increasing KOZ reduces the total wirelength on the top layer but makes routing on other layer more crowded.

We perform full-chip analysis with updated extraction results. Results are shown in Table II. With larger KOZ, total wire length on top metal layer is reduced. Therefore the TSV-to-wire coupling also shows smaller impact on the full-chip timing and noise. Compared with the original design, the LPD decreases by 2.6% and 6.1% for $2.5\mu m$ and $5\mu m$ KOZ, respectively. The KOZ impact on full-chip power result is much smaller since TSV-to-wire capacitance decreases but the wire-to-wire capacitance increases on other layer. Larger KOZ also helps reducing total noise on TSV net. The total worst-case noise on TSV net can be reduced by 14.3% and 45.1% for $2.5\mu m$ and $5\mu m$ KOZ, respectively. Therefore, we conclude that increase KOZ is effective in reducing TSV-to-wire coupling.

### B. Guard Ring Protection

Another way to protect the victim TSV is to use a grounded guard ring. The grounded guard ring shares some E-field around TSV, thus it introduces a ground capacitance on the TSV. This ground capacitance has small delay and power overhead on TSV nets, but it reduces the coupling noise on TSV net. Moreover, The guard ring blocks the E-field to other signal rings and reduces the coupling.

To extract the TSV-to-wire capacitance on a shielded TSV, we build libraries in which TSVs are surrounded by the guard ring. Based on previous layout with $2.5\mu m$ KOZ, we designed the FFT64 with guard rings. We add the guard ring in the KOZ region so that design placement and routing results are kept the same. Wwe perform full-chip analysis and the results are shown in Table III. The longest path will increase by 0.6% and 1.2% for $0.5\mu m$ and $1.5\mu m$ guard ring, respectively. This impact comes from two aspects. The ground capacitance on TSV increases but TSV-to-wire capacitance decreases. The total capacitance on TSV will always increase with wider guard ring since the metal coverage increased. Although there is a small increase on TSV switching power, guard ring impact on total power is negligible. Our results show that guard ring is very effective in TSV net noise reduction and the total TSV net noise reduces by 13.4% and 20.0% for $0.5\mu m$ and $1.5\mu m$ guard ring, respectively.

## VI. CONCLUSION

In this paper, various factors affecting TSV influence region and TSV-to-wire capacitance are studied. For fast and accurate full-chip TSV-to-wire capacitance extraction, we built a pattern matching algorithm which considers multiple wire effects, corner segment effects and wire coverage effects. We verified our method using real 3D IC layout against field-solver simulation. Then we applied our method on a FFT64 3DIC design and studied the TSV-to-wire impact on full-chip level. Analysis results show that TSV-to-wire coupling is not negligible and it has large impact on full-chip delay and TSV net noise. To alleviate the TSV-to-wire coupling, we tried to increase the KOZ around TSV in top routing layer and use a ground guard ring for further optimization. Our results show that both method are effective in TSV net noise reduction with small overhead on routing congestion, full-chip timing and power.

## REFERENCES


[1] J. Cho et al. Modeling and Analysis of Through-Silicon Via (TSV) Noise Coupling and Suppression Using a Guard Ring. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, pages 220–233, 2011.

[2] J. Kim et al. High-Frequency Scalable Electrical Model and Analysis of a Through Silicon Via (TSV). *IEEE Transactions on Components, Packaging and Manufacturing Technology*, pages 181–195, 2011.

[3] Y. Peng et al. On Accurate Full-Chip Extraction and Optimization of TSV-to-TSV Coupling Elements in 3D ICs. In *International Conference on Computer-Aided Design*, 2013.

[4] K. Salah. Analysis of coupling capacitance between TSVs and metal interconnects in 3D-ICs. In *IEEE International Conference on Electronics, Circuits and Systems*, pages 745–748, 2012.