Silicon Effect-Aware Full-Chip Extraction and Mitigation of TSV-to-TSV Coupling

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***Abstract*—This paper presents a silicon effect-aware multiTSV model. Through-silicon-via (TSV) depletion region, silicon substrate discharging path and electrical field distribution around TSV neighbor are modeled and studied in full-chip design. Verification with field solver and full-chip TSV-to-TSV coupling analysis in both the worst case and the average case show this model is accurate and efficient. It is found that 3-D nets receive more noise than their 2-D counterparts due to TSV-to-TSV coupling. To alleviate this coupling noise on TSV nets, two new optimization methods are investigated. One way is to utilize guard rings around the victim TSV so as to form a stronger discharging path, an alternative approach is to adopt differential signal transmission to improve noise immunity. These techniques have been implemented on 3-D IC designs with TSVs placed regularly or irregularly. Full-chip analysis results show that our approaches are effective in noise reduction with small area overhead.**

***Index Terms*—3-D IC, full-chip, noise optimization, TSV parasitic extraction, TSV-to-TSV coupling.**

I. Introduction

THROUGH-SILICON-VIA (TSV) is a popular choice to implement the vertical connections between dies in 3-D ICs. However, TSVs also introduce new parasitic elements to 3-D ICs. TSV is insulated from the substrate with a oxide liner which forms a metal-oxide–semiconductor (MOS) capacitor and it introduces a large capacitance coupling to other signals. Also, TSVs are hundreds of times larger in area compared with metal vias, which makes them as victims to many signal aggressors. The TSV coupling not only is a threat to the signal integrity and the logic functionality, but also degrades the delay and power benefits from 3-D IC. Thus, it is essential to have the coupling capacitance on TSVs extracted accurately for design verification, especially on critical 3-D nets such as clock and power supplies. TSV-capacitance extraction should be a fast procedure so that during the Place&Route stage, the TSV coupling information can be passed to the layout tools to perform 3-D aware delay and signal integrity driven design optimization. Field solver tools can perform a detailed extraction on arbitrary structures, but the long simulation time and large memory requirement make it inappropriate for the full-chip extraction. Therefore, in this paper, a fast and accurate extraction model is proposed for full-chip TSV-to-TSV coupling extraction.

Many previous works have studied the TSV-to-TSV coupling and proposed different models. It is still an open issue because the model needs to handle increasing number of TSVs and various TSV dimension scaling from technology upgrade. Irregular TSV placement where TSVs are not placed on the grid adds more complexity into the modeling. Weerasekera *et al.* [1] used empirical model equations. It is technology-specific and not scalable when TSV dimension changes. Xu *et al.* [2] proposed a Poisson equation based model, where inductors are included for high frequency modeling. Jonghyun *et al.* used a mesh structure to study the TSV-to-TSV coupling. TSV and silicon areas are divided into mesh cells with resistance, inductance, capacitance (RLC) components for intercell connections. This model can be applied to irregular TSV placement designs but it is not feasible for the full-chip extraction since there are millions of RLC components when it is applied to a large design. Larger grid size is possible, but it ignores many physical design details in the full-chip level. Kim *et al.* [3] proposed closed form formulas for two-TSV, with the skin effect and the coupling between TSV and micro bumps taken into consideration. But these models are based on TSV-pair, and lacks precision if there are many neighbor TSVs. When more TSVs are around, the electrical field (E-field) is shared and the coupling between a TSV-pair will reduce. Serafy *et al.* [4] used a model fitting method to study the geometry impact of the TSV shielding. An algorithm is proposed to find the optimum location of the shielding TSVs. However, it can only be applied to few signal TSVs since there are too many possible structure cases to fit the model in multiTSV coupling. The 2-TSV based equations ignore the E-field from other TSVs and assume a clear coupling path between TSVs thus they are overestimating the coupling of a TSV-pair especially if TSVs are placed irregularly and are close to each other. However, these techniques are fast and provide a first-order estimation if two TSVs in a pair are directly facing each other.

There are secondary effects that need to be considered for a TSV-pair. The TSV-liner-substrate forms a MOS structure which introduces a depletion region around TSV, thus it creates a depletion capacitance between TSV and substrate. Also, the

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doped silicon substrate has a finite resistance and it can serve as a discharging path when the TSV is switching. Furthermore, the E-field around TSV is distributed on all sides of TSV. Previous works such as [2] and [5] consider part of the E-field effects, but not altogether. The depletion region of the TSV is found to have nonnegligible impact on the TSV and substrate noise in [6] and [7]. Wang *et al.* [8] studied the substrate resistance and the depletion region on the TSV modeling using various nodes on the substrate as the victim. But the impact on TSV-to-TSV coupling is unknown. Therefore, a compact TSV model that considers multiple TSV-to-TSV coupling, substrate impact, and E-field effect is essential for full-chip design.

Also, there are techniques to reduce the TSV-to-TSV coupling. One way is using grounded TSVs to block the coupling path between two direct-facing TSVs. Liu *et al.* [9] inserted eight ground TSVs around the victim TSV which is shown to be effective in noise reduction. But it introduces large area overhead because of the ground TSVs and therefore, it needs a replacement and routing. Song *et al.* [10] inserted ground TSV into the empty spots in TSV farm to block the direct coupling. Other methods include adding grounded blockages around TSVs to reduce coupling. Khan *et al.* [11] added ground plugs around TSV which is area efficient but hard to manufacture because of the larger aspect ratio of the ground plugs. Cho *et al.* [12] used ground guard rings on the device and metal layer to protect the victim TSV [12]. It is effective to reduce noise for a single TSV, however, its full-chip delay, power and noise impacts are not studied. Differential signal is used for decades to improve signal transmission quality. Common-mode noise is rejected by the differential pair thus it provides better noise immunity. There are works that introduce differential TSVs in 3-D ICs. Chang *et al.* [13] used differential TSVs on a memory design. A pair of TSV is studied in [8] with victim node on the substrate. Signal slew is shown to have large impact on the victim for differential pair transmission. There are also differential TSV models based on TSV-pair assumption [14]–[16]. However, up to 5 TSVs are studied in the model and they are only focusing on the noise impact without delay and power analysis. Also, the TSV-pair based model cannot handle many TSVs in a full-chip, thus the differential TSV impacts on full-chip level are still unknown.

This paper is organized as follows. Section II presents the multiTSV model aware of neighbor TSVs and verification results. Section III presents E-field and substrate impact as well the corresponding circuit model. Section IV studies the TSV-to-TSV coupling in the full-chip level using the multiTSV model. Sections V and VI present two optimization approaches to alleviate TSV-to-TSV coupling. Section VII provides a comparison for multiple TSV-to-TSV coupling optimization techniques and Section VIII concludes this paper.

II. TSV-to-TSV Coupling Model

A. Two-TSV Model

The traditional 2-TSV model used in [9] is based on a pair of parallel wires. Fig. 1 shows the circuit components of this model. A pair of resistor and capacitor is used to model the E-field coupling between two TSVs. On the full-chip level,

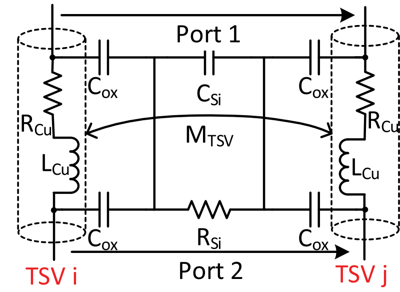


Fig. 1. Traditional circuit model of 2-TSV coupling.

the TSV-to-TSV coupling is calculated based on TSV pairs without considering impacts from neighbor TSVs.

This model assumes that there are no other object which either blocks the coupling path between TSVs or shares the E-field around. This assumption is satisfied only when there are two TSVs buried in the silicon substrate. The model is accurately matching with the measured results of a TSV-pair [17]. It is a good approximation even if the impact of devices and metal layers are considered since they affect only part of the E-field between TSVs. However, the TSV-pair assumption is no longer valid if there are other TSVs around. Those TSVs will share E-field all the way through silicon substrate. In real 3-D designs, there are many TSVs around and all of them affect the E-field distribution within that area. Ignoring the multiTSV effect, the traditional 2-TSV model overestimates the coupling between a TSV pair, and a new model which takes all the neighboring TSVs into account is desired for the full-chip analysis.

B. MultiTSV Model

From the 2-TSV model, the total coupling capacitance on victim TSV increases linearly with number of aggressor TSVs if the coupling path distances are the same for all aggressors. However, from Raphael [18] simulation results, when there are four and eight aggressor TSVs around the victim, the total coupling capacitance merely increases to 194% and 199% compared with 2-TSV case, respectively. As shown in [10], there is an upper bound of the coupling capacitance calculated by the capacitance of coaxial wire, given by the following formula:

$$C_{\max} = \frac{2\pi \varepsilon_{\mathrm{Si}} L}{\ln(P/r)} \tag{1}$$

where P and r is the outer and inner radius of the coaxial wire. In this case, r is the radius of the victim TSV and P is the minimum distance between other aggressors and the victim. According to (1), even when there are many aggressor TSVs, the total coupling capacitance cannot be more than 226% of the coupling between a TSV pair whose distance is P.

To model multiple TSVs, the multiTSV model presented in [10] is used. By assuming the aggressor TSV array as the multiconductor transmission line within silicon substrate and the victim TSV as the ground signal [19], the TSV-array inductance matrix $[L_{\mathrm{Si}}]$ is computed by applying the following formula:

$$L_{\mathrm{Si},ij} = \begin{cases} \frac{\mu_{\mathrm{Si}} L_{\mathrm{TSV}}}{\pi} \ln\left[\frac{P_{i0}}{R_{\mathrm{TSV}}+T_{\mathrm{ox}}}\right] & \text{when } i = j \\ \frac{\mu_{\mathrm{Si}} L_{\mathrm{TSV}}}{2\pi} \ln\left[\frac{P_{i0}P_{j0}}{P_{ij}(R_{\mathrm{TSV}}+T_{\mathrm{ox}})}\right] & \text{when } i \neq j \end{cases} \tag{2}$$

TABLE I
COUPLING S-PARAMETER COMPARISON BETWEEN OUR MODEL AND 3-D SOLVER. TSV DIMENSIONS IN μM AND ERROR IN dB

TSV radius	TSV height	TSV liner width	Max error
2	30	0.2	0.016
		0.5	0.011
2	60	0.2	0.017
		0.5	0.012
4	30	0.2	0.015
		0.5	0.014
4	60	0.2	0.018
		0.5	0.013

where P_{ij} is the distance between aggressor TSV i and j and the victim is labeled 0. Note in this formula, unlike the 2-TSV model, not only the distances between aggressor and the victim are considered, but also the distances between aggressor are considered. This makes it useful for any TSV placement style even when TSVs are not placed on a regular grid. By using the relation of homogeneous material between the capacitance matrix and the inductance matrix [20], the capacitance matrix for TSV array is calculated by

$$[C_{\mathrm{Si}}] = \mu_0 \varepsilon_{\mathrm{Si}} L_{\mathrm{TSV}}^2 [L_{\mathrm{Si}}]^{-1}. \tag{3}$$

Since we focus on the coupling on victim TSV, only the coupling components between aggressor TSV i and the victim is used, which is given by

$$C_{\mathrm{Si},i0} = \sum_{k=1}^{N} C_{\mathrm{Si},ik}. \tag{4}$$

Assuming a homogeneous substrate, the relationship between substrate coupling resistance and capacitance is given by

$$R_{\mathrm{Si}} C_{\mathrm{Si}} = \varepsilon_{\mathrm{Si}} / \sigma_{\mathrm{Si}}. \tag{5}$$

Note that there are also coupling paths between aggressor TSVs, which is given by $C_{\mathrm{Si},ij} (i \neq j)$. However, their impact on the victim TSV is small. This is because each aggressor is connected to a strong driving source with a full power supply (VDD) swing, which is much larger than other coupling noise. The voltage waveforms of the aggressors are not affected much by the coupling. Previous work [19] used all of the coupling components between TSVs which is not a feasible solution in full-chip level. E.g., an array of 100 TSVs leads to more than 20 000 RC components in the model. Therefore, in this paper, the coupling paths between aggressors are ignored. To verify our model, many test cases are generated containing up to 8 TSVs and transient SPICE simulations are performed. Ten layouts are generated for each sample cases. Because of the large runtime and memory space required for field solver simulation, we cannot perform simulations with dozens of TSVs. However, since the test cases mainly contain TSVs which are facing directly to each other, they represent the main contributors of the coupling capacitance and noise in the full-chip level. Model calculated using our equations is compared with extraction results from field solver in frequency domain, and the maximum error on coupling S-parameter is reported in Table I. We also perform a transient analysis in a 3-TSV case and the voltage waveform of a victim TSV is shown in Fig. 2. The results show that for all tested layouts, the coupling parameter error of our extracted model is less than 0.02 dB and we conclude our multiTSV model accurately handles multiTSV effects and is scalable with different TSV dimensions.

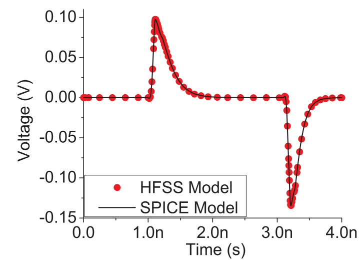


Fig. 2. Transient coupling noise analysis result verification.

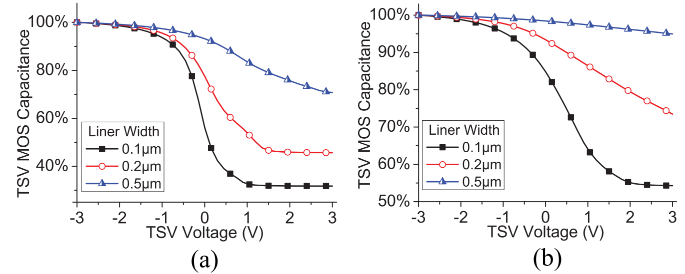


Fig. 3. TSV MOS capacitance with substrate doping of (a) $10^{15}/\mathrm{cm}^3$ and (b) $10^{16}/\mathrm{cm}^3$.

III. TSV-INDUCED SILICON AND FIELD EFFECTS

A. Impact of Silicon Depletion Region

In this section, the effect of silicon depletion region on TSV coupling is discussed. TSV, usually made of copper or tungsten, is insulated from the silicon substrate with a oxide liner, which together form a MOS structure. Due to the nonlinearity of the MOS capacitance, many previous works [9], [10] ignore the depletion region around the TSV and assume that the oxide capacitance is the only part that contributes to the TSV capacitance. Also, the simulation tool is based on field solver (HFSS [21]) which does not take silicon semiconductor effects into consideration. To study the depletion region impacts, a TSV structure is built in device simulator Synopsys Sentaurus [22]. The TSV MOS capacitance extraction result is shown in Fig. 3 with different substrate doping concentration. Copper TSV and P type substrate are assumed for our simulation. The flat band voltage is calculated by the following formula:

$$V_{\mathrm{FB}} = W_{\mathrm{Cu}}/q - \varphi_{\mathrm{Si}} - Q_s/C_{\mathrm{ox}} \tag{6}$$

where W_{Cu} (= 4.65 eV), φ_{Si}, and Q_s are work function of copper, Fermi level of the silicon, and the charges inside oxide liner, respectively. Thus, for most digital systems, when the voltage on TSV is between 0 V and VDD, a depletion region always exists around the TSV and it introduces a voltage dependent capacitance C_{dep}. While digital system usually has a clock running at several hundreds of MHz, it is safe to assume a complete depletion around TSV as in Fig. 3. This is because the substrate is slightly doped and there are not enough carriers

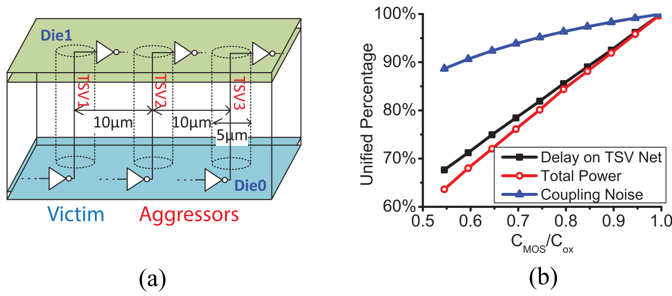


Fig. 4. (a) 3-TSV test structure for multiTSV coupling analysis. (b) Depletion region effects on TSV noise, delay, and power.

which can respond to such high signal frequency. Yi *et al.* [23] proposed a simplified close form formula to calculate the depletion width. There are other works [2], [24] using numerical method to solve partial differential equations (PDEs) and get the depletion width. Direct solution from PDEs can be more accurate than the close-form formula with simplification, but they may lose in terms of the flexibility when TSV layout changes. Therefore, to avoid convergence issue in numeric solution, we use a close-form formula in our work. After considering the depletion region, the oxide thickness T_{ox} in (2) should be replaced by $(T_{\text{ox}} + W_{\text{dep}})$.

The following equation is used to calculate TSV MOS capacitance which is the serious combination of oxide capacitance (C_{ox}) and depletion capacitance (C_{dep}):

$$C_{\text{MOS}} = \frac{C_{\text{ox}} C_{\text{dep}}}{C_{\text{ox}} + C_{\text{dep}}} = \frac{\pi \varepsilon_{\text{ox}} L_{\text{TSV}}}{\ln \dfrac{R_{\text{TSV}} + T_{\text{ox}} + W_{\text{dep}}}{R_{\text{TSV}}}}. \quad (7)$$

The TSV MOS capacitance reaches its minimum value after the silicon is strongly inverted. The MOS capacitance depends on the substrate doping and liner thickness. With a thin liner and a lightly doped substrate, the depletion region impact is more significant, especially if TSV is scaled down in the future technology node. From Fig. 3, the MOS capacitance can be as low as 36% of the oxide capacitance, thus it is overestimated if the depletion region is ignored. This results in a pessimistic estimation on TSV-induced delay and noise. Another observation is that the MOS capacitance becomes smallest when TSV voltage is tied at VDD while it reaches maximum value when TSV is grounded.

To find out how large is the depletion impact on TSV-induced delay, power and noise, a test structure with 3 TSVs is built. The structure is shown in Fig. 4(a). TSVs have 5 μm radius and 10 μm pitch. The substrate has $10^{15}/\text{cm}^3$ doping concentration. Each TSV is driven by an INVX4 and is driving an INVX4 as load. The victim TSV is driven at ground while the aggressors are switching. The switching delay and dynamic power on the aggressor TSV and the coupling noise on the victim TSV are measured in HSPICE. The HSPICE [25] simulation result on 3-TSV test structure is shown in Fig. 4(b). Since the MOS capacitance has the largest capacitance value in the coupling model, any variation of the depletion region width has a large impact on the coupling noise and timing result. Also, as the TSV-induced delay and power are directly related to the load capacitance, they almost increase linearly with the MOS capacitance. The coupling noise, on the other hand, depends not only on the MOS capacitance, but also on the coupling and load capacitance as well as driving strength. It reduces by 13% if MOS capacitance is only half of the oxide capacitance. Highly doped substrate makes it difficult for the MOS capacitor to reach the strong inversion and the maximum depletion width. Therefore, the depletion region impact is smaller and TSV-induce delay and noise are larger.

Though wide depletion region helps reducing TSV coupling noise and increasing performance, it increases the keep-out-zone (KOZ) around TSV. Devices within depletion region are observed with a threshold voltage shift and performance difference. To prevent undesired side-effects introduced by TSVs, a 1 μm KOZ is placed around our TSV and no standard cells are allowed inside to avoid the depletion region impact in our full-chip design. The KOZ is chosen since the advance of TSV fabrication technology allows transistors be placed within 2 μm region to avoid more than 10% performance variation, especially for smaller technology node [26].

B. Impact of Substrate Resistance

Since TSV is buried in doped silicon substrate, the substrate impact needs to be considered. Previous models used in [3] and [10] assume the silicon substrate is a floating net. This assumption is not appropriate since most designs ground the substrate using substrate contacts. Even though each TSV has a KOZ, there is a finite impedance from substrate around the TSV to the ground node. Whenever a victim TSV is affected by the aggressor, charges will accumulate at silicon-oxide interface. With a finite silicon impedance, the MOS capacitance can be discharged through the discharging path of the substrate. Therefore, the coupling noise on the victim TSV is reduced. Especially when the RC time constant of the discharging path is small and aggressor switching frequency is low, the accumulated charges can be quickly discharged even when the aggressor signal is still switching. Therefore, the peak noise voltage on the victim reduces due to fewer charges. The traditional model assumes a floating net at silicon substrate and therefore, overestimates the coupling noise on victim TSV since there is no discharging path. But it underestimates TSV-induce delay and power as the capacitance of the discharging path is also ignored. Therefore, the discharging path needs to be modeled using substrate resistors and capacitors. Fig. 5 illustrates our proposed multiTSV model with components to model silicon and E-field effects, where C_{Sig} and R_{Sig} represent the silicon substrate capacitance and resistance, respectively, between TSV and the substrate contact to model the charging path.

To extract the substrate resistance and capacitance, a TSV structure with grounded substrate is built. The capacitance between TSV and substrate is extracted using Synopsys Raphael and the substrate resistance is evaluated using (5). Fig. 6(a) shows the result comparison on the test structure with or without the silicon discharging path impact. The coupling noise value with 8 μm TSV pitch is used as a reference. If the substrate is assumed to be floating, the coupling noise is largest for all different TSV pitches. Smaller body resistance makes the discharging path stronger and therefore reduces

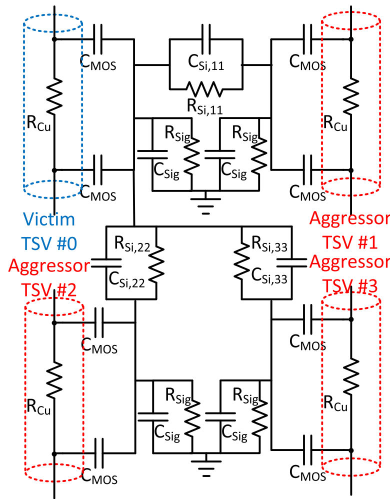


Fig. 5. MultiTSV coupling model with depletion capacitance and body resistance.

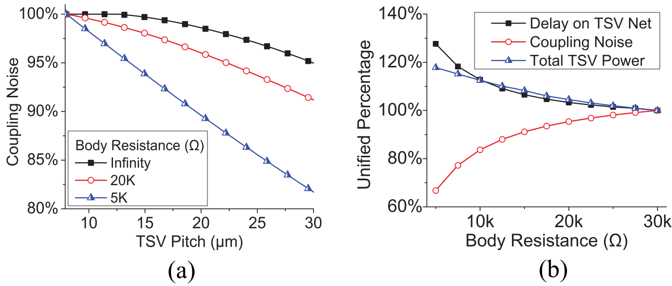


Fig. 6. (a) TSV pitch impact with body resistance. (b) Body resistance impact on delay, noise, and power.

noise more. The substrate impact is more significant with larger TSV pitch. This is because if TSV-to-TSV distance is large, the coupling capacitance between TSVs is much smaller than the TSV MOS capacitance, so any E-field sharing between TSVs has large impact on the coupling and reduces more noise. Without considering substrate discharging path, the TSV pitch is found to have a small impact on the coupling noise [9]. However, the TSV distance becomes an important factor in TSV coupling with substrate impact considered and spreading the TSVs is more effective in noise reduction if the substrate is well grounded.

A 3-TSV test structure shown in Fig. 4(a) is built to study the substrate impact on TSV-induced delay, power, and noise. HSPICE simulation results are shown in Fig. 6(b) and baseline is the simulation with 30 KΩ body resistance. With smaller body resistance, according to (5), the substrate capacitance increases. Therefore, the delay and power on TSV noise increase while the coupling noise decreases.

Previous discussions only consider the substrate resistance impact on the E-field between TSV and the substrate. Furthermore, if the actual physical geometry of the grounded active region is considered, it has impact on the E-field between TSVs as well, e.g., if a grounded active region is placed between two TSVs, it will reduce the coupling between two TSVs. This is because the active region shares some of the E-field, and part of the E-field between a TSV pair will be decoupled by the grounded region. This effect further reduces

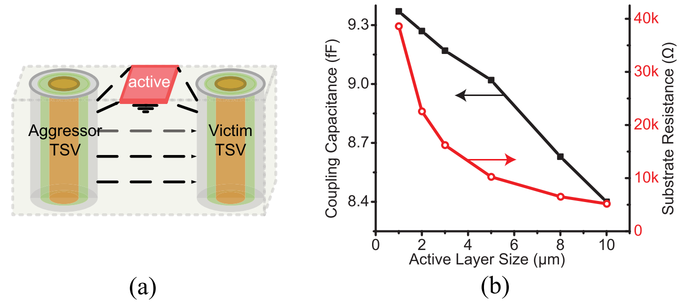


Fig. 7. (a) Two-TSV structure with grounded active layer. (b) Grounded active layout impact on TSV coupling capacitance and resistance.

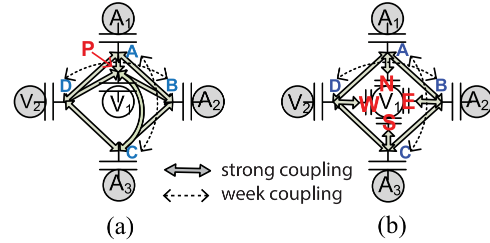
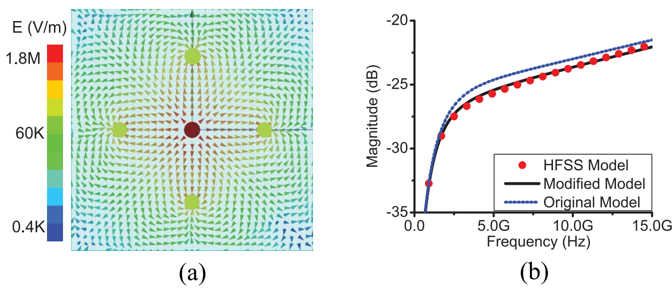


Fig. 8. Circuit model of 5-TSV case. (a) Original. (b) E-field distribution-aware model.

the crosstalk between TSVs. To study this impact, a structure with two TSVs is built. In this structure, a square grounded active region is placed between TSVs. Fig. 7 shows the structure with TSV location held constant and the extraction results from Raphael. Depending on the size of the grounded active layer and the distance between two TSVs, a maximum reduction of 9.6% and 87.1% exists in TSV coupling capacitance and body resistance, respectively. Smaller TSV coupling capacitance and larger substrate resistance indicate a weaker coupling path between TSVs. In this simulation, the TSV locations are kept the same, therefore the noise reduction comes from two aspects. Larger active region shares more E-field and leads to weaker coupling between TSV. Also, smaller distance between active layer and the TSV leads to a stronger discharging path to the ground. In general, if the victim is properly protected by the ground, it suffers less from the noise but more from the performance loss due to larger ground capacitance.

C. Impact of Electrical Field Distribution

In previous works, all of the coupling components connecting other TSVs share a single node around victim TSV which is connected to TSV net by the MOS capacitor. This model assumes that all sides of the TSV is electrically a same node. However, in real case, since the silicon substrate is not a perfect conductor, the electrical properties on different sides of the victim TSV are not the same. Moreover, the coupling between TSVs is mostly between two sides which is directly facing each other and there is few coupling on other sides. Especially in multiTSV case, where each victim TSV is facing many aggressor TSVs in multiple directions, the E-field will be shared heavily. Consider a 5-TSV case which is shown in Fig. 8, where there are 4 TSVs placed on each side of TSV V_1 and the E-field around the victim



(a) (b)

Fig. 9. (a) E-field distribution of 5-TSV case. (b) Coupling S-parameter comparison.

TSV is distributed among each aggressor. In this case, only neighbor TSVs are strongly coupled and there is only a weak coupling between TSV A_2 and TSV V_2 due to the E-field blocking effect of TSV V_1. Shown in Fig. 8, the traditional model uses a common node P to connect all the coupling path from other aggressors. This creates a direct coupling path between TSVs which are weakly coupled. With the common node P, aggressor A_2 is directly coupling with victim V_2 through path B-P-D, which results pessimistically estimation in TSV-coupling. Fig. 9(a) illustrates the HFSS simulation on E-field distribution of this structure. It is clearly seen from the plot that the coupling from each aggressor is mainly through one of the four sides of the TSV V_1, and there is fewer coupling between other sides of the victim and the aggressor because of the distributed E-field. In the traditional model, a single node is used for all sides of the TSV coupling, and it makes the coupling noise stronger since it assumes the coupling noise affects TSV on all sides at the same time. Therefore, it overestimates the coupling noise on the victim TSV.

To model the impact of the E-field distribution, four nodes around victim TSV are used to connect the coupling parameters to aggressors, shown in Fig. 8(b). Regardless of the aggressor TSV number, four nodes are used to model the coupling E-field on their facing side of the area. Therefore, the connections of the aggressor will be attached to the corresponding node to consider E-field distribution around each TSV. Similar assumptions can be found in mesh-structure based TSV model [8], [12] where four nodes are used to consider the E-field distribution. Using more nodes is possible to consider more complicated E-field distribution, but the conductance between TSV nodes needs to be considered as well. Depending on the relative location of aggressor TSVs, the coupling path will be connected using the facing node of the victim TSV. Therefore, the direct coupling path between weakly coupled TSV is eliminated in the new model. Fig. 9(b) shows the coupling parameters of the circuit model compared with the results extracted using HFSS field solver. The result indicates overall both model match well with the field solver results on the coupling noise. But there is a 1.1 dB overestimation in coupling noise due to the direct path between TSVs in the original model. Our model shows smaller errors up to 15 GHz not only in noise magnitude but also in noise phase compared with the original one. Therefore, we conclude that our model is more accurate to reflect the E-field distribution impact in TSV-to-TSV coupling.

TABLE II
INDUCTANCE IMPACT ON TSV NETS

	wo/ TSV coupling	w/ inductor	wo/ inductor
Rise delay (ps)	22.63	168.05	168.06
Fall delay (ps)	11.92	108.88	108.96
Power (μW)	3.47	21.058	21.059
Peak noise (mV)	0	27.06	27.64

IV. Full-Chip Analysis

A. Models Used for Full-Chip Analysis

In the original multiTSV model in [19], the number of components is too large to be simulated efficiently in circuit solver. Therefore, it is not a feasible solution in the full-chip level where simulation time and memory usage are big concerns. On the other hand, the widely used static timing analysis engines, such as primetime [27], reject circuits with floating nets and inductors. Moreover, they cannot output a detailed voltage waveform and assume each net is driven at a certain logic level. To be able to perform full-chip analysis, we need to simplify the full circuit model of TSV-to-TSV coupling while still maintain the model accuracy.

First, the impact of TSV inductors is studied. To precisely model TSV-coupling, the inductors are included to model the magnetic field coupling between TSVs. In high-frequency range, ignoring the inductors lead to S-parameter discrepancy because the impedance of the inductors are comparable to the resistance of the TSVs. In the meantime, the mutual inductors contribute to the coupling between TSVs, and noise will be underestimated if TSV mutual inductors are ignored. As shown in Fig. 9(b), the SPICE model can be verified against field solver up to 15 GHz which covers most analog circuit operation range. However, in a frequency range below 5 GHz, like in most digital systems, the impact of the inductors are almost negligible in terms of noise, delay and power. Within this range, the impact from capacitance and resistance dominates the coupling between TSVs. Table II lists the HSPICE simulation results on our 3-TSV test structure (shown in Fig. 4). The results indicate that the inductors can be ignored while a good estimation on TSV-induced delay, power and noise is maintained. Therefore, to reduce simulation components, the multiTSV model without TSV inductors is used in our full-chip analysis.

Second, a model which is compatible with the static timing analysis engine is proposed. Synopsys primetime is used for full-chip timing and power analysis. There is a traditional TSV-to-TSV primetime model used in [9] and [10]. This model is derived from the SPICE model but it ignores the TSV MOS capacitors (C_{MOS}) so that the floating net between TSVs are eliminated. However, it underestimates TSV-induced delay and power consumption since TSV MOS capacitor is much larger than coupling capacitor. Moreover, this model ignores the substrate impact and assumes a floating substrate. In our approach, a substrate net is added into the verilog netlist as the grounded substrate and the substrate capacitance is included. In addition, since substrate coupling capacitor is smaller by one-order magnitude compared to the TSV MOS capacitor (C_{MOS}). Therefore, it is ignored in full-chip analysis. Without the coupling capacitance, this model is not suitable for noise analysis especially in high-frequency regions where the capacitance

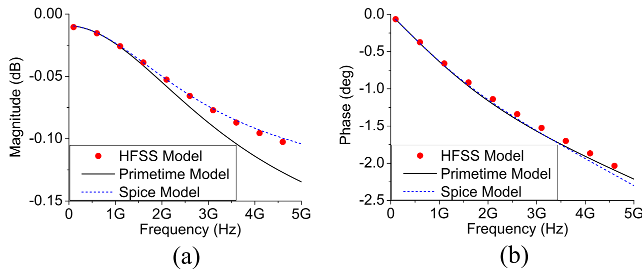


Fig. 10. Transmission S-parameter comparison. (a) shows magnitude, (b) shows phase.

TABLE III
PRIMETIME MODEL COMPARISON

Body resistance (Ω)		0	1K	5K	10K
Multi-TSV model	Power (μW)	96.47	96.32	93.64	89.65
	Timing (ps)	54.0	45.5	40.0	39.1
Without C_{Si}	Power (μW)	96.47	93.64	93.67	89.87
	Timing (ps)	54.0	45.7	39.7	38.6
Without C_{MOS}	Power (μW)	70.24			
	Timing (ps)	37.7			

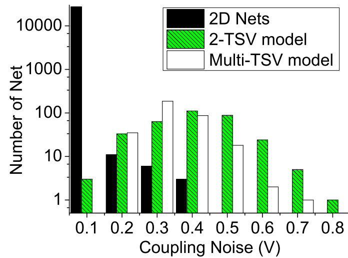


Fig. 11. Noise distribution comparison in full-chip level.

dominates the coupling. However, it can be used for delay and power analysis as they are mainly affected by low frequency response. Fig. 10 shows the transmission S-parameter comparison results up to 5 GHz. Note that the transmission S-parameter is used instead of the coupling S-parameter as this model is not used for coupling noise analysis but for delay and power estimation using primetime. HSPICE transient simulation result is shown in Table III. Since the capacitance mainly affects high frequency range, both of the results show ignoring the substrate coupling capacitor gives a good estimation of the TSV coupling and compared with the original primetime model, our modified model has a smaller error compared with the original model used in [9] and [10].

The comparison between the traditional 2-TSV model and our multiTSV model is shown in full-chip level. The same number of aggressor TSVs is assigned around a victim TSV so that different models can be compared fairly. We also consider the E-field and silicon effects and compare the total coupling capacitance and resistance values. Fig. 11 shows the noise distribution comparison between 2-TSV and multiTSV model on a 3-D design with 328 TSVs simulated. Since the 2-D parasitics are the same for both models, the noise on 2-D net is the same. As shown from the results, by using the 2-TSV model, the TSV net noise is much larger than that using multiTSV model. One reason is the 2-TSV model overestimates the coupling capacitance between TSVs, and another is because it ignores the depletion, substrate and E-field distribution impact.

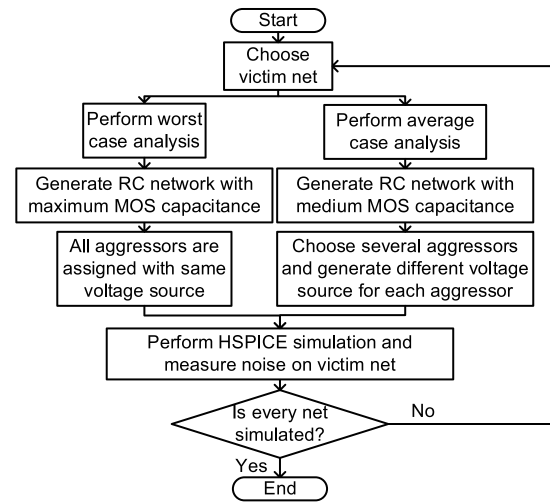


Fig. 12. Full-chip noise analysis flow.

Since our design is operating at 200 MHz, TSV MOS capacitor dominates the coupling between TSVs within this range. However, using the 2-TSV model gives a total TSV net noise of 139.4 V, which is 48.0% larger than total noise measured (94.2 V) using our multiTSV model.

B. Full-Chip Analysis Strategies and Flow

For full-chip analysis, we first extract TSV locations and 2-D parasitics for each die separately from Cadence Encounter. Then a RC parasitic network is generated for all the TSVs using our multiTSV model. The flow reported in [10] and [28] is updated, where TSV capacitance is calculated on one TSV after another. However, since the calculation of multiTSV model gives the coupling capacitance between all TSV pairs, the runtime spent on TSV coupling capacitance calculation can be saved by using all the coupling information. In our flow, all TSVs are considered at the same time thus every coupling capacitor is computed in a single run. For our design with 330 TSVs, the original flow uses more than 13 s, while our flow takes less than 2 s on a XEON-E5 CPU. Note that if the number of TSV considered is the same, each calculation flow produces the same results for TSV coupling capacitance. Our calculation flow has a great speedup compared with the traditional flow.

After the TSV coupling model is calculated, SPICE netlists as well as a top-level standard parasitic exchange format file are generated containing TSV parasitic information. For full-chip noise analysis, HSPICE simulation is performed and the coupling noises on victim nets are extracted. Different from the flow reported in [9] and [10], where the noises are measured at every nodes on a single net, and the coupling noise voltages are added all into the total noise. Thus, the total noise measured is several times larger than it should be. In our flow, only the maximum noise appears on a single net is measured so that the noise value is not counted many times. This procedure is performed on every TSV net in the design and the sum of maximum noise on all TSVs is used as the total noise. Fig. 12 shows our noise analysis flow. Primetime is used to read the parasitic information for each die as well as TSV coupling

TABLE IV
WORST CASE AND AVERAGE CASE COMPARISON

	Worst case	Average case
Time window	Clock period	$\leq$ Clock period
Start time	Fixed	Randomly chosen
Aggressor activity	1	0 to 1
Switching direction	Rise	Rise and fall
Noise definition	Maximum voltage	Peak-to-peak voltage

information altogether and then perform full-chip static timing and power analysis.

Since TSV parasitics are depended on TSV voltage, and it is difficult to estimate the signal arriving time for all possible cases, different strategies are used for worst case and average case analysis. For worst case analysis, it is assumed that all the aggressive signals are arrived at the same time and they all have the same switching waveform from 0 V to VDD. In this case, charges due to TSV coupling accumulate around the victim TSV and introduce a large voltage spike at the victim node. Then, the maximum voltage on the victim net is measured. Note it is only theoretically possible that all aggressors have the same waveform and the victim would see such a large noise, however, it is a good indicator of how severe is the coupling in the full-chip level and the result is only related to the design itself. We use TSV MOS capacitance measured when the TSV voltage is 0 V since the depletion region width is minimum and TSVs are strongly coupled through the substrate.

For average case study, a time window is chosen which is no larger than the target clock period. We use the TSV MOS capacitance values measured at half of the VDD. Moreover, some aggressors may not even switch during the same clock cycle. Since not all aggressor nets are switching at the same time, the arrive times of the aggressor signals are randomly located within the time window. A switching activity factor which is less than 1 is used to determine the possibility of signal switching. Note in worst case analysis, since all of the aggressors are switching, therefore, the switching factor is 1. Also, different from worst case analysis where all the signals are switching in the same direction, aggressor signals may rise or fall in our average case analysis. Therefore, after running HSPICE, the peak-to-peak voltage difference on the victim TSV net is measured as the noise value. Table IV lists the comparisons between worst case and average case analysis, and Fig. 13 shows the victim voltage waveform in different cases. The limitation of this method is, without static timing analysis on all possible input patterns and every timing path, this method cannot simulate the exact value of the noise under various input patterns. Instead, it provides an overview of the total TSV noise in full-chip scale. Therefore, if detailed signal integrity analysis is needed for each signal, combining static timing analysis engine with our multiTSV model can solve this problem. The static timing analysis engine provides detailed signal waveform which includes arriving time and slew for every time path while our model computes the noise and delay on TSV net. Also, the detailed layout of the substrate contacts is not considered and a uniformed discharging path is assumed for the silicon substrate. This assumption is valid since the standard cell placement density is close to 60% everywhere in our design, therefore the substrate contact density is almost the same around each TSV. Pattern-matching algorithm may be used to extract the substrate parasitics and detailed discharging path can be built for each individual TSV.

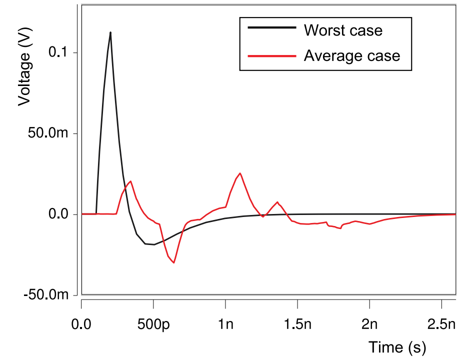


Fig. 13. Transient analysis of victim voltage.

TABLE V
DESIGN SPECIFICATIONS

Placement style	Irregular	Regular
Minimum TSV pitch (μm)	12	19
Footprint	$380\mu m \times 380\mu m$	
TSV count	330	
TSV area (μm^2)	16170	

C. Designs Specification

A 64 point fast Fourier transform (FFT) design is used to demonstrate the full-chip impact of TSV-to-TSV coupling. It has 47 K gates and 330 TSVs. The target clock frequency is 200 MHz. We implement this design on a 2-die 3-D IC using 45 nm technology with five metal layers. The TSV landing pad size is 5 μm and TSV radius is 2 μm. The TSV liner thickness is 0.5 μm. Each TSV has a 1 μm KOZ to ensure all the logic cells are outside of the TSV depletion region so that their threshold voltage and performance will not be affected by the depleted substrate. The total footprint area of the design is 380 $\times$380 μm, and the total TSV area is 16170 μm^2, which is 11.2% of the total area. Table V shows the detailed design information. A in-house 3-D placer [29] is used to obtain the final placement and Cadence Encounter is used to refine placement and route the design. We apply different TSV placement strategies and obtain two kinds of designs. During regular placement, TSVs are placed on regular grid with a pitch of 20 μm. TSVs are distributed all over the design space and TSV placement density is about the same everywhere. For irregular placement, TSVs are treated the same way as other logic cells and try to minimize the total wirelength. The minimum TSV-to-TSV pitch in irregular placement is 11 μm so that it can be manufactured. Fig. 14 shows the die shots with TSV landing pads are highlighted. Though a small digital design is used for full-chip analysis, the TSV placement density is similar to TSV farms in a large design. For those designs, the layout can be partitioned into zones so that each zone can be extracted and simulated efficiently. Thus, our method can be extended to 3-D IC designs with large footprint without sacrificing the efficiently.

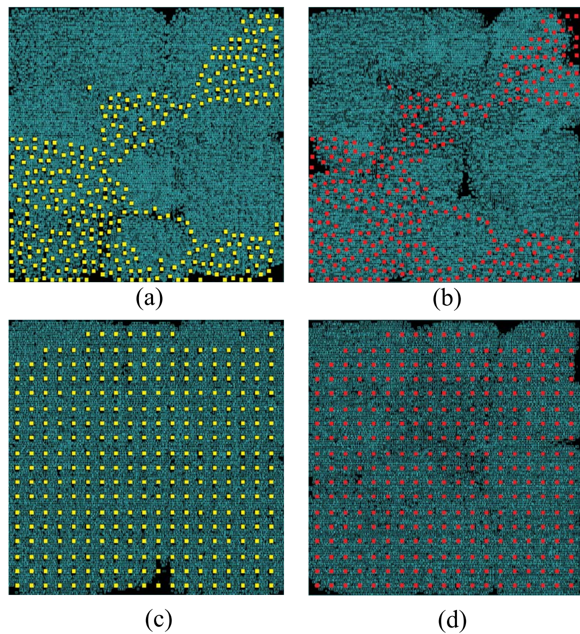


Fig. 14. Design layout. (a) Bottom and (b) top die of irregular placement design. (c) Bottom and (d) top die of regular placement design.

D. Worst Case Analysis Versus Average Case Analysis

From Fig. 11, the largest coupling noise is measured on the TSV net rather than 2-D nets and the average noise value on TSVs is much larger than that of 2-D nets. Also, compared with 2-D nets, 3-D TSV nets heavily suffer from coupling noise and delay. This is because of the following reasons.

1) It is difficult for current technology to fabricate TSVs with very small dimensions and large aspect ratio. Therefore, TSV has large MOS capacitance due to long shape and large radius.
2) In future technology nodes, more TSVs and higher TSV placement density are allowed to increase die-to-die bandwidth, therefore there will be larger coupling between TSVs.
3) The permittivity of the interlayer dielectric (ILD) between 2-D interconnections is very low if low-K material is used ($2\sim3\varepsilon_0$).

However, the silicon substrate that is covering around the TSV has a very high permittivity ($11.9\varepsilon_0$), which results in large TSV coupling capacitance. However, this can be alleviated by using fully depleted silicon on insulator (FD-SOI) technology.

The average case analysis flow described in Section IV-B is used for TSV-to-TSV coupling noise study. In average case, the victim TSV has much smaller peak-to-peak noise due to the following reasons.

1) Not all the aggressors switch in one clock period, and those switching aggressors do not start voltage transition at the same time. Smaller aggressor signal activity results in smaller coupling noise on victim TSV.
2) Due to the load capacitance, many aggressor nets have longer transition time, especially for nets with weak driver.

TABLE VI
AVERAGE CASE AND WORST CASE COMPARISON ON TOTAL TSV NET NOISE (V)

	Activity	Slew (ns)	Irregular	Regular
	0.2	0.1	26.51	24.65
Average case	0.5	0.1	39.61	35.37
	0.2	0.5	14.04	14.62
Worst case	1.0	0.1	139.01	132.44

Slower transition time on aggressor introduces fewer charges through the coupling path thus it reduces the coupling noise on victim TSV. Table VI compares the two analysis in various metrics. In all cases, the average case shows much smaller total TSV coupling noise than the worst case. The average case analysis provides an estimation on average noise level on TSV nets when multiple aggressors with different voltage waveforms are considered. The results show that both the switching activity and the signal slew have a large impact on the noise results on the TSV nets. Larger switching activity and smaller signal slew increase the TSV coupling noise significantly and they should be considered in noise analysis.

Moreover, compared with regular placement design, irregular placement design is showing 5% larger coupling noise. This is because, in irregular placement design, minimum distance between TSVs is smaller, and TSVs are placed with higher density. Therefore, irregular placement suffers more TSV coupling that results in a larger timing degradation. However, since the regular placement is a special case of irregular placement, it is possible to find a better irregular TSV placement which has smaller noise coupling.

E. Full-Chip Substrate and Field Impact

To study the impact of field and substrate effects, we disable each field and silicon effect one by one while keeping other effects the same and perform noise analysis on the full-chip level. The worst case analysis flow is used because the average case analysis flow is random choice based and gives different results for each run. However, the worst case analysis result only depends on the circuit itself which makes it a fair comparison. Table VII details chip-level E-field and silicon effects comparison. Without considering the depletion region, TSV MOS capacitance is overestimated, especially when TSV liner thickness is thin and the substrate doping concentration is low. Since our design runs at 200 MHz, a complete depletion around TSV is assumed. If depletion region is ignored, the result show a 10.5% and 10.2% increase in total TSV net noise for irregular and regular design, respectively. This is because the MOS capacitance is overestimated by 17%. Moreover, ignoring substrate resistors and capacitors is also a pessimistic estimation on coupling noise. The discharging path through a substrate is critical to limit the peak noise on the victim and it also affects delay and power consumption. Also, without considering the electrical field distribution, the noise is over-estimated because every aggressor sees the whole TSV MOS capacitance around victim TSV, even though it only faces to one side of the victim TSV. Since the electrical field distribution effects does

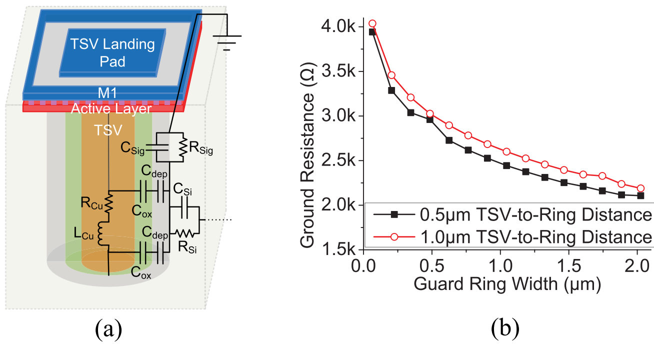


Fig. 15. (a) Guard ring model. (b) Guard ring impact on substrate ground resistance.

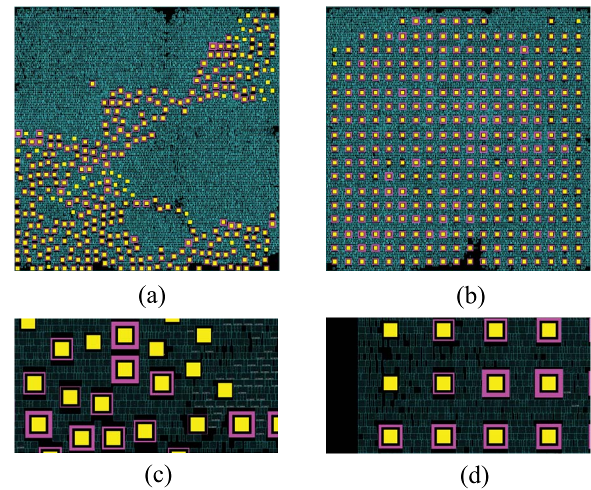


Fig. 16. Noise-optimized design layout. Bottom dies of (a) irregular and (b) regular placement design. (c) and (d) Zoomed-in view shots.

not change any capacitance value, the calculated delay and power is the same using primetime. Overall, the depletion region impact has the largest impact on full-chip metrics as the MOS capacitance is the dominating component in TSV-to-TSV coupling.

V. TSV-to-TSV Coupling Noise Reduction Using Guard Ring

A. Guard Ring Model

Since the silicon substrate provides a discharging path to the ground, it can be used to reduce the coupling noise on TSVs by making the discharging easier and reducing substrate-to-ground resistors (R_{Sig}). We use a grounded guard ring proposed in [12] in the active layer with P+ doping to build a short discharging path for the victim TSV. The ring is connected with grounded rings in Metal1. Therefore, the TSV is protected by ground ring in active layer and landing pad is protected by ring on Metal1. In [12], the guard ring is divided into many cells, and each cell contains 6 to 12 components. This model uses too many components which makes it unsuitable for full-chip analysis. To reduce the model complexity, we propose a new guard ring model with few added components to multiTSV model. The proposed guard ring structure is shown in Fig. 15(a). The discharging path through the grounded ring contains two components C_{Sig} and R_{Sig}, and we use Synopsys Raphael to extract the substrate capacitance to the ground. Detailed extraction results are listed in Fig. 15(b), with various edge-to-edge distance and guard ring width. Small ground resistance leads to a strong connection between the substrate and the ground net, thus it can help shielding coupling noise introduced by TSV-to-TSV coupling. The ring width shows a large impact on the ground resistance. Thus, the coupling noise reduces further if the width of the guard ring is increased. However, the distance between TSVs and the guard ring does not affect much on the ground resistance. Longer edge-to-edge distance between TSV and guard ring results in a larger guard ring but the coupling E-field strength is reduced. The drawbacks of this method include a slight timing degradation on TSV nets due to the increased ground capacitance and a small area overhead. Wider guard ring shows larger noise reduction but they introduce longer delay. On other hand, while the silicon around TSV is depleted and cannot be used for devices, the guard ring in the active area can make use of this area and help reducing noise. This makes the guard ring more appropriate for designs with large KOZ and increase the silicon utilization. Transient analysis is performed on the 3-TSV test structure with our multiTSV model and the guard ring shows 47.5% noise reduction on victim TSV net.

B. Optimization Flow and Results

Liu *et al.* [9] proposed a TSV shielding technique. The coupling path impedance between TSVs is used to select which TSV should be protected. However, the coupling path impedance is not a good indication of coupling noise because of the following reasons.

1) Not only neighbor TSVs, but also the 2-D nets are aggressors for a victim TSV. Using only coupling between TSVs cannot reflect the coupling from 2-D aggressors.
2) TSV coupling path impedance and the coupling noise is not in a linear relationship.
3) The number of coupling neighbors also affects the noise value.

Therefore, to efficiently find TSVs which need noise protection, the following strategy is utilized to perform the noise optimization. First, a worst case noise analysis is performed on the full-chip design and obtain the noise levels on each TSV. Then, the TSVs are sorted according to the noise levels and guard rings with different widths are added around TSVs. To minimize the area overhead, a minimum noise threshold is used below which no guard ring will be added. Above the threshold, TSVs that suffer larger coupling noise is protected with a wider guard ring and vice versa. Worst case analysis is used here as it is not random seed dependent. Fig. 16 shows the layout with TSV and guard ring highlighted after the optimization is performed on our regular placement and irregular placement designs. Shown in the layout, TSVs with large coupling noise are mostly located in the center of the

TABLE VII
SILICON AND E-FIELD IMPACTS ON TOTAL TSV NET NOISE (V), TSV-INDUCED DELAY (NS), AND POWER (μW) INCREASE

Placement style	Irregular			Regular		
	Total TSV noise	TSV-induced Delay	TSV Net Power	Total TSV noise	TSV-induced Delay	TSV Net Power
no depletion region	153.7 (+10.5%)	0.85 (+7.6%)	13.53 (+6.7%)	145.9 (+10.2%)	0.98 (+7.7%)	13.66 (+7.0%)
no body resistance	144.9 (+4.2%)	0.78 (-1.2%)	12.54 (-1.1%)	138.9 (+4.9%)	0.90 (-1.1%)	12.63 (-1.1%)
no E-field distribution	146.3 (+5.2%)	0.79 (0%)	12.68 (0%)	138.9 (+4.9%)	0.91 (0%)	12.77 (0%)
all-effects-included	139.0	0.79	12.68	132.4	0.91	12.77

TABLE VIII
FULL-CHIP COUPLING OPTIMIZATION RESULTS OF TWO DESIGN STYLES

Placement style	Irregular	Regular
Total TSV noise without guard ring (V)	139.0	132.4
Total TSV noise with guard ring (V)	101.1	96.5
Noise reduction	27.3%	27.1%
TSV-induced delay (ns)	0.81	0.93
TSV-induced power (μW)	12.75	12.86

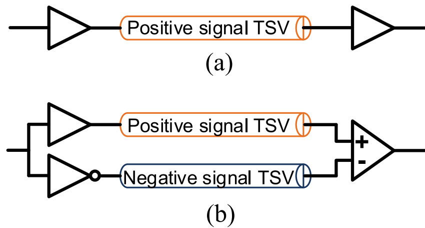


Fig. 17. Signal transmission using TSV. (a) Single-ended. (b) Differential pair.

die where TSVs are surrounded by more aggressor TSVs as well as standard cells.

After the guard rings are added to the design, the overlapping in the layout is fixed using incremental placement and routing and then perform worst case analysis on the new layout. Table VIII shows the noise optimization results. There is a 27.3% reduction in total TSV net noise with only 7.65% area overhead from guard rings. The delay of the design also increases a little due to the increased substrate ground capacitance. Our results show that guard ring protection is very effective in TSV noise reduction with minimum area overhead.

VI. TSV-TO-TSV COUPLING NOISE REDUCTION USING DIFFERENTIAL TSV PAIR

A. *Differential TSV Impact on Modeling*

Another method to enhance the signal transmission reliability is using differential TSV pairs. Fig. 17 compares the single-end TSV and the differential TSV transmission. In differential TSV transmission case, voltages on a pair of TSVs are compared and the difference is used to determine the output level. There are differential TSV models proposed in [14], [15], and [23]. These models analyze a pair of differential TSV with grounded TSV nearby. The model matches the measurement result, however, they ignore the coupling from other TSVs and the E-field distribution. Also, in many 3-D ICs, signal TSVs are often placed in TSV farms where there is no power/ground TSV around. Therefore, to analyze the full-chip impact of differential TSV, our multiTSV model is used in the following discussion.

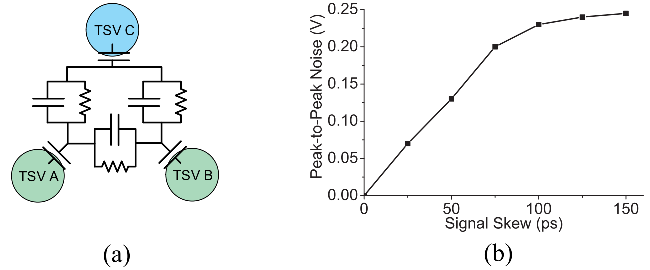


Fig. 18. (a) 3-TSV coupling case. (b) Signal skew impact on noise when the differential pair is aggressor.

A test case with 3-TSV is shown in Fig. 18(a). TSV A and B form a differential pair and TSV C is a single-end TSV. Each TSV is driven with a signal slew of 0.1 ns and an INVX4 as load. If TSV A and B are aggressors and TSV C is a victim, when one of the aggressors is switching, the noise voltage on victim is 0.16 V. And if both aggressors are switching with the same waveform, the noise on victim C is almost doubled to 0.31 V. However, if TSV A and B form a differential pair and their signals are perfectly symmetric in ideal case, there is no noise on the victim since the aggressive signals cancel each other. Even in real cases when there are unsymmetrical factors due to signal skew and process variation, and the differential signals are not perfectly synchronized, the noise can still be smaller than single-end TSV coupling. The signal skew impact is shown in Fig. 18(b) when the differential pair is the aggressor, and the noise voltages are measured in peak-to-peak swing. For differential signal, once the signal skew is larger than the input transition time (0.1 ns), there is no benefit on the victim noise level since the aggressive signals can be treated as two individual signals in those cases. The unsymmetrical location between the victim and the differential pair does not heavily affect the coupling noise on the victim. This is because according to (5), the RC time constant between TSVs is the same. Thus, the signal arrive time from TSV A and TSV B will be similar if the signal input skew is small. In our 45 nm technology, the signal skew between a INVX4 and BUFX4 is 16.4 ps without load capacitance and is 4.9 ps with 50 fF load capacitance. Therefore, differential TSV can effectively reduce the TSV coupling noise.

On the other hand, the differential TSV transmission improves the noise immunity and reliability. Consider the case when TSV C is the aggressor, and TSV A and B are victims. Since the voltage is compared at the end of the differential pair and the common-mode noise is assumed to be perfectly rejected by the comparator, the absolute value of the voltage subtraction is used as the noise. HSPICE simulation is performed with our multiTSV model. Fig. 19 shows the

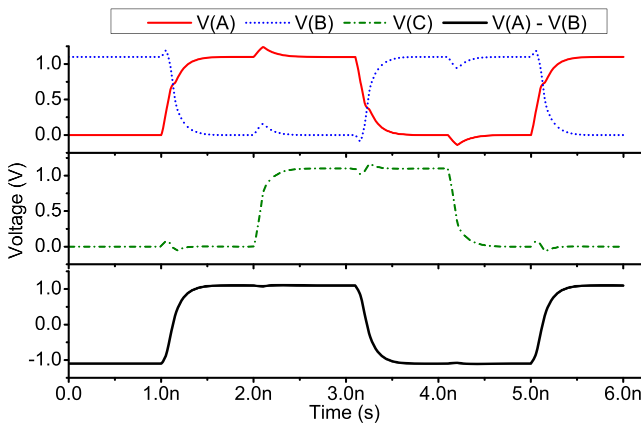


Fig. 19. Hspice simulation of 3-TSV coupling case.

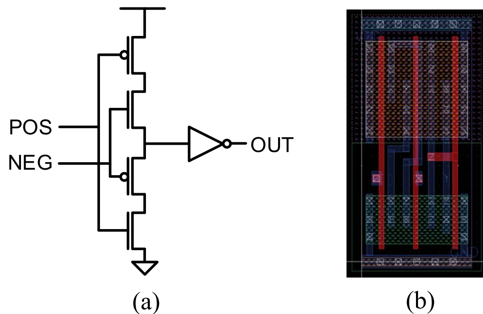


Fig. 20. Digital comparator design. (a) Schematic. (b) Layout in 45 nm technology.

voltage waveform. Even though each TSV still sees a 0.16 V voltage noise on its waveform, the subtraction voltage perfectly rejects the coupling noise. Also, the subtraction voltage has a swing of two times of VDD, which gives more room for signal detection. Note that TSV is used as the aggressor in this analysis, same strategy can be applied for noise reduction when the aggressor is a 2-D net.

B. Full-Chip Optimization Flow and Analysis With Differential TSVs

For full-chip implementation, a simple digital comparator proposed in [30] is used. Fig. 20 shows the circuit and the layout. Our comparator (COMPX4) is designed using the same footprint and output transistor width as a BUFX4. For regular design, similar as in Section V, the worst case noise analysis results from original design is used to set a noise threshold. TSVs with noise above the threshold will be replaced by differential TSV pairs. However, for irregular design, since TSVs are placed closer, it is possible that when a single TSV is replaced by a differential pair, the inserted TSV overlaps with existing TSVs. Therefore, for irregular design, starting from the TSV with largest noise, we try to replace TSVs with differential pair, unless the new inserted TSV will cause overlapping in the layout. Compared with regular design, a slightly lower noise threshold is used if same number of TSVs are protected. After the differential TSV insertion, a refine placement is performed to fix TSV overlapping with standard cells and to insert new cells such as comparators. Then incremental routing is performed so that no major redesign is needed when

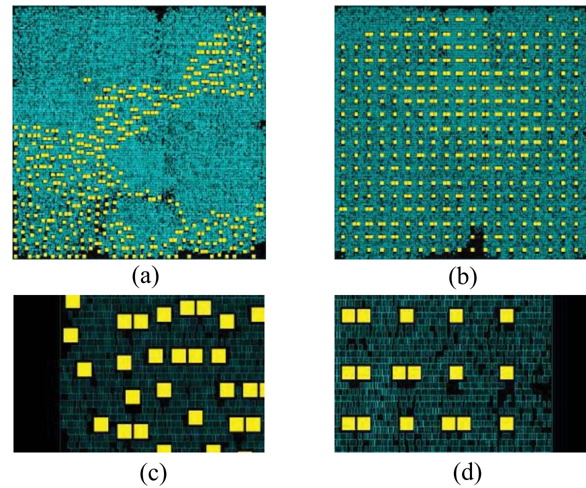


Fig. 21. Design optimization with differential TSVs. Layouts of (a) irregular and (b) regular design. (c) and (d) Zoomed-in view shots.

TABLE IX
FULL-CHIP IMPACT OF DIFFERENTIAL TSVS

Design style	Irregular		Regular	
With differential TSV?	no	yes	no	yes
Protected TSV#	0	100	0	100
Area increase	-	3.4%	-	3.4%
LPD (ns)	4.62	4.64	4.36	5.02
Total TSV noise (V)	139.0	76.5	132.4	83.1
TSV noise reduction	-	44.9%	-	37.2%
Total TSV coupling cap (pF)	4.32	8.10	3.27	6.33
Total TSV MOS cap (pF)	21.9	28.5	21.9	28.5

applying the differential TSV insertion. Note the differential TSV pair impact comes from two aspects. Once a victim TSV is replaced by a differential pair, it has better noise immunity. On the other hand, when other TSV is considered as the victim, the coupling noise from each member of the differential pair cancels each other and it results in a smaller noise on the victim TSV. To consider both effects, full-chip analysis flow needs to be modified for differential-TSV-awareness.

To perform the full-chip noise analysis, the worst case flow in Section IV-B is modified to consider the differential TSV impact. First, differential pair is divided into positive TSV and negative TSV where positive TSV has the same voltage switching direction as other aggressors and the negative TSV has the opposite switching direction. Moreover, for differential TSV pair, noises are compared at the both TSVs and the absolute value of voltage subtraction is taken as the noise of a differential pair of TSVs rather than the peak-to-peak voltage in single-end TSV case. Layouts of designs with differential TSV pairs are shown in Fig. 21 and full-chip analysis results are shown in Table IX. For the regular design, the TSV on the critical path is replaced by a differential pair so there is a small increase in the longest path delay due to slower comparators and longer signal transition time. However, for the irregular design, such TSV is not protected. Therefore, only minor change exists on the longest path delay. From the results, we conclude that differential TSV transmission is very efficient in TSV coupling noise reduction with a small overhead in timing and area.

TABLE X
FULL-CHIP ANALYSIS COMPARISON WITH GUARD RING VERSUS TSV SHIELDING

	TSV shielding in [9]	Guard ring protection	Differential TSV insertion
Base design	FIR	FFT	FFT
Protected TSV #	118	298	110
Initial TSV size (μm^2)	49	49	49
Protected TSV size (μm^2)	361	68.89 ~ 121	105
Initial footprint	$402\mu m \times 402\mu m$	$380\mu m \times 380\mu m$	$380\mu m \times 380\mu m$
Final footprint	$421\mu m \times 421\mu m$	$380\mu m \times 380\mu m$	$380\mu m \times 380\mu m$
Noise reduction	42.04%	27.3%	49.2%
Area overhead (μm^2)	42598 (26.4%)	11053 (7.65%)	4900 (3.9%)

VII. TSV NOISE OPTIMIZATION METHOD COMPARISON

In this section, we compare different full-chip TSV noise optimization method including ground TSV insertion (TSV shielding [9]), guard ring protection and differential TSV pair insertion. Table X shows the detailed comparison. TSV shielding method uses a FIR design while our methods use a FFT design. TSV shielding is very effective in TSV-to-TSV noise reduction, but there are major drawbacks for this technique.

1) It requires large additional area for ground TSVs, and for every TSV protected, eight additional TSVs are inserted which results in a large area overhead.
2) TSV shielding needs to enlarge the footprint area and perform a redesign to achieve good noise reduction. Thus, it requires more design time compared with guard rings which is easier to implement.
3) The ground TSVs also introduce a large capacitance to the victim TSVs, which will cause delay increase on paths through the protected TSV.

As the worst case noise is used to find out TSVs which are heavily affected by the coupling, the coupling direction is not considered. Thus, we assume the victim TSV needs to be protected on all sides. Song *et al.* [10] used fewer grounded TSVs inside the TSV farm. This leads to smaller impact on timing and power in the full-chip level, but the noise reduction is also compromised. On the other hand, guard ring protection introduces smallest overhead to the design since no additional TSVs are required and minimum changes are needed for full-chip optimization. Thus, it is a cost-effective method. However, the noise reduction percentage is also smallest among all of the techniques. The differential TSV insertion introduces small area increase but relatively larger longest path delay increase due to the comparator. Their noise reduction percentage is also large thanks to the differential signal transmission. One benefit from guard ring protection and differential pair TSV insertion is that no refloorplan is needed if the placement is not heavily congested, which saves a lot of design time and efforts. Overall, our conclusion is, for TSVs on the critical path, guard ring protection is the best solution with minimum delay overhead. For other TSVs, differential TSV is a good choice to minimize area overhead and TSV shielding can be applied on TSVs which needs full protection on every side.

VIII. CONCLUSION

In this paper, we studied the TSV-to-TSV coupling and its impact on 3-D IC. We proposed a compact multiTSV model that can be applied to full-chip TSV-to-TSV coupling analysis that considers E-field and substrate effects. Our multiTSV model was shown to be highly accurate compared with 3-D field solver. Depletion region, substrate impedance, and E-field distribution effects were found to be critical in TSV modeling. We proposed worst case and average case analysis methods and full-chip analysis showed that TSV-to-TSV coupling has large impact on full-chip timing and noise. To alleviate the TSV-to-TSV coupling noise, we proposed a novel guard-ring model and an optimization method to protect the victim TSVs by grounded active region. Our analysis results showed that this optimization method can reduce the coupling noise up to 27.3% with the maximum area overhead by only 7.65%. Also, with differential TSV insertion, the total TSV noise can reduce up to 49.6% with only 3.9% area overhead. Results showed that our optimization method is very effective, easy to implement and area efficient.

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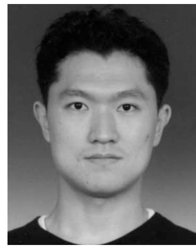

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