Fast and Accurate Full-chip Extraction and Optimization of TSV-to-Wire Coupling

Yarui Peng[1] Dusan Petranovic[2], and Sung Kyu Lim[1]
[1]School of ECE, Georgia Institute of Technology, Atlanta, GA, USA
[2]Mentor Graphics, Fremont, CA, USA
yarui.peng@gatech.edu, limsk@ece.gatech.edu

ABSTRACT

In this paper, for the first time, we model and extract the parasitic capacitance between TSVs and their surrounding wires in 3D IC. For a fast and accurate full-chip extraction, we propose a pattern-matching-based algorithm that considers the physical dimensions of TSVs and neighboring wires and captures their field interactions. Our extraction method is accurate within 1.9% average error for a full-chip-level design while requiring negligible runtime and memory compared with a field solver. We also observe that TSV-to-wire capacitance has a significant impact on the noise of TSV-based connections and the longest path delay. To reduce TSV-to-wire coupling, we present two full-chip optimization methods, i.e., increasing KOZ and guard ring protection that are shown to be highly effective in noise reduction with minimal overhead.

Categories and Subject Descriptors

B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids

General Terms

Design

Keywords

3D IC, TSV-to-Wire, Coupling

1. INTRODUCTION

Through-silicon-via (TSV) is widely used for vertical interconnection in 3D IC. TSV parasitics usually increase path delay and switching power. Figure 1 shows our 3D IC structure where two dies are bonded in face-to-back fashion with via-first technology [4]. The capacitance in red shows the capacitance between TSV and nearest wire layer and TSV-to-wire capacitance is usually larger than wire-to-wire capacitance because of the following reasons. First, TSV has a large coupling influence zone since TSVs are very tall. For regular wire-to-wire coupling, the electrical field (E-field) is often blocked by other wires. However, for the top metal layer, there are no other blockages between TSV and wires, and hence the largest TSV-to-wire coupling capacitance will occur in this region. Second, compared with a low-K dielectric material (about 3F/m in permittivity), the silicon substrate has a much larger permittivity (11.9F/m). TSV parasitics in 3D IC are not fully extracted using current parasitic extraction tools, but only wire-to-wire capacitance for each die are extracted separately.

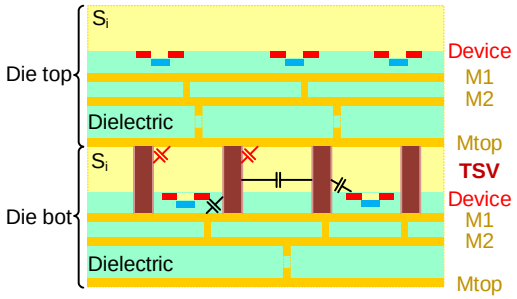

Figure 1: Structure of 3D IC with 2 dies, the capacitance in red is the TSV-to-wire capacitance extracted in this work.

Tools like StarRC and Calibre xRC can extract TSV-to-TSV coupling, but TSV-to-wire capacitance is ignored. In addition, TSVs are often used as interconnecting components in silicon interposer, the capacitance between TSV, microbumps and redistribution layer (RDL) needs to be considered in packaging level as well. The parasitic extraction using a field solver can handle small designs, but this requires huge computing resources and runtime, which is not feasible for full-chip design. Therefore, a fast and accurate TSV-to-wire capacitance extraction tool is desired for both layout optimization and accurate analysis of timing, power, and signal integrity.

Some previous works investigated TSV-to-TSV coupling parasitics [1, 7], but none of these studied the TSV-to-wire coupling. TSV with RDL connection is studied in [3], but TSV-to-RDL coupling capacitance is ignored. TSV-to-wire parasitic extraction using a field solver is discussed in [6] and the authors concluded that TSV-to-wire capacitance is not negligible for TSVs with low aspect ratio. The equation based TSV-to-wire coupling extraction is discussed in [2], which is accurate in simple layouts. However, there is no full-chip-level result provided at the full-chip level. Additionally, these equations only consider one TSV-wire pair at a time without E-field sharing and neighbors' influence.

The contributions of this paper are as follows: (1) We investigate the E-field sharing effects on TSV-to-wire coupling model; (2) We develop a fast and accurate pattern-matching method for mul-

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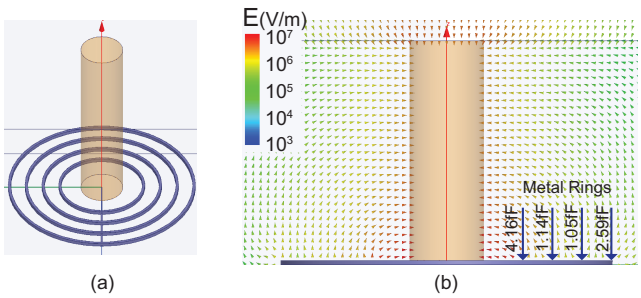

Figure 2: Multi-wires effects. (a) TSV-ring structure. (b) E-field distribution around TSV.

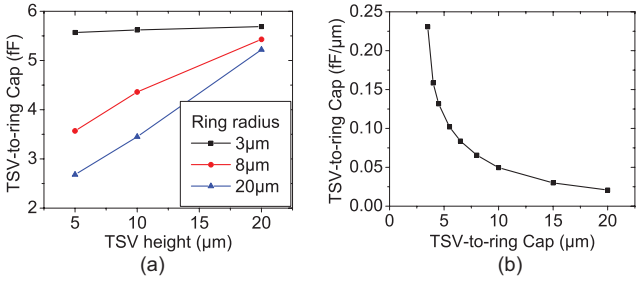

Figure 3: TSV influence region. (a) TSV height impact. (b) TSV-to-wire distance impact.

tiple wires; (3) We perform timing, power, and noise analysis on full-chip level and study the TSV-to-wire coupling impact; (4) We implement two optimization methods, i.e., Keep-Out-Zone increasing and guard ring protection. To the best of our knowledge, this is the first work where TSV-to-wire coupling capacitance is extracted in full-chip scale.

2. MODELING OF E-FIELD SHARING

2.1 TSV Influence Region

Since the capacitance is geometry dependent, the dimension of TSVs and wires affects their coupling capacitance. In addition, TSV size and the relative distance between TSV and wire determine the TSV influence region, beyond which the TSV-to-wire coupling capacitance is ignored. We use a structure shown in Figure 2(a) to study the TSV influence region. We use metal rings so that the TSV-to-wire distance is kept the same for all parts of a wire ring. To study TSV influence region, we consider a structure with a single TSV and a single wire ring. As shown in Figure 3(a), a short TSV does not affect far away wires much, but a tall TSV does. Figure 3(b) shows the relation between coupling capacitance and TSV-to-wire distance as well. The TSV is 15μm in height and 2.5μm in radius. TSV-to-wire coupling is majorly within 10μm distance and wires located farther than 20μm from TSV show negligible coupling capacitance. Therefore, we use 20μm as an extraction distance threshold (TSV influence region) to build our libraries.

2.2 Effect of Multiple Wires

Traditional models only consider one pair of TSV and wire at one time. However, if multiple wires are located around TSV, the E-field will be shared among the wires. Traditional modeling method overestimates the capacitance as no neighbors are considered. Figure 2(b) shows the E-field distribution simulated using a field solver (HFSS) when four wires are considered. The E-field between the nearest neighbor and TSV is the strongest, which forms the largest capacitance. If there is no outer wires, the outer-most wire also shows a large total capacitance since the E-field sharing is smaller. Wires between inner-most and outer-most wire show relatively small coupling capacitance.

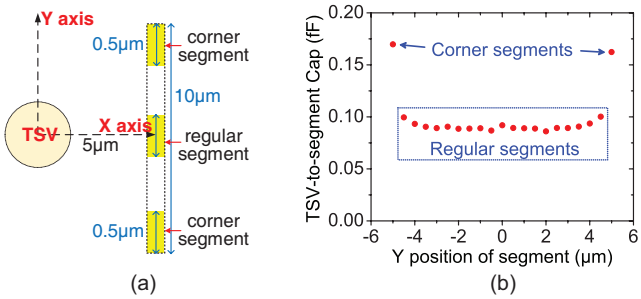

Figure 4: Corner segment impact. (a) Simulation structure with wire segment in 0.5μm length. (b) Extraction result for each segment.

We also observe that if ring pitch is small, e.g., 0.28μm, the coupling capacitance of middle rings becomes similar to each other due to similar E-field distribution in this region. When more rings are considered, e.g., from five rings to nine rings, the coupling capacitance difference is only 5% for middle rings. Therefore, if the ring pitch is small enough, we can use fewer rings to estimate the cases with more number of rings. This condition is often satisfied: if there are many rings in a TSV influence zone, this results in a smaller ring pitch. In our study, we use up to five rings for TSV-to-wire capacitance library generation.

2.3 Corner Segment Effect

The E-field sharing effect is also observed in different parts of a wire. We use one TSV-wire pair as an example and extract the capacitance using a field solver (Synopsys Raphael). Figure 4(a) shows our simulation structure. We break the wire into several segments, and each segment is 0.5μm in length. We observe that the corner segment shows much larger (1.8×) capacitance than the regular segment. This is because the corner segment is connected with the neighboring segment only at one side. This corner segment has larger capacitance even though it is located further away from the TSV. Therefore, for accurate extraction, corner segments need to be considered separately, especially for short wires. Otherwise, the extraction result will be underestimated.

2.4 Wire Coverage Effect

The E-field sharing effect also depends on how much part of a TSV is surrounded by metal wires. As shown in Figure 5, due to the E-field sharing, the coupling capacitance is evenly distributed among all the surrounding wires. Therefore, the unit length capacitance is larger when a TSV is only surrounded on one side. When the wire coverage around a TSV is high, even though the total capacitance increases, the unit length capacitance decreases. Therefore, the wire coverage effect also needs to be taken into account for an accurate TSV-to-wire capacitance extraction.

3. EXTRACTION AND VERIFICATION

In this section, we discuss how we build our TSV-to-wire coupling capacitance libraries in which multiple wires with all the aforementioned effects are considered. We build two libraries for regular segments, i.e., line library and ring library, and one library for corner segments.

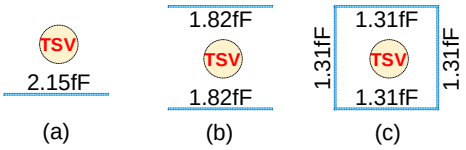

Figure 5: Impact of wire coverage around TSV on coupling capacitance.

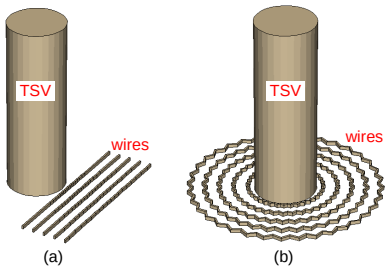

Figure 6: Test structures for library generation. (a) Structure for line library. (b) Structure for ring library.

3.1 Library Indexes

In our libraries, TSV and wire dimensions are used as indexes. To consider the impact of relative locations, the nearest TSV-to-wire distance, wire pitch, and wire location angle are also included. The location angle of a segment is defined as the angle between the ray from TSV to the segment and positive horizontal axis. To consider multiple-wires, we build libraries containing from one to five wires, and include the number of wires as a library index. Linear interpolation method is used when the target segment does not have the exactly same index as in the library.

Our libraries contain thousands of entries based on test structures covering a wide range of possible scenarios. Since the TSV and wire dimensions are mostly determined by technology and this work focuses on the extraction based on a 45nm technology, we fix TSV and wire dimension related indexes. The wire dimensions are based on M4 to M6 layer. The technology parameters we use in our work are as follows: TSV height is $15\mu m$, TSV radius is $2.5\mu m$, wire thickness is $0.28\mu m$, and wire width is $0.14\mu m$.

3.2 Line Library

We build a line library for TSVs covered by wires on one side. As shown in Figure 6(a), the line library is built by dividing the metal wires into segments and extract all the capacitance at the same time. The wire segment length is different depending on its distance from the TSV and the location angle to the TSV. For example, wire segments far from TSV with large location angle will be longer. Thus, a coarse grid structure can be applied to wires farther away from the TSV, while a finer grid structure can be used for closer wires. This helps to reduce library generation time using a field solver without sacrificing the extraction accuracy.

The line library assumes that only one side of TSV is surrounded by metal wires. In general, when TSV is surrounded by wires on multiple sides, the line library will give larger coupling capacitance, since it assumes there is less E-field sharing among wires. As the line library needs less complicated geometries, it helps reducing library generation time and memory space. In addition, we can extract several entries at the same time.

3.3 Ring Library

We build a ring library for TSVs covered by wires from all sides.

Table 1: Library Comparison

	Ring Lib	Line Lib	Corner Lib
For which segment?	regular	regular	corner
E-field sharing	strong	weak	weak
Capacitance value	smaller	larger	largest
Geometry complexity	high	lower	lowest
Parallel extraction?	no	yes	no
Generation time	longest	shortest	shorter

As shown in Figure 6(b), we pick one test segment and duplicated it to form a ring around TSV. Then we extract the total capacitance of the ring and divide it by the total number of the ring segments. To simulate multiple wires, multiple rings are added around TSV. We perform this on all test structures and save extraction results into the library. The ring library is built assuming a heavy E-field sharing around TSV. Thus, in general cases, when TSV is covered by fewer metal wires, it will underestimate the coupling capacitance. Although, the ring library needs to extract only one capacitance at a time, the overall simulation time is the longest due to the complex geometries elements such as polygons used to form a ring.

3.4 Corner Library

Since the corner segment has only a neighbor on one side, and its side wall also contributes to the coupling, it shows much larger capacitance compared with regular segments. The test structure is similar to the one used in the line library. However, we merge all the regular segments and only extract the capacitance of the corner segment. Compared with other libraries, it has the largest capacitance value. The geometry complexity for corner library is smallest, but unlike the line library where many entries can be extracted in parallel, corner library needs longer runtime to build. Table 1 shows the library comparison.

3.5 Pattern Matching Algorithm

Once all the libraries are built, we divide the all the wires into segments and choose the most similar test structure in the library to obtain the TSV-to-wire coupling capacitance. Since Raphael does not consider the frequency dependent silicon substrate, we use a dielectric material with a permittivity of 11.9F/m in our simulations.

We develop an algorithm for pattern-matching-based TSV-to-wire coupling capacitance extraction. The extraction is conducted on each TSV one by one. We parse the routing results and build a list for each TSV. The list contains all the wires within a TSV influence region. Wires shorter than $2\mu m$ is ignored. After one TSV is picked, we divide the space into 72 circular sectors, each with 5° in central angle. If finer meshing grid is used, library generation time will be longer. Wires are cut into segments at the sector boundary. Then we exclude segments beyond the distance threshold and gather segments with the same location angle into a list. Each TSV has 72 lists and each list contains the segments with the same location angle to the TSV. The look-up procedure is applied to each segment in the list and it looks for the closest entry that matches the segment. Linear interpolation is used when the library index does not exactly match. Average spacing is used for unevenly distributed wires. If the list contains no more than the maximum number of wires simulated in the library, we directly look up from the library. If the list has more wire segments than the library supported, library entry with maximum number of wires is used. For corner segments, results from corner library is used. For regular segments, we combine the line library and ring library based on wire coverage around the TSV. If the wire coverage is above 80%, we use the ring library only. On the other hand, if the coverage is below 20%, we use the line library only. Otherwise, we use a

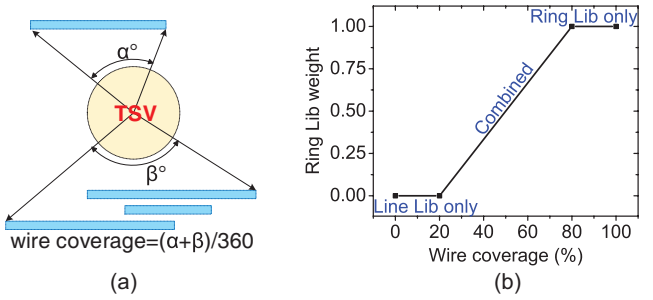

Figure 7: Our combined method. (a) shows the calculation of wire coverage, (b) shows the calculation of weighted average.

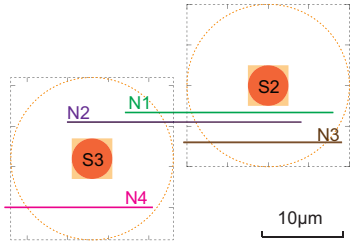

Figure 8: Sample extraction layout with two TSVs and their four surrounding wires.

weighted average from both libraries. Wire coverage calculation is shown in Figure 7(a) and the ring library weight is shown in Figure 7(b). Finally, the capacitance for the same net will be added and annotated into SPEF file and used for full-chip analysis.

3.6 Validation Against a Field Solver

To validate our extraction method, we perform extraction on sample layouts. Figure 8(a) shows a sample layout. Its extraction results are listed in Table 2. The results show that our extraction method is very accurate in all cases. The maximum error is only 0.17fF and the average error is only 0.05fF.

For full-chip verification, we implement a two-die 3D design and apply our method to all TSVs. The TSV influence region for our extraction is $10\mu m$. We run Raphael simulation on each TSV with $10\mu m$ as simulation window size. As discussed before, using a single ring library gives a 8.3% underestimated total capacitance, while using a single line library gives a 5.3% overestimated total capacitance. However, both of them are accurate enough: an average error of 0.171fF for the ring library only case and 0.163fF for the line library only case.

If we consider the wire coverage effect and combine both libraries in calculation, the total capacitance error is only 1.9% and the average error drops to only 0.112fF. The correlation coefficients are 0.971, 0.966 and 0.981 for ring library, line library, and combined method, respectively. Full-chip extraction result is shown in Figure 9 and the library comparison is listed in Table 3. Table 4 shows the simulation time comparison. Although our method needs longer time to build the libraries, once all libraries are ready, it can be applied to any designs. Also, field solver needs much longer time and memory on larger design with more TSVs. The runtime and memory usage are negligible compared with the field solver case. Therefore, we conclude that both ring and line libraries are accurate for multiple wires, and our combined method considering wire coverage effect is very fast and highly accurate.

4. FULL-CHIP TSV-TO-WIRE IMPACT

Table 2: Sample layout extraction result from Figure 8, where capacitance is reported in fF.

TSV	Wire	Raphael	Our method		
			Ring Lib	Combined	Line Lib
S2	N1	1.76	1.49 (-15%)	1.93 (+9.3%)	2.07 (+17%)
S2	N2	0.76	0.68 (-10%)	0.76 (-0.7%)	0.78 (+2.5%)
S2	N3	0.81	0.86 (+6.2%)	0.81 (-0.6%)	0.79 (-2.8%)
S3	N1	0.31	0.29 (-7.9%)	0.31 (-0.3%)	0.34 (+6.9%)
S3	N2	1.38	1.28 (-6.6%)	1.33 (-3.6%)	1.37 (-0.7%)
S3	N4	1.62	1.49 (-7.8%)	1.53 (-5.3%)	1.57 (-2.9%)

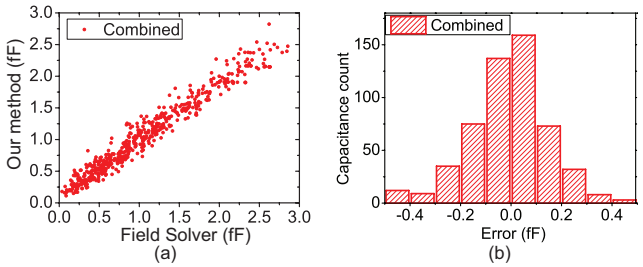

Figure 9: Full-chip Verification using combined method. (a) shows extraction result comparison, (b) shows error histogram.

4.1 Design Specification and analysis flow

We use a 64 point FFT design based on 45nm technology. There are 47K gates in this design and it is partitioned into two dies. The cross-section structure is shown in Figure 1. The TSVs are $15\mu m$ in height and $2.5\mu m$ in radius. TSV landing pad size is $5\mu m$. The bottom die has 330 TSVs with the landing pad on M1. TSVs are evenly distributed on the bottom die with about $18\mu m$ spacing to each other. Therefore, we pick $18\mu m$ as our extraction distance threshold to avoid other TSVs while ensure all wires within TSV influence region is extracted.

Full chip placement results are shown in Figure 10. The top die has TSV landing pad on its top metal layer to connect TSVs from the bottom die. For our study, only the capacitance between TSV and metal wires on top metal layer is extracted since other metal layers are blocked by either device layer or metal layers. We assume the wires are routed in preferred direction. Since the metal layer M4 to M6 have the same wire dimension, our library can handle design with M4 to M6 as their top metal layer. We present our design up to M4 in following sections. With the usage of more metal layers, the wire length on top metal layer is reduced.

We apply our pattern matching method to FFT design and then use Primetime to merge all the parasitic file, e.g., TSV-to-wire coupling, wire-to-wire coupling and TSV-to-TSV coupling using the extraction method proposed in [5]. Then we use Primetime for full-chip timing and power analysis and use HSPICE for worst case noise analysis.

4.2 Full-chip Analysis

The full-chip analysis result is shown in Table 5. The critical path starts from a register in the top die, goes to the bottom die through TSV274, then goes back to the top die through TSV89 and ends on another register. As TSVs are on the critical path in this design, TSV parasitic affects the Longest-Path-Delay (LPD) of the whole design.

TSV coupling elements are the major part of TSV parasitics. However, if TSV-to-wire capacitance is ignored, there will be a large underestimation in TSV net capacitance and TSV-induced de-

Table 3: Full-chip Extraction with $10\mu m$ extraction threshold

	Ring Lib	Combined	Line Lib
Total Cap (fF)	538	579	618
Total Cap error	-8.3%	-1.9%	+5.3%
Correlation coefficient	0.971	0.981	0.966
Average error (fF)	0.171	0.112	0.163

Table 4: Simulation time and memory comparison on FFT64 design on XEON E5.

Library generation time	Line Lib	8h
	Ring Lib	18h
	Corner Lib	9h
Extraction method	Field-solver	Our method
Runtime	7.5h	5.8s
Memory space	>500MB	~20MB

lay and noise. Without TSV-to-wire coupling capacitance, there is a 2.01pF underestimation on total TSV net capacitance and a 0.6ns underestimation on LPD. Note that LPD change only comes from net TSV274 and TSV89 as we assume clock network is ideal. If real clock tree network is included, the LPD will be further affected since the clock signal needs to be delivered to the top die using TSV and it is also affected by TSV-to-wire parasitics. After TSV-to-wire capacitance is considered, the total power on TSV net also increases by 17.5% due to larger capacitance. And there is also a noticeable change on total net switching power though its impact on total power is negligible. Note that the sample design is a small circuit, if the design uses larger footprint with more TSVs and longer wirelength, the TSV-to-wire impact on the power will increase. In worst case, all of the wires that has coupling capacitance to the victim TSV serve as aggressors. Therefore, if TSV-to-wire capacitance is not considered, a lot of aggressors are ignored which results in smaller TSV net noise. The result shows that total noise on TSV net doubled in worst case after the TSV-to-wire coupling is plugged in.

5. COUPLING MINIMIZATION

5.1 Impact of Keep-Out-Zone

The TSV-to-wire coupling is majorly between TSV and the nearest metal layer. Therefore, for TSV-to-wire coupling reduction, reducing the total wire length on top metal layer while increasing the minimum distance between TSV and nearest wire help reducing TSV-to-wire coupling. We define this minimum distance as Keep-Out-Zone (KOZ) of the top metal layer routing. We designed our FFT with different KOZ size with die shots shown in Figure 11. The original design has a KOZ of $0.5\mu m$. With larger KOZ, the capacitance between nearest wire and TSV will reduce. Also, larger KOZ reduces routing resources on top metal layer. Therefore the total wire length on the top metal layer decreases with larger KOZ. The drawback for this optimization method is that it results in longer wire length and heavier routing congestion on other layer. If the routing resources are not enough, it can have negative impact on routing quality. The routing quality degradation introduces longer routing, more buffers and heavier coupling between wires which have negative impact on timing and power. We re-designed our top die with a KOZ size of $2.5\mu m$ and $5\mu m$ while we kept the placement result. Increasing KOZ reduces the total wirelength on the top layer but makes routing on other layer more crowded.

We perform full-chip analysis with updated extraction results. Full-chip analysis result is shown in Table 6. With larger KOZ, total wire length on top metal layer is reduced. Therefore the TSV-to-wire coupling also shows smaller impact on the full-chip timing and noise. Compared with the original design, the LPD decreases by 2.6% and 6.1% for $2.5\mu m$ and $5\mu m$ KOZ, respectively. Note that the timing degradation may increase if there's not enough routing resources. The KOZ impact on full-chip power result is much smaller since TSV-to-wire capacitance decreases but the wire-to-wire capacitance increases on other layer. Larger KOZ also helps reducing total noise on TSV net. The total worst-case noise on TSV net can be reduced by 14.3% and 45.1% for $2.5\mu m$ and $5\mu m$ KOZ, respectively. Therefore, we conclude that increase KOZ is effective in reducing TSV-to-wire coupling.

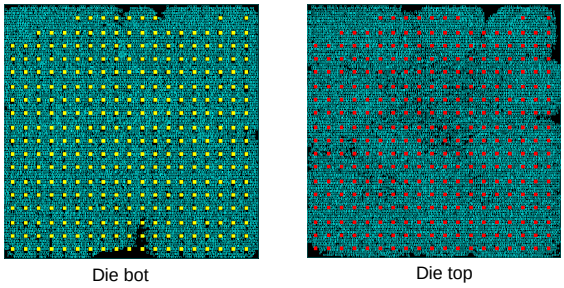

Figure 10: Placement layout shots of FFT64. The footprint is $380\mu m \times 380\mu m$.

Table 5: TSV-to-wire coupling full-chip impact. Capacitance is reported in pF.

Top metal layer	M4	
Total TSV MOS cap	4.47	
Total TSV-to-TSV coupling cap	0.74	
Total TSV-to-wire coupling cap	2.01	
Is TSV-to-wire included?	no	yes
Longest path delay (ns)	4.48	5.08 (+13.4%)
Total power on TSV net (mW)	0.303	0.356 (+17.6%)
Total net switching power (mW)	2.42	2.50 (+3.3%)
Total noise on TSV net (V)	32.5	78.2 (+104%)

5.2 Guard Ring Protection

Another way to protect the victim TSV is to use a grounded guard ring. Different from the previous work [5] focusing on TSV-to-TSV coupling reduction and using a guard ring in active area, this work uses a wire guard ring on top metal layer. The grounded guard ring shares some E-field around TSV, thus it introduces a ground capacitance on the TSV. This ground capacitance has small delay and power overhead on TSV nets, but it reduces the coupling noise on TSV net. Moreover, The guard ring now becomes the nearest wire around TSV which makes all other wires have neighbors on both sides. Therefore, the TSV-to-wire coupling capacitance is reduced and TSV is better shielded with guard ring.

To study the guard ring impact, we use Raphael on a shielded TSV and extract the capacitance. The simulation structure is a single TSV with a surrounding guard ring. A $10\mu m$ long wire is located $8\mu m$ far from the center of TSV. Figure 12 shows the capacitance between TSV, wire and ground. With a wider guard ring width, the TSV is better protected from TSV-to-wire coupling. But the ground capacitance on TSV and wire increases with larger guard ring which introduces larger delay and power overhead.

To extract the TSV-to-wire capacitance on a shielded TSV, we build libraries in which TSVs are surrounded by the guard ring. We designed the FFT64 with two different guard ring width, the die shots are shown in Figure 13. This design is based on previous layout with $2.5\mu m$ KOZ. We add the guard ring in the KOZ region

Table 6: Keep-out-zone impact on full-chip design. Power is reported in mW.

KOZ size (μm)	0.5	2.5	5
Longest path delay (ns)	5.08	4.95 (-2.6%)	4.77 (-6.1%)
Total power on TSV net	0.356	0.342 (-3.9%)	0.327 (-8.1%)
Total net switching power	2.50	2.47 (-1.2%)	2.45 (-2.0%)
Total noise on TSV net (V)	78.2	67.0 (-14.3%)	42.9 (-45.1%)

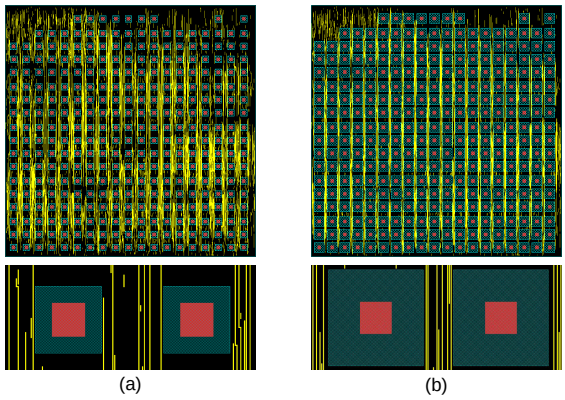

Figure 11: Routing layout shots of FFT64 with different KOZ. (a) 2.5μm KOZ, (b) 5μm KOZ.

so that design placement and routing results are kept the same. After re-extraction on TSV-to-wire and wire-to-wire coupling capacitance, we perform full-chip analysis and the results are shown in Table 7. For design up to M4, the longest path will increase by 0.6% and 1.2% for 0.5μm and 1.5μm guard ring, respectively. This impact comes from two aspects. The ground capacitance on TSV increases but TSV-to-wire capacitance decreases. The total capacitance on TSV will always increase with wider guard ring since the metal coverage increased. Although there is a small increase on TSV switching power, guard ring impact on total power is negligible. Our results show that guard ring is very effective in TSV net noise reduction and the total TSV net noise reduces by 13.4% and 20.0% for 0.5μm and 1.5μm guard ring, respectively. Since the KOZ of this design is 2.5μm, compared with the original design with 0.5μm KOZ, a combination of increasing KOZ and guard ring protection can reduce up to 31.4% total TSV noise. Since the TSV-to-TSV coupling elements remain the same and the it also contributes to the TSV net noise, increasing KOZ and adding guard ring cannot reduce TSV net noise too much. From the results, we conclude that the guard ring is effective in TSV net noise reduction with small delay and power overhead.

6. CONCLUSION

In this paper, various factors affecting TSV influence region and TSV-to-wire capacitance are studied. For fast and accurate full-chip TSV-to-wire capacitance extraction, we built a pattern matching algorithm which considers multiple wire effects, corner segment effects and wire coverage effects. We verified our method using real 3D IC layout against field-solver simulation. Then we applied our method on a FFT64 3DIC design and studied the TSV-to-wire impact on full-chip level. Analysis results show that TSV-to-wire coupling is not negligible and it has large impact on full-chip delay and TSV net noise. To alleviate the TSV-to-wire coupling, we tried to increase the KOZ around TSV in top routing layer and use a ground guard ring for further optimization. Our results show that both method are effective in TSV net noise reduction with small overhead on routing congestion, full-chip timing and power.

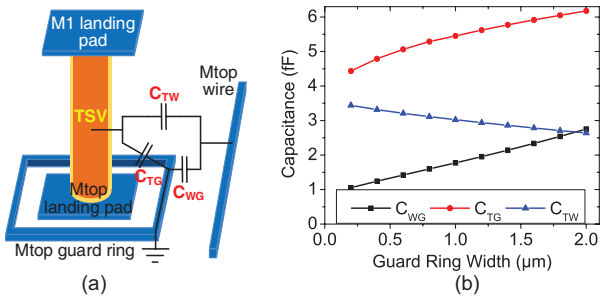

Figure 12: Guard ring capacitance, (a) shows the simulated structure (b) shows the extraction result.

Table 7: Guard ring impact on full-chip design with 2.5μm KOZ. Power is reported in mW.

Guard ring width (μm)	0	0.5	1.5
Longest path delay (ns)	4.95	4.98 (+0.6%)	5.01 (-1.2%)
Total power on TSV net	0.342	0.351 (+2.6%)	0.358 (+4.7%)
Total net switching power	2.47	2.475 (+0.2%)	2.479 (+0.4%)
Total noise on TSV net (V)	67.0	58.0 (-13.4%)	53.6 (-20.0%)

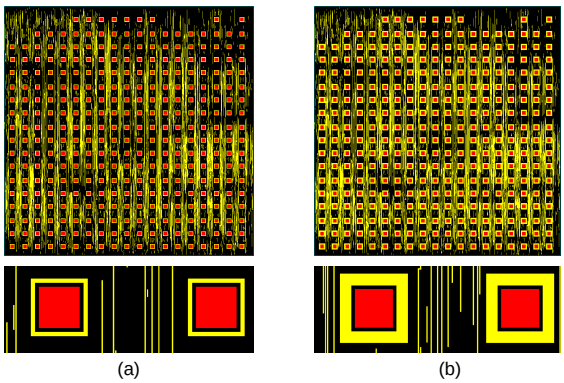

Figure 13: Routing layout shots of FFT64 with guard ring. (a) 0.5μm guard ring, (b) 1.5μm guard ring.

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