On Accurate Full-Chip Extraction and Optimization of TSV-to-TSV Coupling Elements in 3D ICs

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***Abstract*—In this paper, we present a multiple-TSV based TSV-to-TSV coupling model and extraction methods that consider the impact of depletion region, the silicon substrate effect, and the electrical field distribution around TSVs. Our studies show that these factors have a significant impact on the individual and full-chip scale TSV-to-TSV coupling. Our effort leads to a simplified coupling model that is accurate and efficient on timing, power, and signal integrity in full-chip scale. In order to alleviate the coupling noise in full-chip level 3DIC, we propose grounded guard rings that are more effective than grounded TSV insertion. Results show that our approach reduces coupling noise on TSV nets up to 27.3% with only 7.65% area overhead.**

I. Introduction

Through-silicon via (TSV) is a popular choice to implement three dimensional integrated circuit (3DIC). For TSV-based 3DIC, introducing TSV not only increases the total die area, but also has impact on signal integrity, longest path delay, and power consumption. For designs that require high performance, noises on the TSV nets make it difficult to control clock skew and estimate cell delay. For low power applications, the supply voltage is lower than normal circuits. Thus, coupling noise on critical nets is a threat to the whole system. Therefore, a precise estimation of the TSV impact on the whole system is essential. Current parasitic extraction tools can precisely estimate coupling between 2D nets, but parasitics of TSVs must be extracted using TSV model. Field solver tools can perform a detailed extraction on any structures, but the long simulation time and large memory requirement make it inappropriate for the fullchip extraction.

[1] and [2] build a 2-TSV model that calculates TSV coupling using parallel wires. [3] builds a TSV model based on Poisson equation and takes the depletion region into consideration. These studies accurately model TSV when only 2-TSV exist in a layout, but it lacks precision if there are more than two TSVs. [4] uses an RLC mesh structure and models each mesh cell based on their material property. It can model TSV shielding structure with guard rings, but the impact of silicon body effects such as depletion regions are ignored. Other studies use empirical model [5], which is not scalable when TSV dimension changes and does not consider electric field (E-field) effect. Traditional modeling methods cannot handle cases with multiple TSVs and ignore several important silicon impacts and E-field effects of the TSV. The 2-TSV model overestimates the coupling parasitics and many TSV models ignore field and substrate effects. These models over-estimate the TSV MOS capacitance and thus over-estimate noise and delay on TSV nets. RLC mesh models have too many extracted RLC components on the TSV coupling that it is not feasible for full-chip analysis. Other TSV models [6] [7] consider part of the field effects, but not altogether. Therefore, a compact TSV model that considers multiple TSV-to-TSV coupling, substrate impact, and E-field effect is essential for full-chip design.

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Therefore, in this paper, we make the following contributions: (1) We propose a new multi-TSV model that also considers the effects of silicon depletion region, silicon substrate, and E-field distribution with minimum components; (2) We propose two coupling analysis methods, for analyzing worst-case and average case TSV-to-TSV coupling, and perform a detailed extraction and analysis on the full-chip design using our multi-TSV model; (3) We perform an accurate full-chip coupling analysis considering all the silicon and field effects on two design-style, namely, regular placement design and irregular placement design showing TSV coupling impact; (4) We propose a guard-ring model and study the impact of guard-rings in full-chip level. Based on our model, we show the impact of guard-ring on both regular and irregular placement design and show its effectiveness in noise reduction, delay, area, and design time.

II. TSV-to-TSV Coupling Model

A. Two-TSV Model

We show the traditional 2-TSV model that many papers used in in Fig. 1 [1]. It assumes that the impedance of the coupling path between TSVs only depends on the distance and the size of TSVs. The traditional model calculates the substrate resistors and capacitors assuming it is a parallel wire. It assumes that there is no E-field other than the coupling field and there are no obstacles in the substrate. The following equations are used to extract coupling components between TSV i and j:

$$C_{ox} = \frac{\pi \varepsilon_{SiO_2} L_{TSV}}{\ln \frac{R_{TSV}+T_{ox}}{R_{TSV}}} \tag{1}$$

$$C_{Si,ij} = \frac{\pi \varepsilon_{Si} L_{TSV}}{\ln\left\{\frac{P_{ij}}{2R_{TSV}+T_{ox}} + \sqrt{\left(\frac{P_{ij}}{2R_{TSV}+T_{ox}}\right)^2 - 1}\right\}} \tag{2}$$

$$R_{Si,ij} = \frac{\varepsilon_{Si}}{C_{Si,ij}\sigma_{Si}} \tag{3}$$

where L_{TSV}, R_{TSV}, T_{ox}, and P_{ij} are the height of the TSV, radius of the TSV, liner thickness, and the pitch between two TSVs, respectively. The self inductance and mutual inductance of the TSV are calculated based on parallel wires, while the TSV resistors are calculated based on cylinder wires with skin-effects in high-frequency range [2]. Previous studies have shown that this model is highly accurate in 2-TSV case compared with and measurement results [8].

B. Multi-TSV Model

The 2-TSV model overestimates TSV coupling capacitance, and therefore overestimates coupling noise and timing delay [9]. The coupling capacitance does not increase linearly as the number of neighbors increase. Even when a victim TSV is surrounded by

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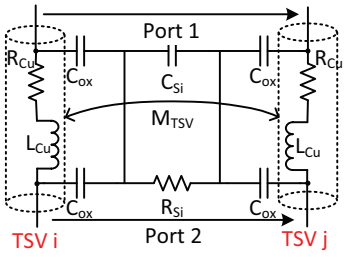

Fig. 1. Traditional 2-TSV model

TABLE I
S-PARAMETER COMPARISON BETWEEN OUR MODEL AND 3D SOLVER. TSV DIMENSIONS IN μM AND ERROR IN DB.

TSV radius	TSV height	TSV liner width	Max error
2	30	0.2	0.016
		0.5	0.011
	60	0.2	0.017
		0.5	0.012
4	30	0.2	0.015
		0.5	0.014
	60	0.2	0.018
		0.5	0.013

many aggressor TSVs, the total capacitance cannot be more than the capacitance of a coaxial wire. , which is given by:

$$C_{\text{si,max}} = \frac{2\pi\varepsilon_{si}L}{\ln(P/r)} \tag{4}$$

where P and r is the outer and inner radius of the coaxial wire.

To model multiple TSVs, we use the TSV model presented in [9]. We first compute the TSV-array inductance matrix $[L_{Si}]$, where each symbol is calculated by the following formula:

$$L_{Si,ij} = \begin{cases} \frac{\mu_{Si}L_{TSV}}{\pi} \ln\left[\frac{P_{i0}}{R_{TSV}+T_{ox}}\right] & \text{when } i=j \\ \frac{\mu_{Si}L_{TSV}}{2\pi} \ln\left[\frac{P_{i0}P_{j0}}{P_{ij}(R_{TSV}+T_{ox})}\right] & \text{when } i\neq j \end{cases} \tag{5}$$

P_{i0} and P_{j0} are the pitch between aggressor TSV and the victim TSV, and P_{ij} is the pitch between aggressor TSV i and j. By using the relation of homogeneous material between the capacitance matrix and the inductance matrix [10], we get the capacitance matrix for TSV array:

$$[C_{Si}] = \mu_0\varepsilon_{Si}L_{TSV}^2[L_{Si}]^{-1} \tag{6}$$

We only use the coupling components between aggressor TSV i and the victim, which is given by:

$$C_{Si,ii} = \sum_{k=1}^{N} C_{Si,ik} \tag{7}$$

We calculate the substrate coupling resistance $R_{Si,ii}$ by using (3). Table I shows S-parameter comparison between field solver results (Ansys HFSS) and our model. From the result we conclude our multi-TSV model is scalable and accurate.

III. TSV-INDUCED SILICON AND FIELD EFFECTS

A. Impact of Silicon Depletion Region

In this section, we discuss the effect of silicon depletion region on TSV coupling. The copper TSV, silicon oxide liner and the silicon substrate form a MOS structure that forms a depletion region around the TSV. The flat band voltage for this MOS structure is:

$$V_{FB} = \varphi_{Cu} - \varphi_{Si} - Q_s/C_{ox} \tag{8}$$

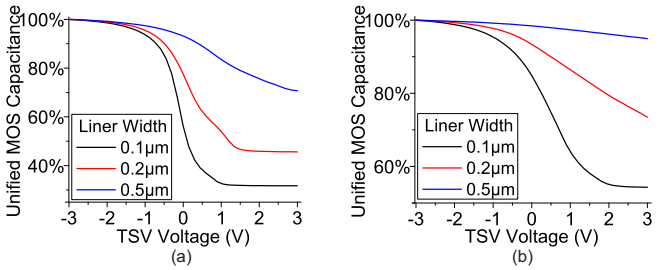

Fig. 2. Depletion effects on TSV MOS capacitance with substrate doping of (a) $10^{15}/cm^3$, (b) $10^{16}/cm^3$

where φ_{Cu} (= 4.65V), φ_{Si}, and Q_s are work function of copper, work function of the silicon, and the charges inside oxide liner, respectively. From the equation, the flat band voltage is -0.3V when the substrate doping is $10^{15}/cm^3$ and no extra charges are within the liner. Thus, for most digital systems, when the voltage on TSV is between 0V and VDD, a depletion region always exists around the TSV that introduces a voltage dependent capacitance C_{dep}. We assume a complete depletion and the TSV MOS capacitance cannot resume even if the silicon substrate is strongly inverted. The operating frequency in digital systems is usually above several hundreds of MHz and TSVs are usually build inside the low-doped substrate with a large height. Therefore, not enough carriers around TSVs can respond to such high frequency. After considering the depletion region, (5) should be rewritten as:

$$L_{Si,ij} = \begin{cases} \frac{\mu_{Si}L_{TSV}}{\pi} \ln\left[\frac{P_{i0}}{R_{TSV}+T_{ox}+W_{dep}}\right] & \text{when } i=j \\ \frac{\mu_{Si}L_{TSV}}{2\pi} \ln\left[\frac{P_{i0}P_{j0}}{P_{ij}(R_{TSV}+T_{ox}+W_{dep})}\right] & \text{when } i\neq j \end{cases} \tag{9}$$

and the TSV MOS capacitance is calculated by:

$$C_{MOS} = \frac{C_{ox}C_{dep}}{C_{ox}+C_{dep}} \tag{10}$$

where C_{dep} and W_{dep} are the depletion capacitance and depletion region width. They follow the equation:

$$C_{dep} = \frac{\pi\varepsilon_{Si}L_{TSV}}{\ln\frac{R_{TSV}+T_{ox}+W_{dep}}{R_{TSV}+T_{ox}}} \tag{11}$$

We use Synopsys Sentaurus to extract the depletion capacitance. Fig. 2 shows the depletion region effects. As we can see from the plot, the depletion region width is heavily dependent on substrate doping concentration, the liner width, and TSV voltage. In terms of coupling noise and TSV-induced timing and power degradation, the worst-case is when all TSVs are grounded (maximum MOS capacitance). The best case is when TSVs are all at VDD (minimum MOS capacitance). Therefore, we assume two cases for simulation: Worst-case simulation when all TSVs are tied to GND, and average case simulation when all TSVs are tied to half of VDD.

We use a 3-TSV test structure shown in Fig. 3(a) and study the impact of the depletion region. The HSPICE simulation result on 3-TSV test structure is shown in Fig. 3(b). For signal frequency within 1GHz, the MOS capacitance is the dominate component in the coupling structure, therefore, any variation of the depletion region width has a large impact on the coupling noise and timing degradation. High-doped substrate make it difficult for the MOS capacitor to reach the strong inversion and the maximum depletion width. Therefore, within 0V to 1.2V range, even though the depletion region increases the impedance on the substrate, high doping concentration introduces

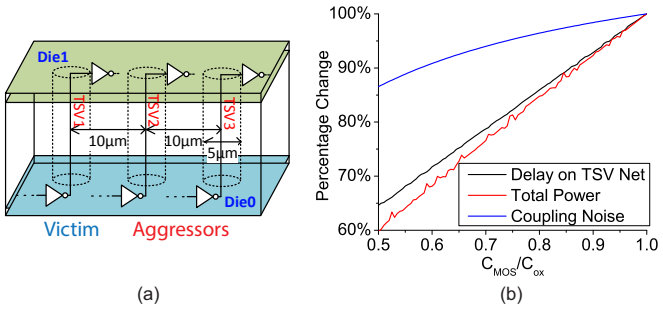

Fig. 3. (a) 3-TSV test structure, (b) depletion region effects

large coupling and delay by increasing the MOS capacitance. The depletion region has a larger impact on TSVs with thinner liner width, since the depletion width is more comparable to the oxide thickness if the liner width is small. With the development of 3D IC fabrication technology, TSVs are getting smaller and denser in future technology nodes, and impact from the TSV depletion region will increase since liner width scales down with TSV dimensions.

Wide depletion region helps reducing TSV coupling noise and increasing performance, but any NMOS located within or near the depletion region suffers a large reduction in threshold voltage. The leakage from the substrate of the PMOS to the ground increases since the potential energy barrier is lowered. Therefore the keep-out zone of the TSV should increase to prevent unwanted side-effects introduced by TSVs. Beside the trade off between area and performance, another factor should be taken into consideration when determine the liner width. According to (8), thick oxide liner helps reducing the total MOS capacitance, but introduces a larger variation in flat band voltage of the TSV MOS capacitor and affects performance and signal integrity results.

B. Impact of Substrate Resistance

Silicon substrate also plays an important role in TSV-to-TSV coupling issue. Many previous modeling studies ignore the effect of silicon substrate and assume the substrate nodes are floating. This assumption is not appropriate since most designs connect the substrate to the ground net using substrate contacts. Even though each TSV has a keep-out zone, there is a finite impedance from substrate around the TSV to the ground node. Assuming the substrate to be floating will introduce over-estimation on the coupling noise since all the charges on the substrate accumulate around the victim TSV and there is no discharging path for them. It also under-estimates the delay on TSV nets since the capacitance of the TSV to the ground is ignored. Therefore, we need to model the discharging path using substrate resistors and capacitors. Fig. 4 illustrates our proposed multi-TSV model with all silicon and field effects.

Using Synopsys Raphael, we extract body capacitance and evaluate body resistance from (3). Fig. 5(a) shows the result comparison on the test structure with or without considering the silicon discharging path. Since TSVs are buried in bulk silicon and active layer is on one side of the substrate, the discharging path has larger impact on designs with short TSV since it cannot affect the electrical field on the other side of the substrate.

Furthermore, if grounded active region is placed between two TSVs, the impedance to the ground reduces and the impedance between two TSVs increases. This is because part of the electrical field is decoupled by the grounded active layer. This effect further reduces the crosstalk between TSVs. Fig. 6 shows this structure and

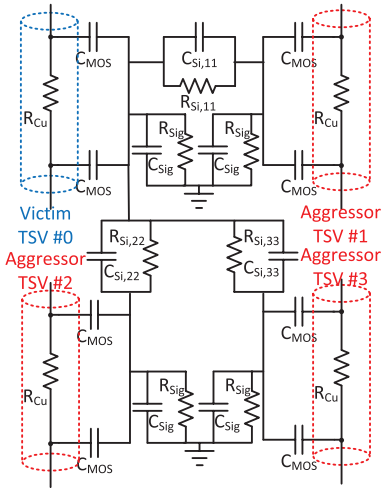

Fig. 4. Multi-TSV coupling model with depletion capacitance and body resistance

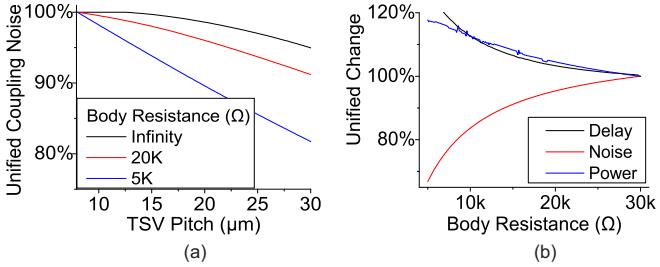

Fig. 5. Body resistance effect on (a) noise, delay, and power, (b) relation between TSV coupling noise and TSV pitch

the Raphael extraction results. Depending on the size of the grounded active layer and the distance between two TSVs, a maximum variation of 9.6% and 87.1% exists in coupling capacitance and body resistance, respectively. In general, if the victim is properly protected by the ground, it suffers less from the noise but more from the performance loss.

After considering the finite impedance from substrate to the ground, the coupling noise shows a larger dependence with the TSV pitch. Fig. 5(b) shows how coupling noise is related to TSV distance using HSPICE simulation. We use the coupling noise value when TSV pitch is $8\mu m$ as a reference. If there's a finite impedance to the ground at the substrate nodes, the R_{si} and C_{si} show a larger influence on the coupling noise. This is because the coupling voltage is divided between impedance of coupling path and the discharging path. Therefore, the TSV distance becomes an important factor in TSV coupling and spreading the TSVs is more effective in noise reduction if the substrate is well grounded.

C. Impact of Electrical Field Distribution

In previous studies, all of the coupling components connecting other TSVs share a single node around victim TSV which is connected to TSV net by the MOS capacitor. This model is very accurate in Two-TSV cases. But if multiple TSVs are considered altogether, this coupling model creates a direct coupling path through other aggressor TSVs and causes an over-estimation in coupling noise. Consider a 5-TSV case which is shown in Fig. 7, where the victim TSV is in the array center, the electrical field around the victim

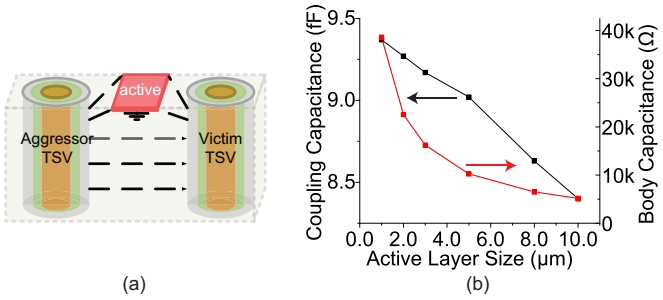

Fig. 6. (a) Two-TSV structure with grounded active layer (b) Raphael extraction results

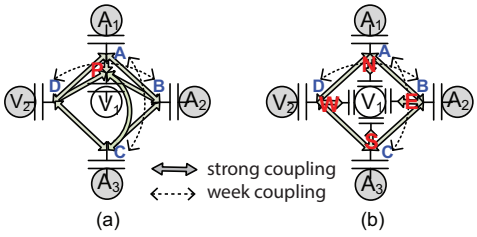

Fig. 7. Model comparison for 5-TSV case: (a) original model, (b) E-field distribution-aware model

TSV is distributed among each aggressor. Only neighbor TSVs are strongly coupled. However, because of the common node P, aggressor A_2 is directly coupling with victim V_2 through path BPD, which results over-estimation TSV-coupling. Fig. 8(a) illustrate the HFSS simulation on electrical field map. It is clearly seen from the plot that the coupling from each aggressor is mainly through one of the four sides of the victim TSV, and there is few coupling between the far side of the victim and the aggressor.

In Two-TSV model, coupling components are only determined by the distance between two aggressors. However, if the locations of multiple TSVs are considered in modeling, the charges on the victim TSV is mainly determined by its nearest neighbor, which is a major factor in multi-TSV model. In worst-case noise analysis, it does not cause discrepancy since all of the aggressors are assigned with the same waveform. There's no difference between each aggressors except for their aggressive strength. But in real modeling case, the direct path between TSVs pessimistically estimates of the coupling noise on the victim TSV. To model the field distribution effect around the victim TSVs, we use four nodes to connect the coupling parameters around the victim TSV, shown in Fig. 7(b), where the victim's MOS capacitor is split into four and A_2 and V_2 is only weekly coupled. Fig. 8(b) shows the modeled coupling parameters of the structure compared with the results extracted using HFSS field solver. The result shows both model match well on the coupling noise between nearest TSVs. But when far-away TSVs are considered, there is a 1.1dB over-estimation in coupling noise due to the direct path between TSVs in the original model.

IV. Full-chip Analysis

In this section, we demonstrate an SI analysis flow on a design to show the silicon effects on the full-chip level and compare two different design styles, namely, TSV regular placement and irregular placement.

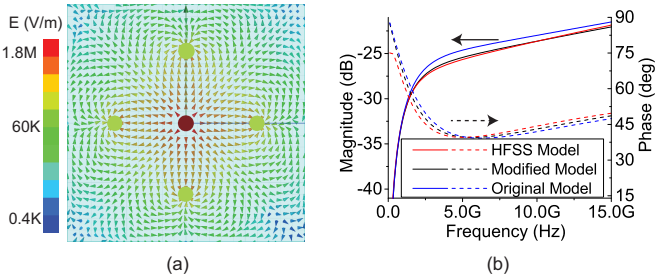

Fig. 8. E-field impact. (a) HFSS simulation result of E-field distribution, (b) noise parameter comparison

TABLE II
Inductance Impact on TSV Nets

	wo/ TSV coupling	w/ inductor	wo/ inductor
Rise delay (ps)	22.63	168.05	168.06
Fall delay (ps)	11.92	108.88	108.96
Power (*muW*)	3.47	21.058	21.059
Peak noise (mV)	0	27.06	27.64

A. Models Used for Full-chip Analysis

The multi-TSV model in [11] is accurate in a wide range of operating frequencies. However, this model is not feasible because of the many parasitic elements in the actual netlist. The simulation runtime is another important factor that must be considered due to hundreds (or even thousands) of TSVs. Current design tools cannot fully handle the TSVs in 3D IC. Therefore, we need to simplify the model to handle TSV coupling in timing and power analysis engines such as Synopsys Primetime.

To precisely model TSV-coupling, the inductors are included to model the magnetic field coupling between TSVs. In high-frequency range, ignoring the inductors lead to S-parameter discrepancy because the impedance of the inductors are comparable to the resistance of the TSVs. However, in a frequency range below 5GHz, like in most digital systems, the impact of the inductors are almost negligible in terms of noise, delay, and power. Table II shows the HSPICE simulation results on the 3-TSV test structure (Fig. 3). From the result, we prove that we can ignore the inductors. Therefore, we use the multi-TSV model without inductors in our full-chip analysis.

We use Synopsys Primetime for full-chip timing and power analysis. Since Primetime is not a SPICE engine, it cannot run simulation on a design that has floating nets and support a detailed voltage transition. To avoid floating nets, traditional Primetime model used in [1] and [9] ignores the TSV MOS capacitors (C_{MOS}) but keeps the coupling capacitor (C_{si}). This model will under-estimate TSV-induced delay and power consumption since TSV MOS capacitor is much larger than coupling capacitor. However, in our approach, we add a substrate net in the Verilog netlist. We use SPEF file to annotate substrate resistor network. Assuming a substrate with 10s/m substrate conductivity, from (3) we can calculate the impedance ratio between substrate coupling resistor (R_{Si}) and capacitor (C_{Si}), which is 0.11 at 5 GHz signal frequency. Below 5 GHz signal frequency, this ratio is even smaller and it is not dependent on the TSV-to-TSV pitch. Since the coupling resistor and capacitor are in parallel connection, the resistor dominates the coupling. Moreover, compared to the TSV MOS capacitor (C_{MOS}), substrate coupling capacitor is smaller by one-order magnitude. Therefore, we can ignore it if the signal frequency is below 5GHz. Fig. 9 shows the S-parameter comparison results. HSPICE transient simulation result is shown in

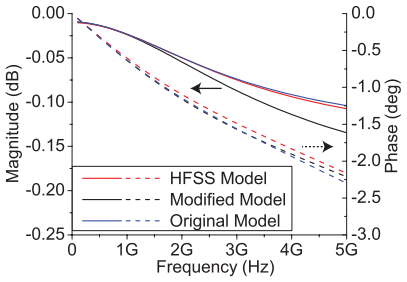

Fig. 9. Transmission S-parameter results

TABLE III
PRIMETIME MODEL COMPARISON

Body resistance (Ω)		0	1K	5K	10K
Multi-TSV model	Power (μW)	96.47	96.32	93.64	89.65
	Timing (ps)	54.0	45.5	40.0	39.1
Ignoring C_{Si}	Power (μW)	96.47	93.64	93.67	89.87
	Timing (ps)	54.0	45.7	39.7	38.6
Ignoring C_{MOS}	Power (μW)	70.24			
	Timing (ps)	37.7			

Table III. The results show ignoring the substrate coupling capacitor gives a good estimation of the TSV coupling.

B. Full-chip Analysis Strategies and Flow

For full-chip analysis, we first extract TSV locations and parasitic information for each die separately from Cadence Encounter. For a victim, we choose 50 closest aggressor TSVs and calculate the capacitance using equations in Section III. However, to simplify the simulation, we ignore the aggressor if the capacitance of an aggressor is below 0.01fF. Then, we generate an RC network between the victim net and all other 2D and 3D aggressors. We generate a SPICE netlist based on our multi-TSV model as well as a top-level SPEF file that contains the TSV parasitic information. After a netlist is created, we run HSPICE simulation on the netlist. Finally, we extract the coupling noise on a victim net from HSPICE. Note that in the flow reported in [1] and [9], the noise numbers are measured at every nodes on a single net, and the coupling noise voltages are all added into the total noise. Therefore, the total noise measured is several times larger than it should be. In our flow, we only report the maximum noise measured in each nodes for a single net so that the noise value is not counted twice. We perform this on every net in the design and add all the maximum noise values measured as the total noise. Fig. 10 shows our noise analysis flow. We use Primetime to read the parasitic information for each die and TSV coupling information in incremental mode and then perform static timing and power analysis.

Since TSV parasitics depend on the voltage of the TSV net, it is difficult to estimate the arriving time of each net. Therefore, we use different strategies for worst-case and average case analysis. For worst-case analysis, we assume all the aggressor signals are arrived at the same time. They all have the same switching waveform from 0V to VDD. Then, we measure the maximum voltage on the victim net. We use TSV MOS capacitance measured when the TSV voltage is 0V since the depletion region width is minimum. For average case study, we choose a time window that is no larger than the target clock period. We use the TSV MOS capacitance values measured at half of the VDD. Moreover, some aggressors may not even switch during the same clock cycle. Since not all aggressor nets are switching at the same time, we randomly locate the start time of the aggressor signals within the time window, and we choose a switching activity

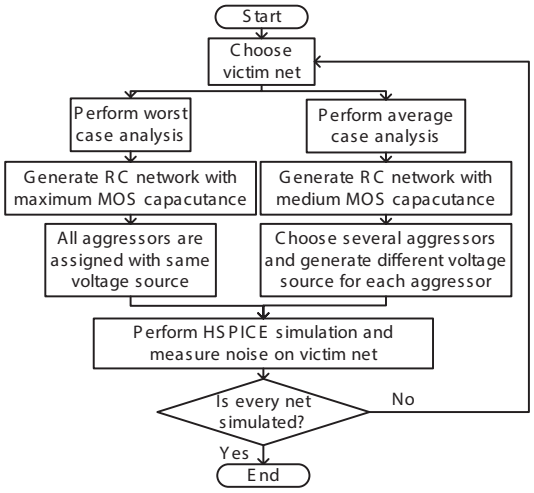

Fig. 10. Full-chip noise analysis flow

TABLE IV
WORST-CASE AND AVERAGE CASE COMPARISON

	Worst-case	Average case
Time window	Clock period	$\leq$ Clock period
Start time	Fixed	Randomly chosen
Aggressor activity	1	0 to 1
Switching direction	Rise	Rise and fall
Noise definition	Maximum voltage	Peak-to-peak voltage

factor and randomly pick aggressors that are switching during the time window. After running HSPICE, we measure the peak-to-peak voltage difference on a victim TSV net. Table IV lists the comparisons between worst-case and average case analysis, and Fig. 11 shows the victim voltage waveform in different cases.

C. Designs Specification

We use a 64 point FFT design to perform coupling analysis. It has 47K gates and 330 TSVs. The target clock frequency is 200MHz. We implement this design on a 2-die 3D IC using 45nm technology with 5 metal layers. The TSV landing pad size is $5\mu m$ and TSV radius is $2\mu m$. Each TSV has a $1\mu m$ keep out zone to ensure all the logic cells are outside of the TSV depletion region that their threshold voltage and performance will not be affected by the depleted substrate. The total footprint area of the design is $380\mu m \times 380\mu m$, and the total TSV area is $16170\mu m^2$, which is 11.2% of the total area. We show our important design information in Table V. We use different placement strategies to implement this design. During regular placement, we place TSVs in an array that TSV pitch is $19\mu m$. After we fix the locations of the TSVs, we use our own in-house 3D placer [12] to obtain the final placement and use Cadence Encounter to route the design. For irregular placement, we treat TSVs the same as other logic cells. Then we use Cadence Encounter to refine the placement and route the design. The minimum TSV-to-TSV pitch in irregular placement is $11\mu m$. Fig. 12 shows the die shots and TSV landing pads are highlighted.

D. Worst-case Analysis

We compare traditional 2-TSV model with our multi-TSV model in full-chip level. The TSV is $2\mu m$ in radius and has $0.5\mu m$ liner. For a fair comparison, we assign the same number of aggressor TSVs around a victim TSV. We consider the field and silicon effects and compare the total coupling capacitance and resistance values using

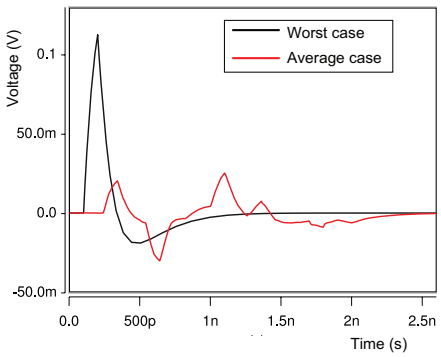

Fig. 11. Victim voltage waveform comparison

TABLE V
DESIGN SPECIFICATIONS

Placement style	Irregular	Regular
Minimum TSV pitch (μm)	12	19
Footprint	$380\mu m \times 380\mu m$	
TSV count	330	
TSV area (μm^2)	16170	

different models. Fig. 13 shows the noise comparison between 2-TSV and multi-TSV model. As shown from the results, We see over-estimation in calculating the coupling capacitance in the 2-TSV model (C_{si}). Thus, it also underestimates the substrate coupling resistance value (R_{si}). Therefore, the 2-TSV model overestimates the coupling noise. Since our design is operating at 200MHz, TSV MOS capacitor dominates the coupling between TSVs within this range. However, using the 2-TSV model gives a total TSV net noise of 139.4V, which is 48.0% larger than total noise measured (94.2V) using our multi-TSV model.

Compared with 2D nets, 3D TSV nets heavily suffer from coupling noise and delay for the following reasons: (1) It is difficult for current technology to fabricate TSVs with very small dimensions and there's a limitation on thinning the substrate. Therefore, TSV has large MOS capacitance; (2) TSVs are placed denser in future technology nodes, which increases TSV coupling components; (3) The permittivity of the inter-layer dielectric (ILD) between 2D interconnections is very low ($3.9\varepsilon_0$). However, the silicon substrate that is covering around the TSV has a very high permittivity ($11.9\varepsilon_0$), which results in large TSV coupling capacitance. In our regular and irregular placement designs, the largest coupling noise (0.75V) is measured on the TSV net. These large coupling voltage can cause logic failures.

Compared with regular placement design, irregular placement design is showing 5% larger coupling noise. In irregular placement design, minimum distance between 2 TSVs is smaller, and the number of TSV neighbors within a certain distance is larger. Therefore, irregular placement suffers more TSV coupling that results in a large timing degradation. However, since the regular placement is a special case of irregular placement, it is possible to find a better placement using irregular TSV locations.

E. Average Case Analysis

We use the average case algorithm in Section IV-B for TSV-to-TSV coupling noise study. In average case, the victim TSV suffers much smaller peak-to-peak noise due to the following reasons: (1) Not all the aggressors switch in one clock period, and those switching aggressors do not start voltage transition at the same time; (2) Due to the load capacitance, many aggressor nets have higher transition

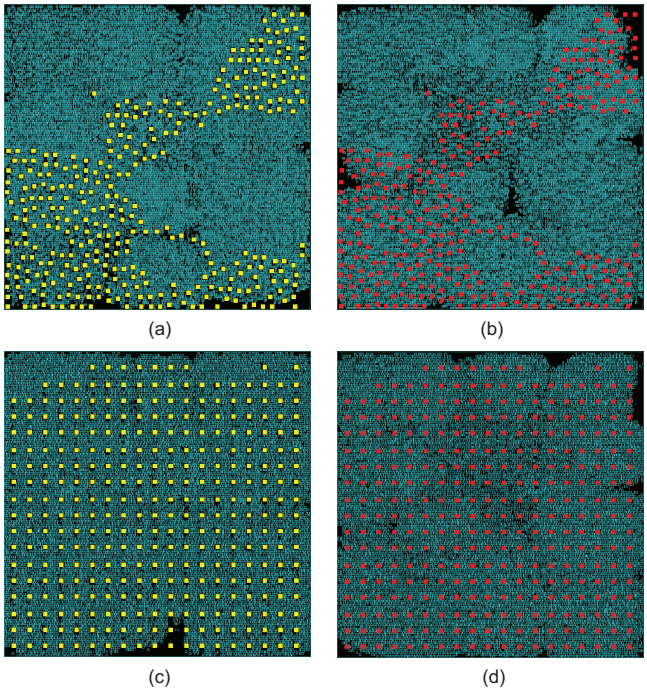

Fig. 12. Design layout. (a) and (b) are bottom and top die of irregular placement design, respectively, (c) and (d) are bottom and top die of regular placement design, respectively

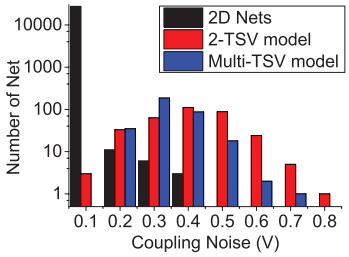

Fig. 13. Noise distribution comparison of TSV-coupling models

time, especially for low-power designs running at long clock-period with low supply voltage. Table VI compares the two analysis in various metrics, and table VII compares the runtime. The average case analysis provides an estimation on average noise level on TSV nets when multiple aggressors with different voltage waveforms are considered. The results show that both the switching activity and the signal slew have a large impact on the noise results on the TSV nets.

F. Full-Chip Substrate and Field Impact

In this section, we see the impact of field and substrate effect. To do this, we disable each field and silicon effect one by one while keeping other values the same. We compare how severe the field and silicon effect is on final results. The TSVs are $2\mu m$ in radius and have $0.2\mu m$ liner. Depletion region effect decreases the MOS capacitance especially for designs with thinner oxide liner. Without considering the depletion region, TSV MOS capacitance is overestimated. In addition, in full-chip, depletion region not only affects the signal integrity and performance, but also alters the performance of logic cells around TSVs.

Moreover, ignoring substrate resistors and capacitors are also a pessimistic estimation on coupling noise. The discharging path

TABLE VI
AVERAGE CASE AND WORST-CASE COMPARISON ON TOTAL TSV NET NOISE (V)

	Activity	Slew (ns)	Regular	Irregular
Average case	0.2	0.1	26.51	24.65
	0.5	0.1	39.61	35.37
	0.2	0.5	14.04	14.62
Worst-case	1.0	0.1	139.01	132.44

TABLE VII
SIMULATION RUNTIME (MIN) COMPARISON

Placement style		Irregular	Regular
Average case	Only TSV nets	14	12.5
	All nets	387	367
Worst-case	Only TSV nets	15	13.5
	All nets	389	369

TABLE VIII
SILICON AND FIELD EFFECTS ON THE TOTAL TSV NET NOISE (V)

Placement style	Irregular	Regular
no depletion region	153.7	145.9
no body resistance	144.9	138.9
no E-field distribution	146.3	138.9
all-effects-included	139.0	132.4

TABLE IX
SILICON AND FIELD EFFECTS ON TSV-INDUCED DELAY (NS) AND POWER (μW) INCREASE

Placement style	Irregular		Regular	
	Delay	Power	Delay	Power
no depletion region	0.85	13.53	0.98	13.66
no body resistance	0.78	12.54	0.90	12.63
no E-field distribution	0.79	12.68	0.91	12.77
all-effects-included	0.79	12.68	0.91	12.77

through a substrate is critical to limit the peak noise on the victim and it also affects delay and power consumption. In worst-case analysis, we overestimate the coupling noise when we do not consider the E-field distribution around the victim TSV. Also, without considering the electrical field distribution, the noise is over-estimated because aggressors are seeing the whole TSV MOS capacitance. However, each aggressor mainly affects the victim charges only on the side that is facing it. Table VIII and Table IX details chip-level field and silicon effects comparison.

V. TSV-TO-TSV COUPLING NOISE REDUCTION

In this section, we propose a TSV protection method using guard rings to reduce the coupling. We show the effectiveness of this method on our FFT design.

A. Guard Ring Model

Since the silicon substrate provides a discharging path to the ground, we make the discharging easier by reducing substrate-to-ground resistors (R_{Sig}). We use a grounded ring proposed in [4] in the diffusion layer with P+ doping to build a short discharging path for the victim TSV. In [4], the guard ring is meshed into many cells, and each cell contains 6 to 12 components that makes it unsuitable for full-chip analysis. Therefore, we propose a new guard ring model. The proposed guard ring structure is shown in Fig. 14(a). We use Synopsys Raphael to extract the substrate resistance to the ground. We list the detailed extracted results in Fig. 14(b), with different edge-to-edge distance and guard ring width. Small ground resistance leads to a strong connection between the substrate around TSVs and the ground net can help shield coupling noise introduced by TSV-to-TSV coupling. Due to the increased ground capacitance, it introduces little timing degradation on TSV nets. However, the distance between TSVs and the guard ring does not affect much on the ground resistance. This is because larger edge-to-edge distance between TSVs and guard ring creates a longer discharging path but it also results in a larger guard ring.

The ring width shows a large impact on the ground resistance. Thus, the coupling noise reduces further if the width of the guard ring is increased. Plugging our guard ring model to our TSV-coupling model, we perform transient analysis on the 3-TSV test structure. We see that the guard ring shows 47.5% noise reduction on a TSV net. Compared to other TSV shielding techniques, such as ground TSV insertion, this method introduces a very small area overhead because the dimensions of a diffusion layer is much smaller than ground TSVs. In [1], the authors use eight TSVs around the victim to shield the noise, which introduces significant area overhead. The TSVs and logic cells must be re-placed to solve the overlap problem introduced by adding ground TSVs. The authors had to increase the die area to complete the placement and routing. However, in our approach, only minor changes are need to be made into the design including refine placement and incremental routing. Therefore, we save significant total design time especially for large designs with high density and large area.

B. Optimization Flow

In [1], the authors proposed a TSV shielding technique that requires large changes in the design flow. The path impedance between TSVs are chosen as the reference of the noise coupling. However, this estimation is not accurate for the following reasons: (1) Not only neighbor TSVs, but also the 2D nets are aggressors for a victim TSV. (2) TSV coupling path impedance and the coupling noise is not in a linear relationship. (3) Since TSVs that are far from the victim can also impact significantly although the path impedance is small, the number of TSV neighbors must be taken into consideration. Since the guard ring strategy do not require a large change on the layout, we use the following strategy to perform the noise optimization: First, we perform a worst-case analysis on the full-chip design and obtain the noise levels on each TSV. Then, we sort the TSVs according to the noise levels and start protecting the TSVs by adding a guard ring with different widths. To minimize the area overhead, we set a minimum noise threshold for a victim that no guard ring is necessary. Above the threshold, TSVs that suffer larger coupling noise is designed with a larger guard ring. We set a maximum limit on the guard ring width that no overlap is in the layout. Fig 15 shows the layout with TSV and guard ring highlighted after we perform the optimization on the our regular placement and irregular placement designs.

C. Full-Chip Noise Reduction Results

Adding the guard rings, we perform our worst-case analysis on the new layout. Table X shows the noise optimization results. The total noise reduction on the 3D nets is by 27.3% with only 3.86% area overhead by guard rings. The delay of the design also increases little due to the increased substrate ground capacitance. Our results show that our approach is very effective in TSV noise reduction with minimum area overhead.

We compare our results with TSV shielding. From Table XI, both optimization methods are effective in TSV-to-TSV noise reduction, but our approach uses smaller area. The major drawbacks for the TSV shielding are the following: (1) It requires large additional area

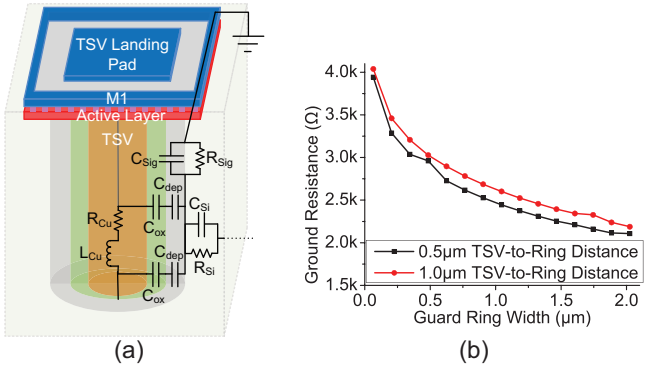

Fig. 14. Guard ring impact: (a) our proposed guard ring structure, (b) extracted substrate ground resistance

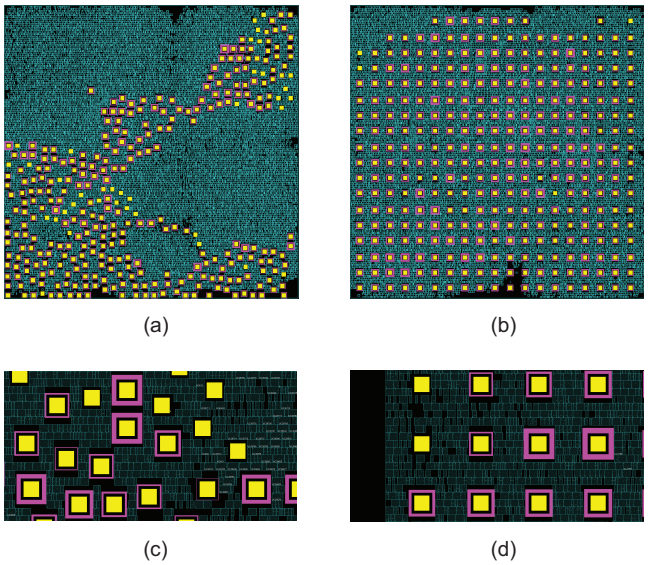

Fig. 15. Noise-optimized design layout. (a) and (b) are bottom die of irregular and regular placement design, respectively, (c) and (d) are zoom-in shots

for GND TSVs. (2) TSV shielding needs to enlarge the footprint area and perform a redesign to achieve good noise reduction. (3) TSV shielding requires more design time compared with guard rings that is easy to implement. (4) The GND TSVs also introduce a large capacitance to the victim TSVs, which is much larger than the ground capacitance introduced by the guard ring. Therefore, designers need to perform static timing check for the design again. In short, we conclude that our approach is more useful and convenient than the ground TSV insertion.

VI. Conclusion

In this paper, we studied the TSV-to-TSV coupling and its impact on 3D IC. We proposed a compact TSV model that can be applied to multi-TSV coupling analysis that considers field and substrate effects. From our simulations, we show that our multi-TSV model is highly accurate compared with 3D field solver. We find that depletion region, substrate impedance, and E-field distribution effects are critical in TSV modeling. To accurately perform full-chip analysis, we proposed worst-case and average case analysis methods and developed algorithms. To alleviate the TSV-to-TSV coupling noise, we proposed a novel model and a method to protect the victim TSVs by grounded

TABLE X
Noise reduction results on two design styles

Placement style	Irregular	Regular
Total noise on TSV net (V)	101.1	96.5
Noise reduction	27.3%	27.1%
TSV-induced delay (ns)	0.81	0.93
TSV-induced power (μW)	12.75	12.86

TABLE XI
Full-chip noise reduction with guard ring vs TSV shielding

	Guard ring	TSV shielding in [1]
Protected TSV #	298	118
Initial TSV size (μm^2)	49	49
Protected TSV size (μm^2)	68.89 to 121	361
Initial footprint	$380\mu m \times 380\mu m$	$402\mu m \times 402\mu m$
Final footprint	$380\mu m \times 380\mu m$	$421\mu m \times 421\mu m$
Noise reduction	27.3%	42.04%
Area overhead (μm^2)	11053 (7.65%)	42598 (26.4%)

active region. Our analysis results show that this optimization method can reduce the coupling noise up to 27.3% with the maximum area overhead by only 7.65%. We conclude that our optimization method is very effective, easy to implement and area efficient.

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