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VLSI-Inspired Design Automation for Scalable Power Electronics Layout Optimization

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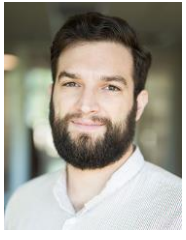

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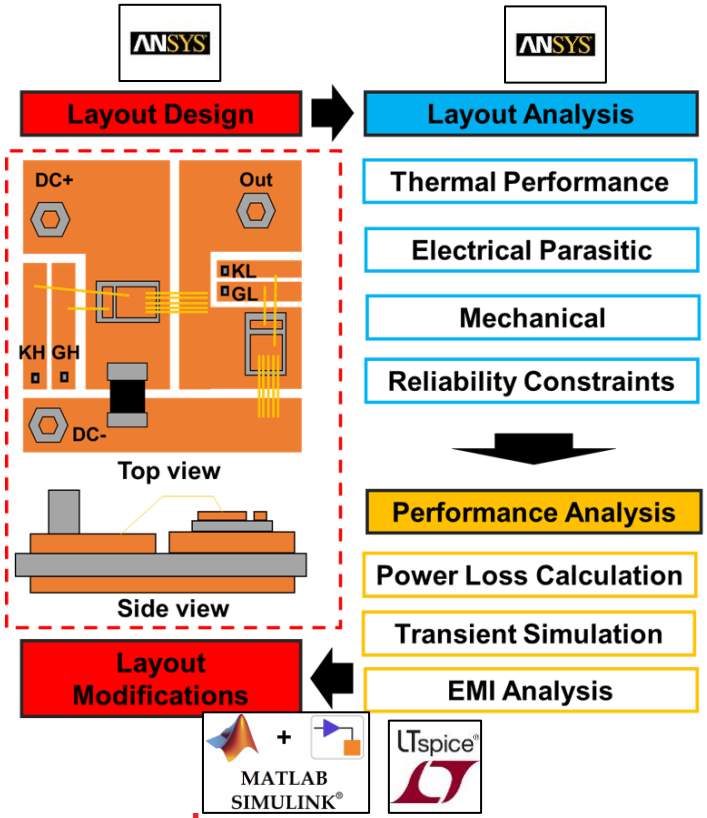
Outline

- Background and Motivation
- Electronic Design Automation (EDA) for Power Electronics
- Proposed EDA Tool
  - Overview
  - VLSI Techniques Used
  - Results
- EDA Toward Converter Design
- Conclusion

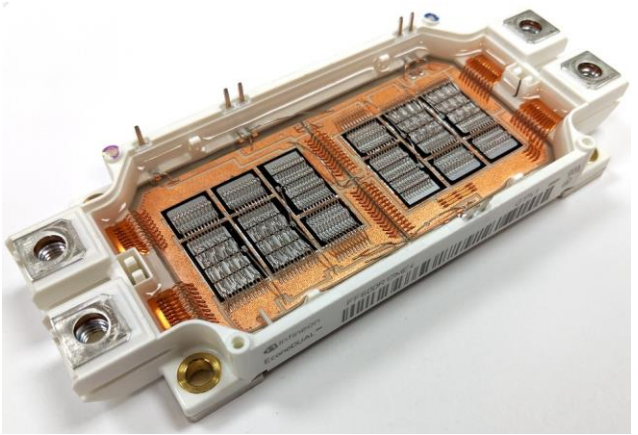
Background and Motivation

Power Module Design



Traditional Multi-Chip Power Module (MCPM) Design:

- Multidisciplinary
- Employs multiple tools
- Computationally expensive and iterative



The field of Very Large-Scale Circuit Integration (VLSI) has developed many techniques for solving similar problems

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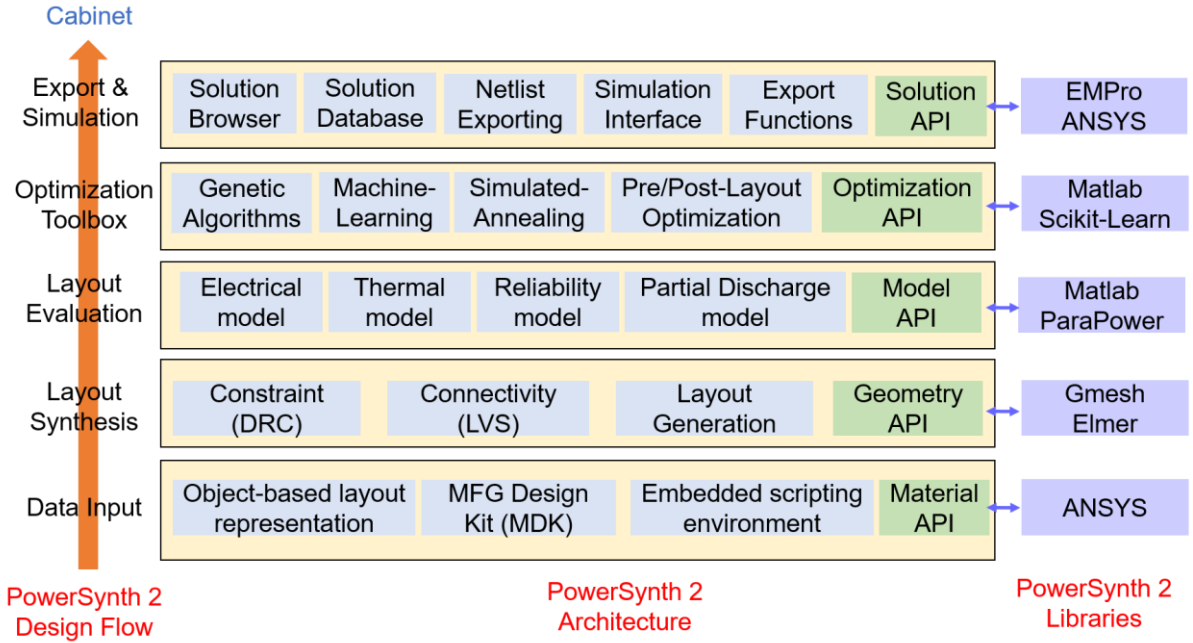
PowerSynth Introduction



- EDA tool MCPM design
- Multi-objective layout optimization
- Reduced order models
- Pareto-front of tradeoffs
- Design export

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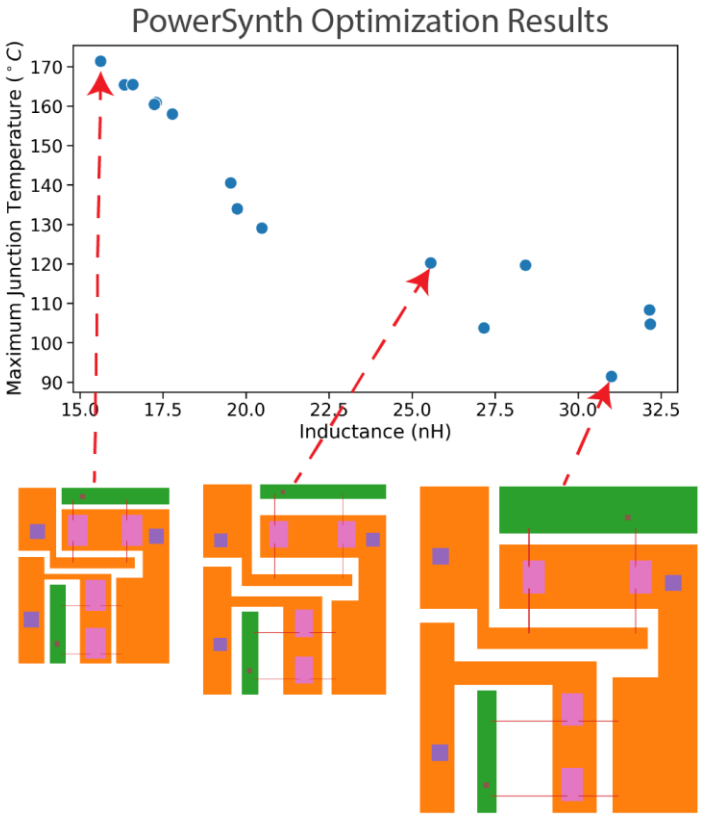
Expanding PowerSynth Results

- PowerSynth optimizes for tradeoffs in :
  - Electrical performance
  - Thermal performance
  - Mechanical reliability
- Maintains design intent by altering trace geometry and device positions

Automatically synthesizing module artwork for given design criteria would lead to an expanded solution space in shorter time



PowerSynth optimization results with selected layouts from the Pareto frontier shown to scale

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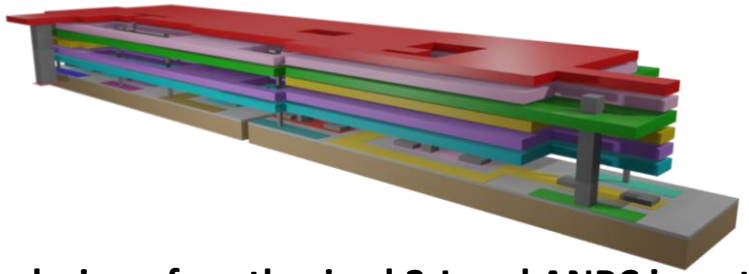
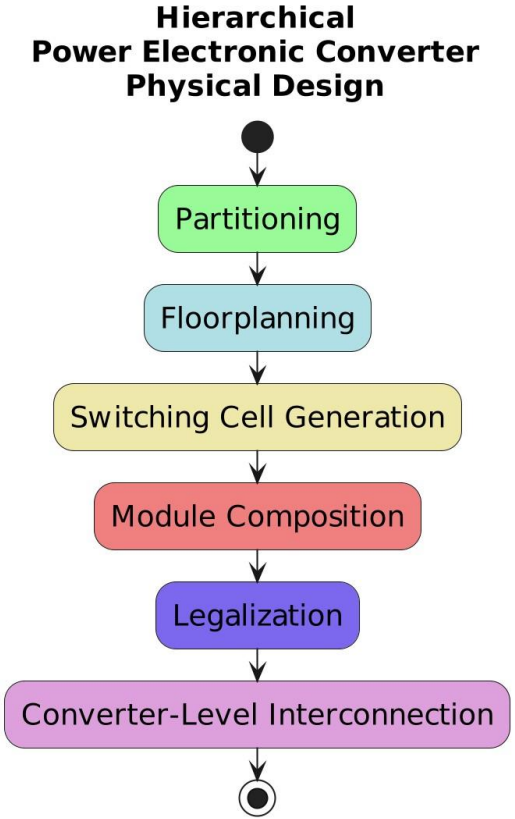
Proposed EDA Tool

Proposed EDA Tool Overview

- Netlist to layout
- Annotations drive:
  - Terminal locations
  - Device count/rating
  - Placement, routing, and modularization parameters
- Synthesizes modules and their interconnects to hierarchically form converters
- Export designs as 3D models or PowerSynth projects



3D rendering of synthesized 3-Level ANPC inverter from two modules with laminated bus bar interconnects



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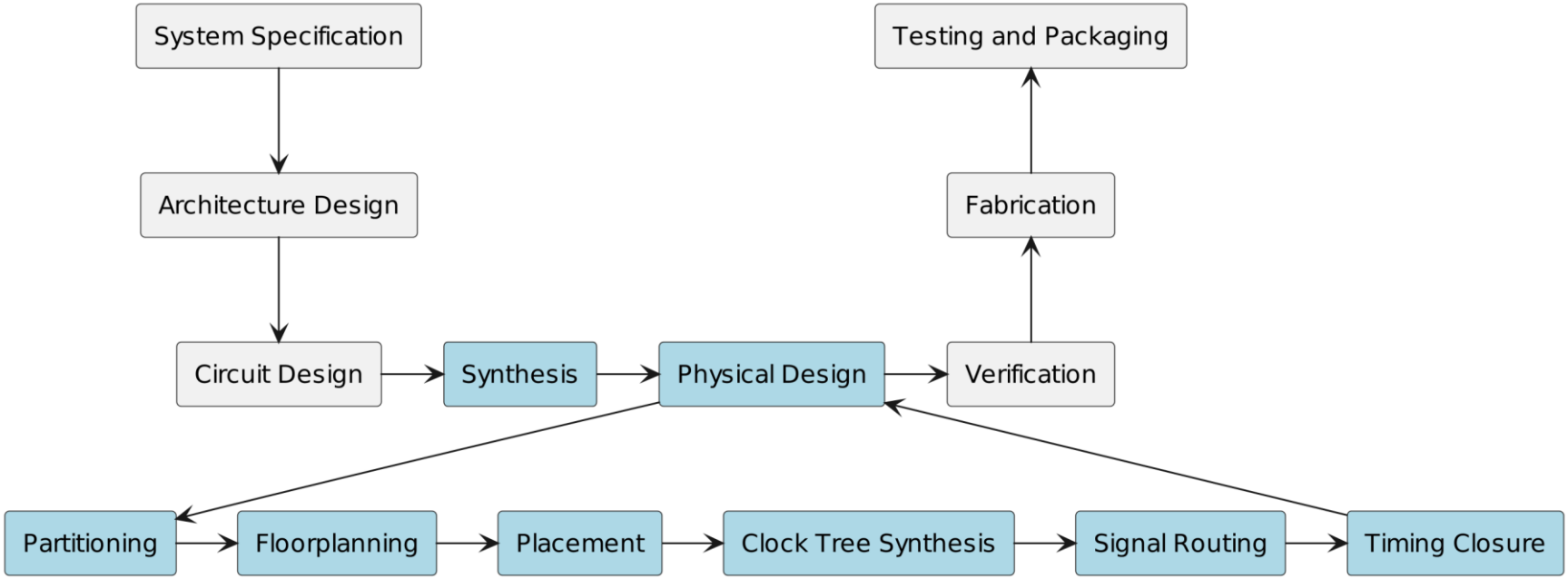
VLSI Design Flow



VLSI physical design steps

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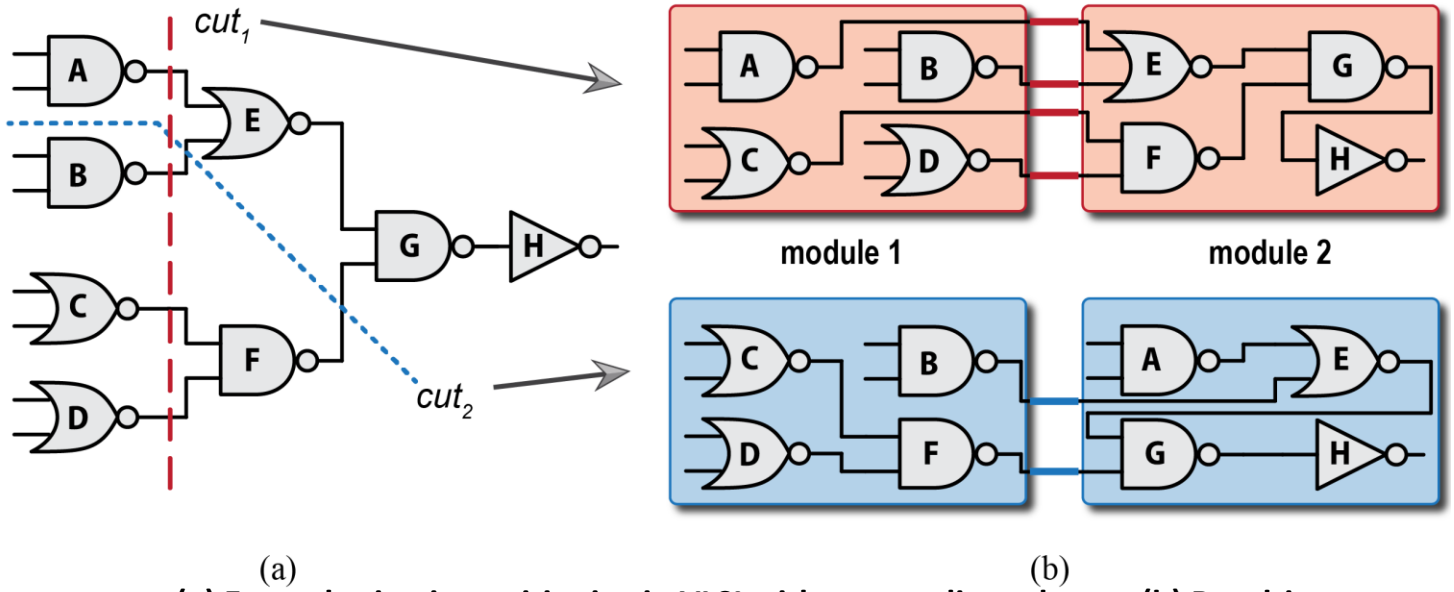
VLSI Inspiration: Circuit Partitioning

- Splits a larger circuit into smaller subcircuits or modules
- Aims to minimize the number of interconnects among modules



(a) Example circuit partitioning in VLSI with two cut lines shown. (b) Resulting modules formed by the cutlines in (a).

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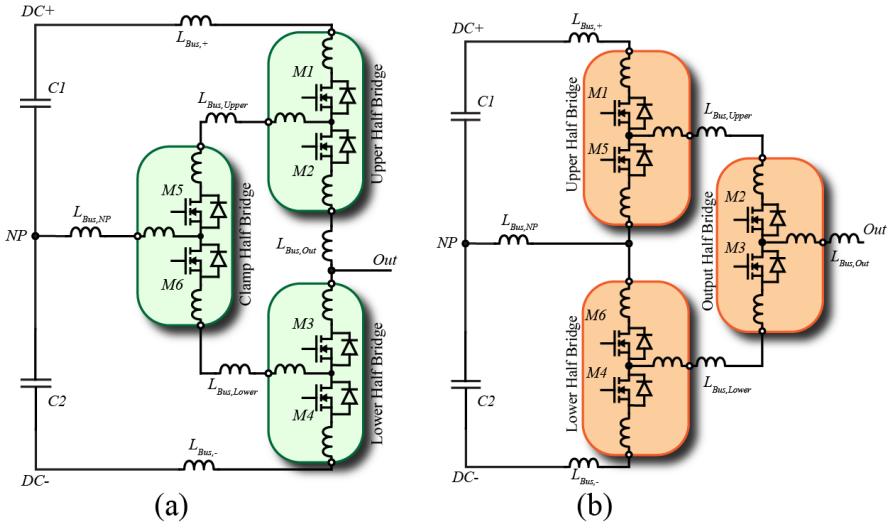
Circuit Partitioning for Power Electronics

- Power circuits can also be partitioned to realize different arrangements of modules
- Concept can be extended at different levels of hierarchy to realize non-standard module designs for larger converter designs



Various ways of partitioning a 3L-ANPC inverter into half-bridge modules (a, b) or two custom modules (c).

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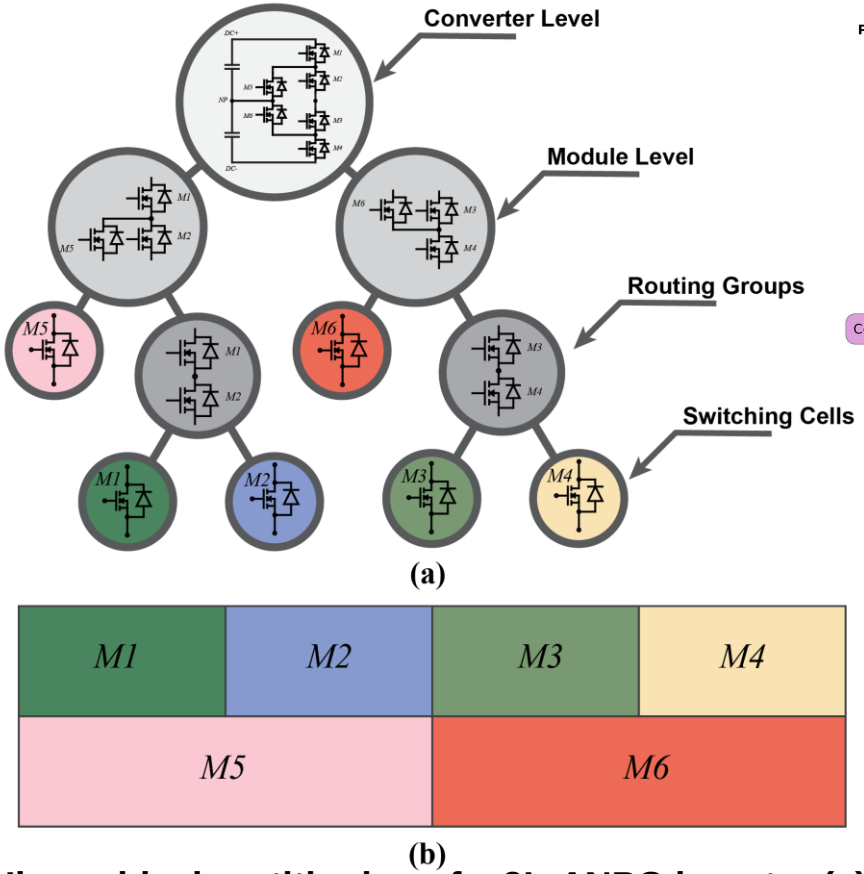
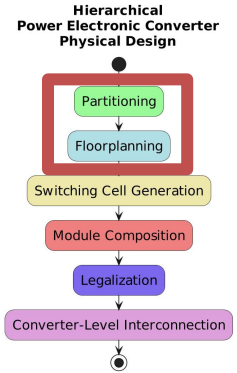
Floorplanning of Partitions

- Uses recursive Fidducia and Mattheyes (FM) bi-partitioning to split converter design down to switching cell level in *O(n)* time
- Minimizes the number of interconnects at each step
- Hierarchical tree structure can be used as binary slicing tree for floorplanning with associated design string specifying horizontal or vertical cuts at each level
- Module depth used to determine cutoff for routing/bus bars





Hierarchical partitioning of a 3L-ANPC inverter (a) with floorplan of switch positions (b)

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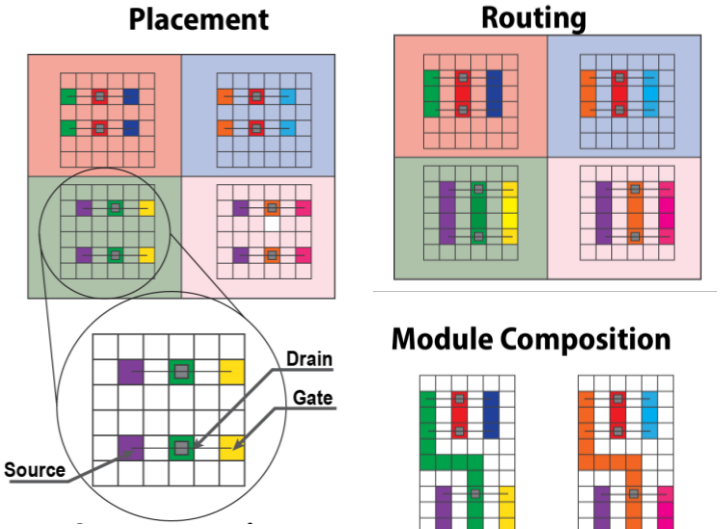
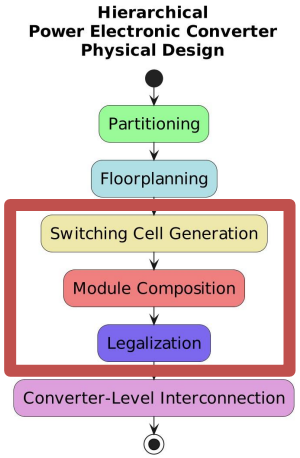
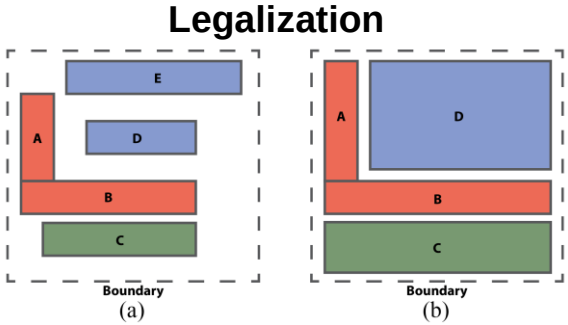
Building Modules and Determining Fitness

- Placement and routing techniques used to create routing groups and then modules
- Legalization minimizes geometry description while ensuring feasibility
- Simulated annealing employed to guide design string toward:
  - Routability
  - Path length between selected terminals
  - Overall footprint







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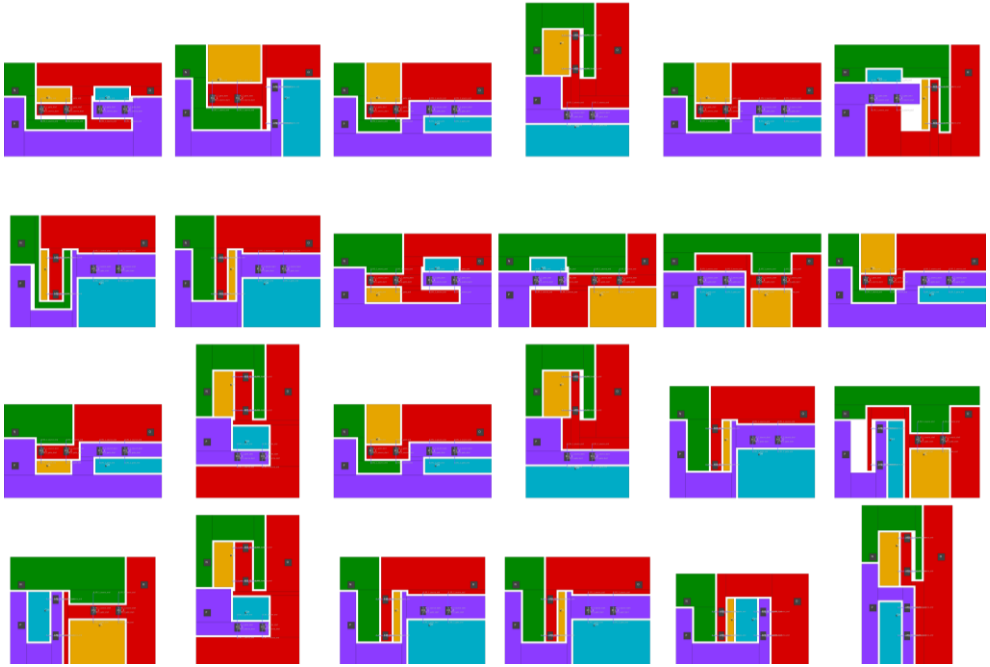
Example: Half-Bridge Layout Synthesis

- Half-bridge module layout with 2 paralleled devices per switch position
- Synthesis constraints:
  - DC+ and DC- on left
  - AC output on right
  - Optimize for minimal wirelength from DC+ to DC- and footprint area
- 55 unique layouts synthesized in 18 minutes



Trace Net Color Key:
DC+ DC- AC_{Out} $Gate_{High}$ $Gate_{Low}$

24 variations of the half-bridge module layout synthesis example

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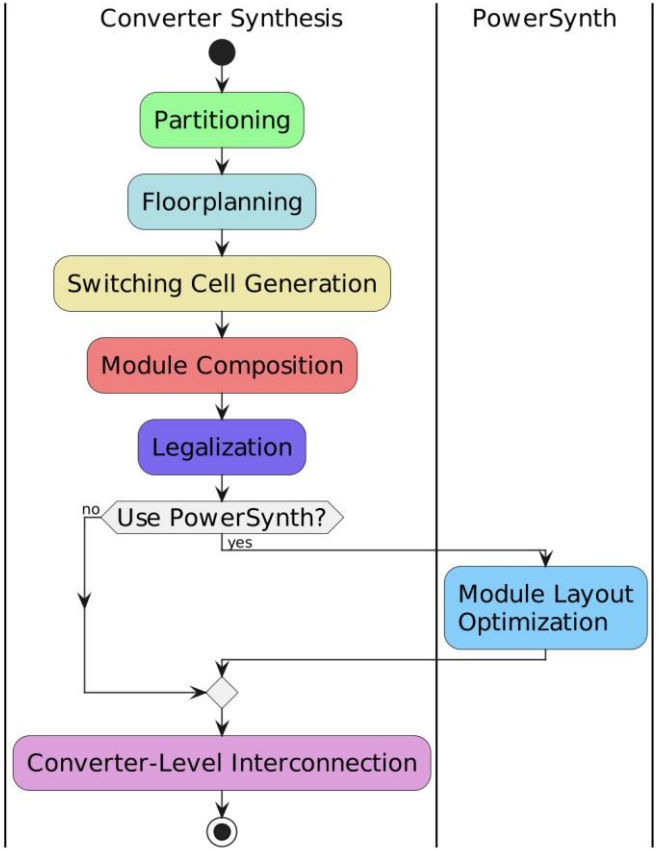
PowerSynth Integration

- Synthesizer excels at creating new layouts from minimal inputs
- However, lacks design optimization based on electrical and thermal models
- Integration with PowerSynth enables fast:
  - Generation and optimization of multiple layout variations for each synthesized design
  - Electrical and thermal tradeoff evaluation using tested models



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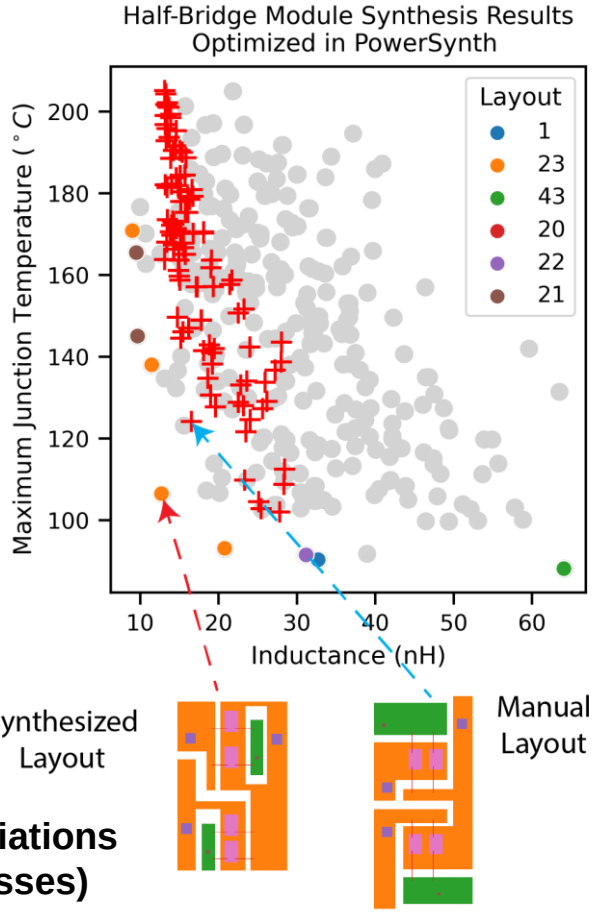
PowerSynth Integration Results for a Half Bridge Design

- Using PowerSynth:
  - Generate 15 layouts for each of the 55 synthesized designs (825 data points)
  - Compare with 100 variations of a single, manual design
  - Optimize for tradeoffs in max junction temperature and loop inductance (DC+ to DC-)
- Boundary conditions:
  - 10 W/device power dissipation
  - 150 W/m^2/K heat removal

Comparison of Pareto-optimal results for each type

Design Type	Inductance (nH)	Max Temperature (°C)
Manual	16.6	124
Synthesized	12.7	106



Graph Key: Synthesized layouts and variations (circles), Manual layout variations (crosses)

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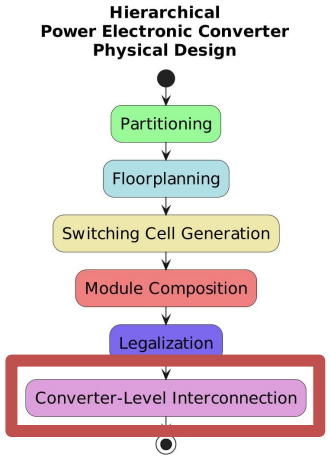
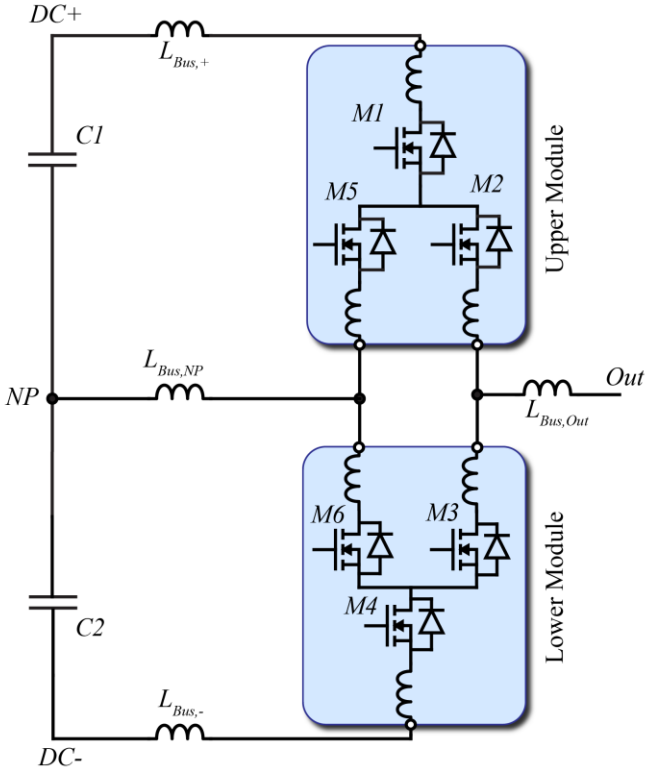
EDA Towards Converter Design

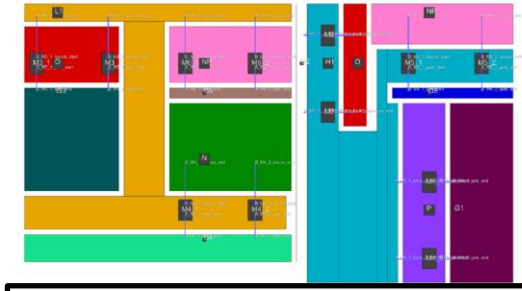
Converters from Synthesized Modules



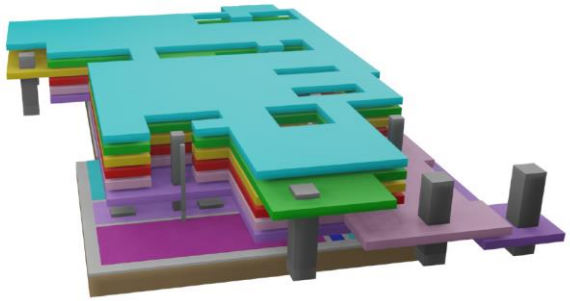


3L-ANPC inverter partitioned into two custom modules

Lower Module **Upper Module**



Selected Trace Net Color Key:
DC+ DC- AC_{Out} NP



Synthesized module layouts (above) and the laminated bus bar-structure interconnecting them (below)

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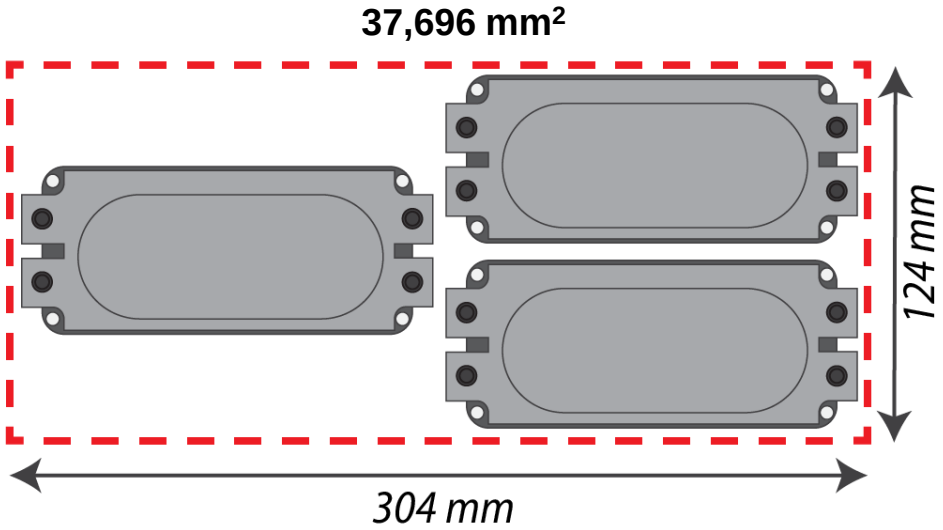
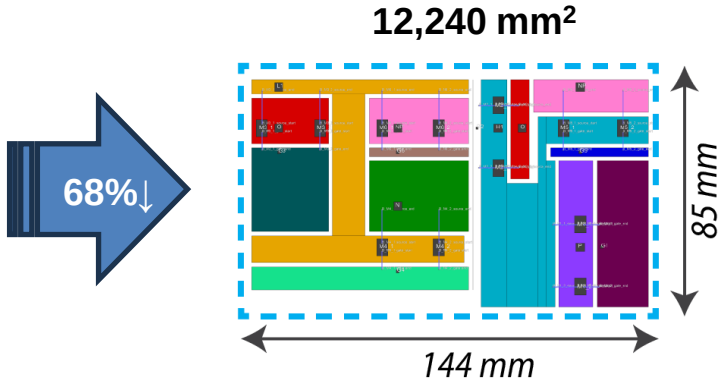
Potential for Area Reduction



3L-ANPC inverter from 3 standard 62 mm half-bridge module packages.



3L-ANPC inverter from 2 custom module layouts

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Conclusion

- Introduced a new tool for hierarchical power converter design inspired by VLSI techniques
  - Netlist to layout
  - Fast generation of original design artwork
  - Integration with PowerSynth for detailed optimization
- Using tool with PowerSynth produces richer solution space in less time than single manual design
- Hierarchical implementation provides inroads to high-density converter design automation

Thank you!