PowerSynth 2

Physical Design Automation for High-Density 2D/2.5D/3D Multi-Chip Power Modules

Yarui Peng

Assistant Professor

Computer Science and Computer Engineering

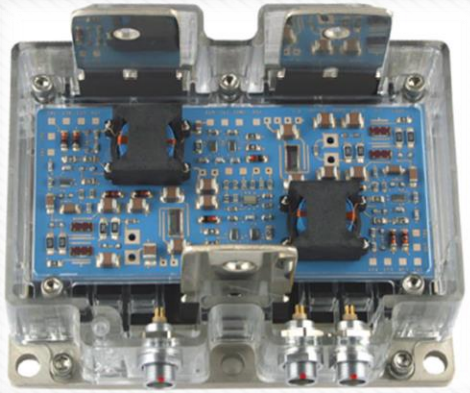
University of Arkansas

UNIVERSITY OF ARKANSAS

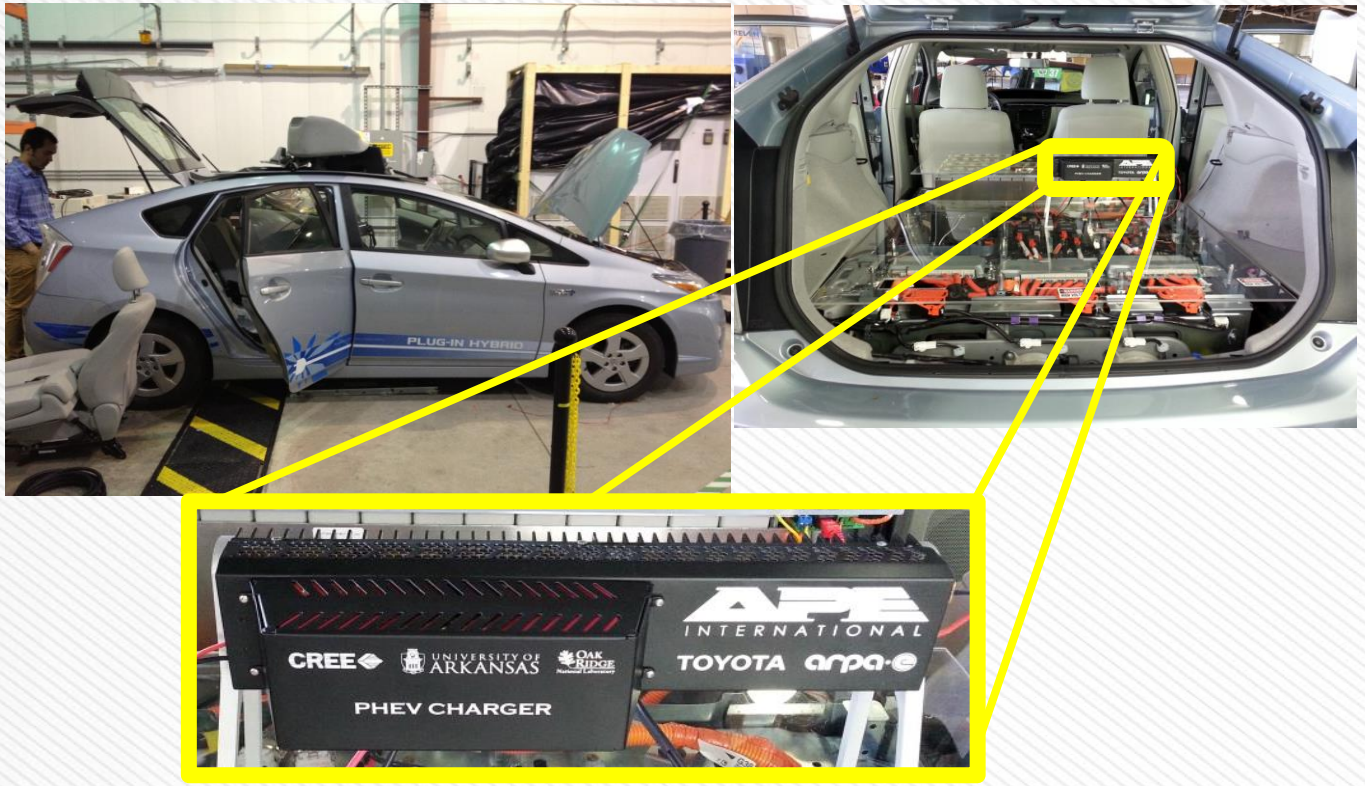
https://e3da.csce.uark.edu yrpeng@uark.edu +1 (479) 575-6043

Multi-Chip Power Modules

- **Foundation element of power converters**
- **Integrates power devices and control circuitry in a single package**
- **Wide Bandgap Devices (SiC/GaN)**
  - Increased power density
  - New packaging technologies
  - Heterogeneous integration



R&D 100 Award-Winning MCPM Design

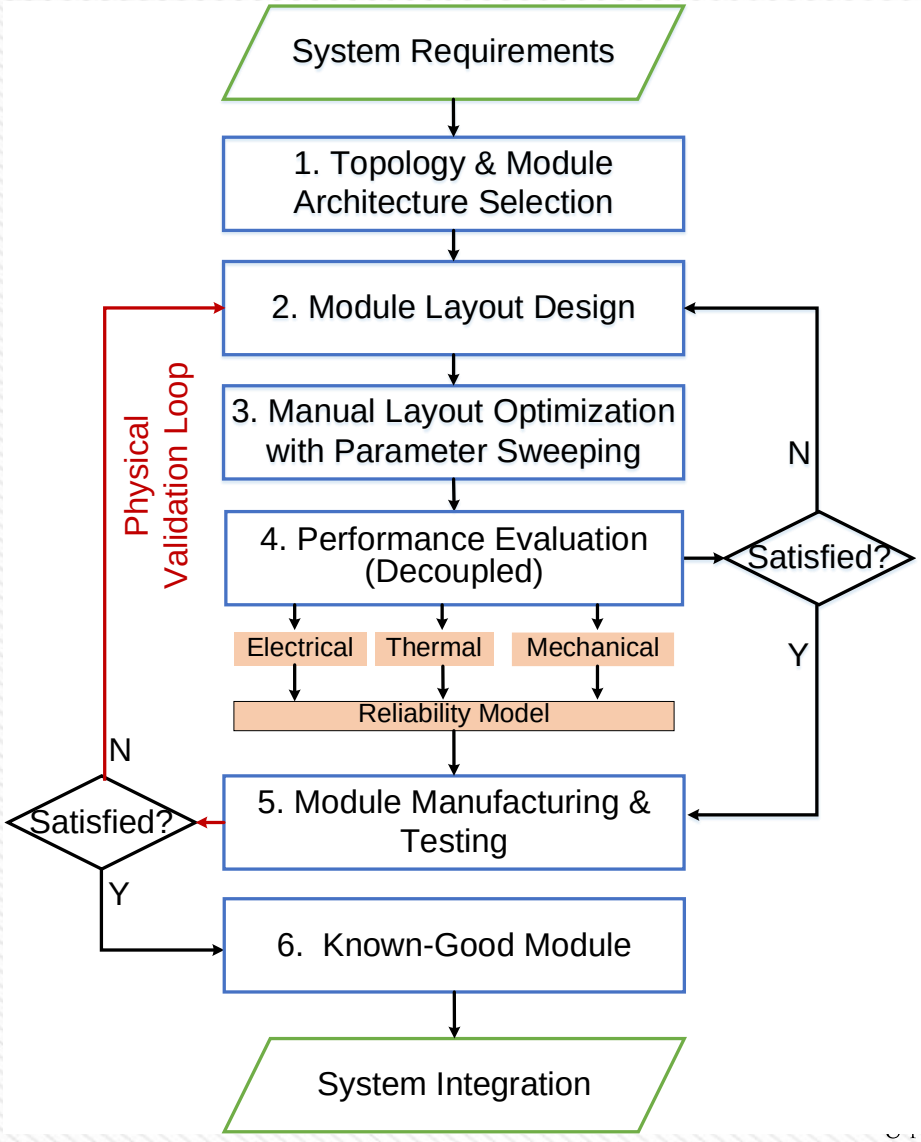


MCPM layout design complexity is increasing

UNIVERSITY OF ARKANSAS

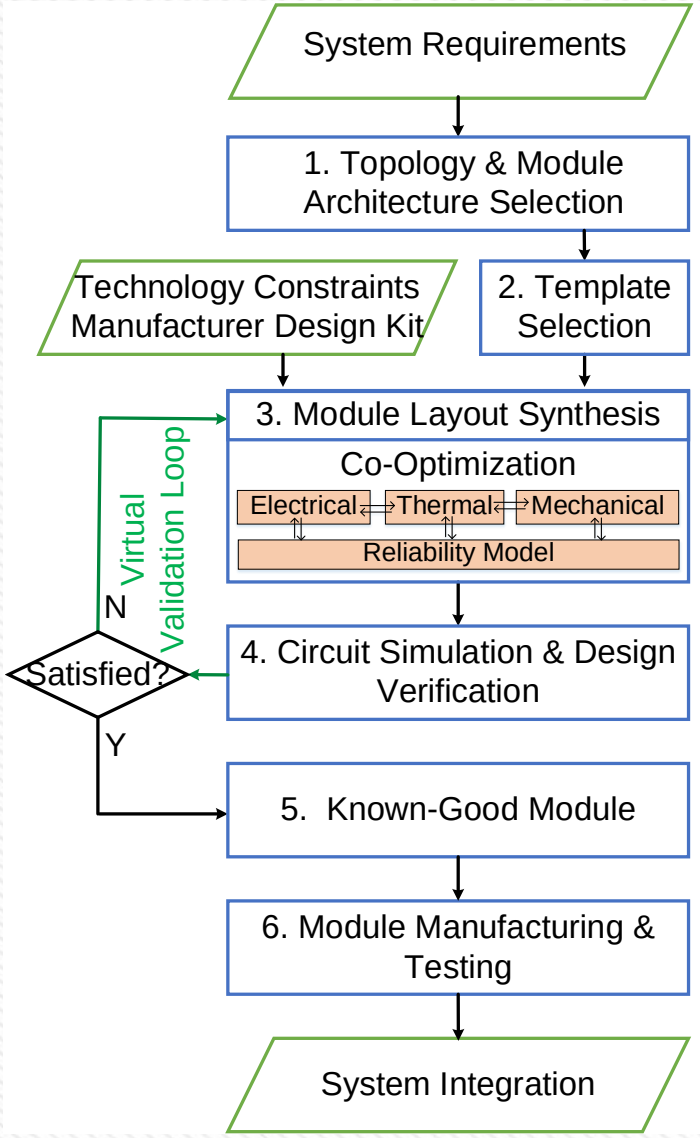
Traditional Design Flow

- **Traditional:**
  - Manual, iterative
  - Computationally expensive
  - Single solution at a time
  - Interaction with multiple FEA tools
  - No known-good module before fabrication and testing
  - Requires human expertise



Automated Design Flow

- **Automated:**
  - **Reduced time and cost**
  - **Reduced-order modeling**
  - **Large solution space at a time**
  - **Multi-objective optimization**
    - Electrical
    - Thermal
    - Mechanical
    - Reliability
  - **Known-good module before fabrication**



Power Module Design Automation Efforts

Methodology Features	Puqi Ning et. al. (2017)	Shuhei et. al. (2021)	Zhou et. al. (2022)
Initial layout	Simplified	Simplified	Not required (Template library & Netlist)
Layout generation method	Sequence pair	Parameter sweep	Integer linear programming & Block graph model
Layout types	2D	2D	2D
Scalability	N/A	N/A	N/A
Interconnection technology	Wire bond	Wire bond	Wire bond
DRC checking	Required	Required	Not required
Solution space	Limited	Limited	Limited
Hierarchical optimization	N/A	N/A	N/A
Performance evaluation	Discrete model	Finite element analysis	In-house model
Objectives	Area and power loop inductance	Power loop inductance & Junction temperature	Multiple loop inductance & Junction temperature
Reliability optimization	N/A	N/A	N/A
Optimization algorithm	Evolution (GA)	Evolution (NSGA II)	Evolution (NSGA II)

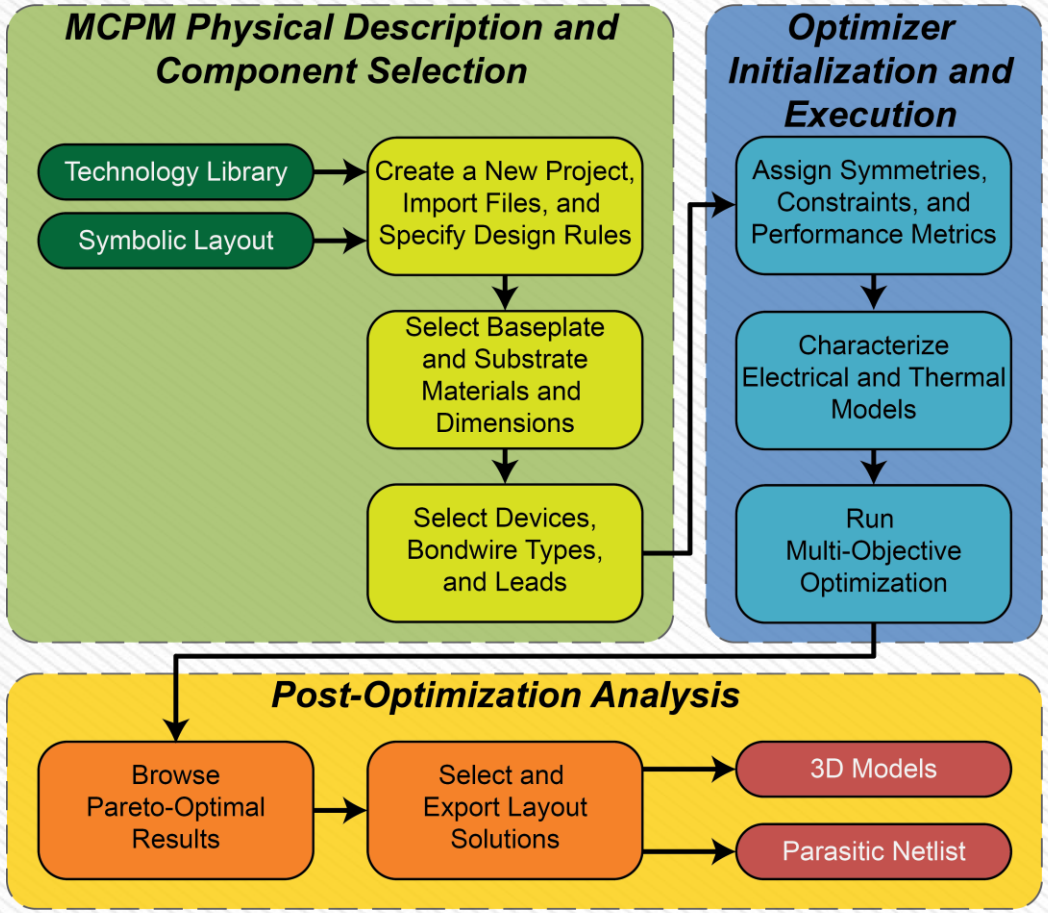
PowerSynth Motivations

❑ Features:

- Built-in technology library
- Symbolic layout input
- Matrix-based layout generation
- Reduced-order and fast electrical, thermal models
- Multi-objective optimization through GA
- Pareto-front solution browser
- Export solution to commercial FEA tools
- Post-layout optimization: filleting sharp corners
- Parasitic netlist extraction

❑ V1 Limitations:

- Fixed layer stack
- Simple 2D layout geometry only
- Limited solution space
- Requires iterative DRC



PowerSynth v1.1 work flow

PowerSynth Progression

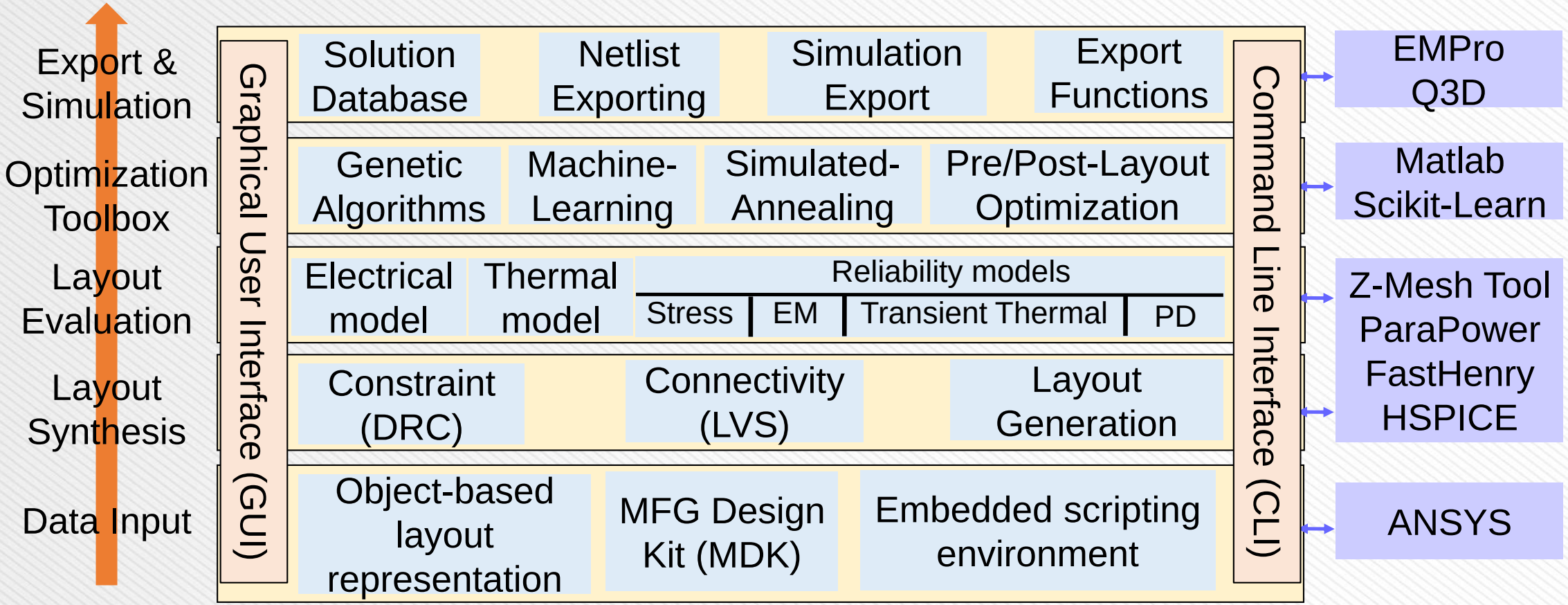
❑ PowerSynth Development Summary

- **Features**

▪ 2D layouts with complex geometry ▪ Constraint-aware, flat-level layout engine ▪ Heterogeneous components ▪ Multiple optimization techniques	PS v1.3/1.4
▪ All 2D/2.5D Manhattan geometries ▪ Hierarchical layout representation & optimization ▪ Larger solution space ▪ Hardware-validated optimization result	PS v1.9
▪ All 2D/2.5D/3D Manhattan layouts ▪ Both GUI and CLI for users ▪ Randomization and NSGAII ▪ Electro-thermal and reliability optimization ▪ Hardware-validated CAD flow	PS v2.0

UNIVERSITY OF ARKANSAS

PowerSynth 2 Architecture



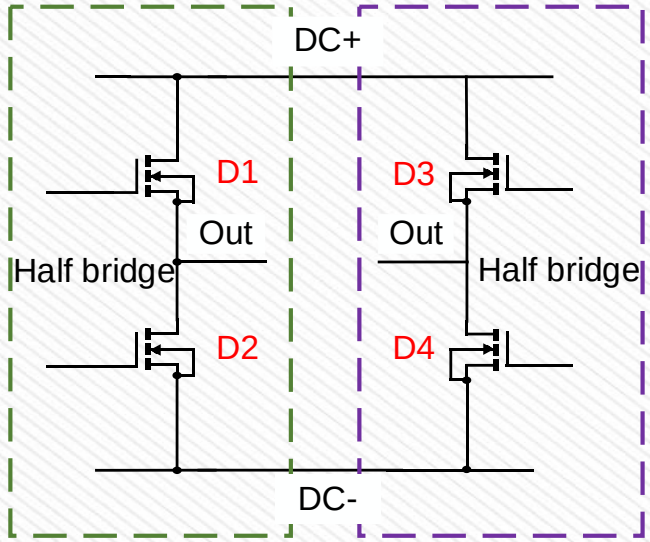
Design Flow Core: 2D/2.5D/3D Designs, Python 3.8, QT 5.12, Windows/Linux External Tools

[1] Imam Al Razi, Quang Le, Tristan Evans, H. Alan Mantooth, and Yarui Peng, “PowerSynth 2: Physical Design Automation for High-Density 3D Multi-Chip Power Modules”, (accepted) IEEE Transactions on Power Electronics, 2023.

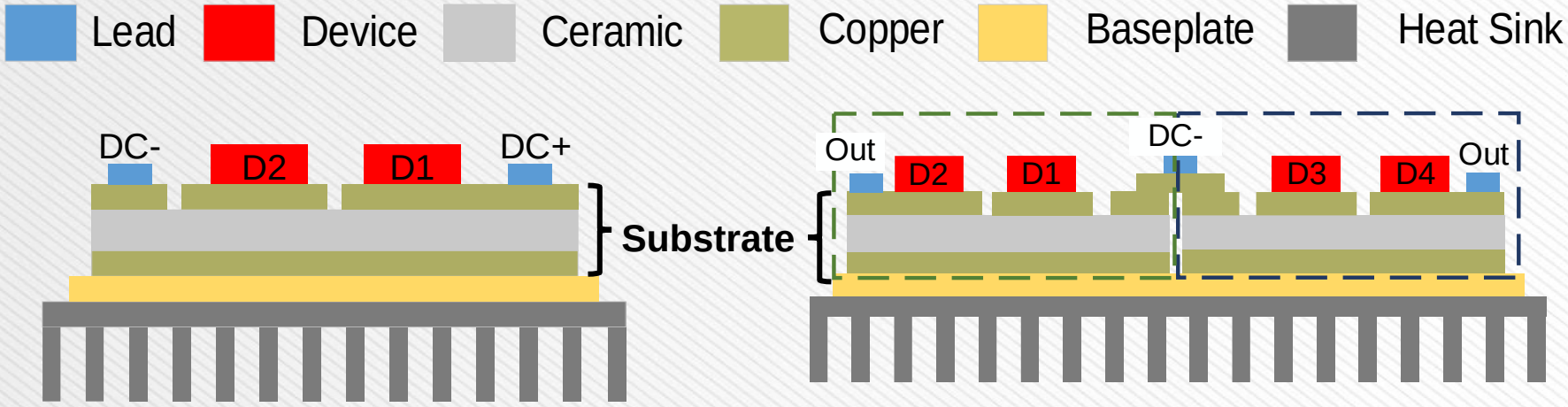
2D-2.5D-3D Module Definition

❑ Definition under PowerSynth scope:

- 2D: One device layer with routing layers on the same substrate
- 2.5D: Multiple 2D designs connected on a supporting 2D plane
- 3D: Multiple device layers stacked vertically on the same substrate

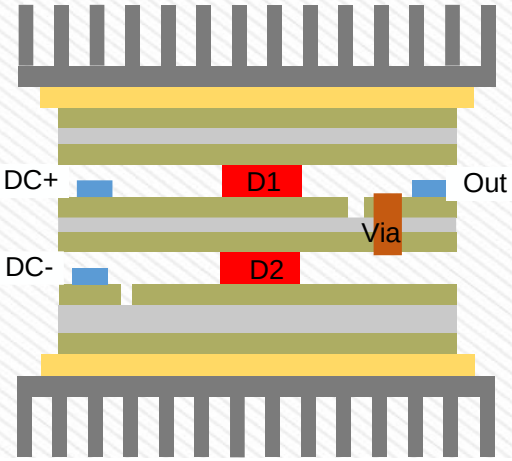


Circuit schematic of a full-bridge module



2D Half-bridge power module

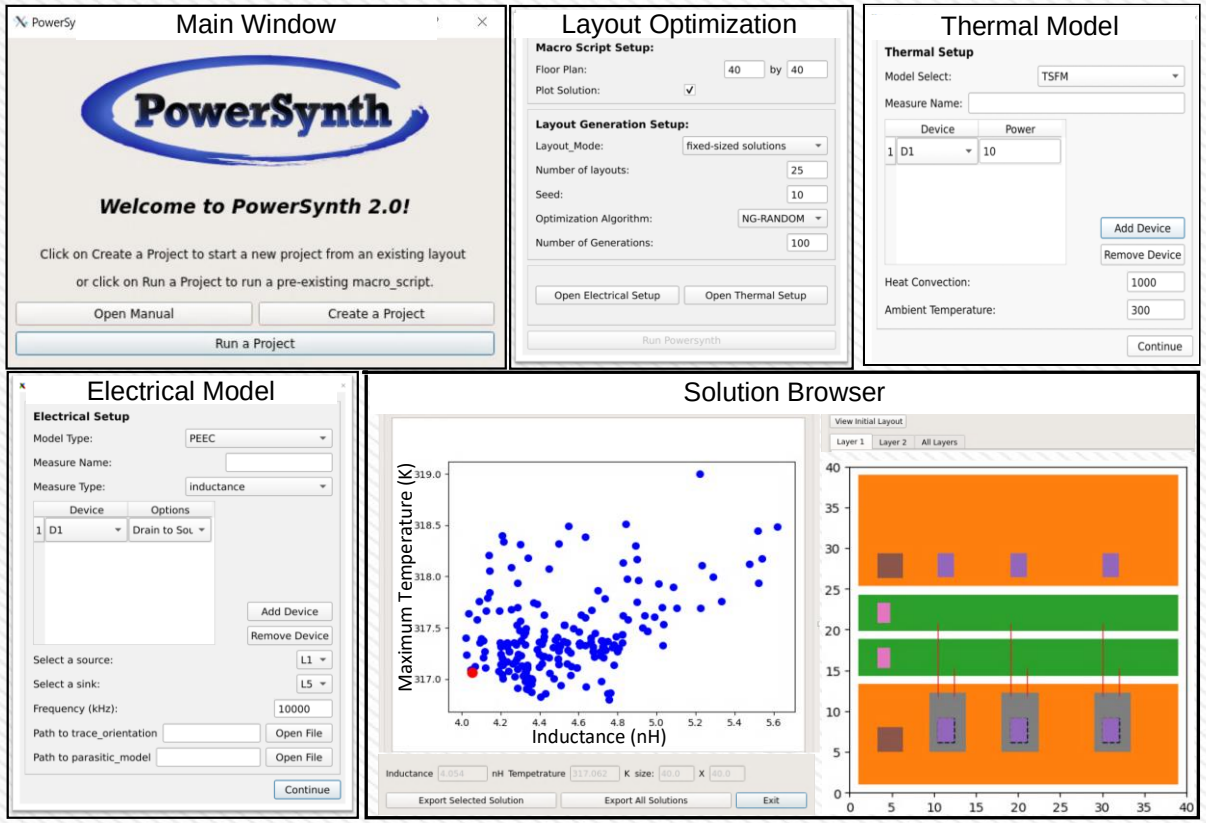
2.5D Full-bridge power module



3D half-bridge power module

PowerSynth 2 User Interfaces

- **Command Line Interface (CLI)**
  - Linux compatibility
  - User input through terminal
  - Modes: Script-based or Step-by-step
- **Graphical User Interface (GUI)**
  - Two flows:
    - Creating new project
    - Run existing project through ‘Macro script’
  - MDK editor
  - Optimization setup
  - Performance evaluation model setup
  - Interactive solution browser

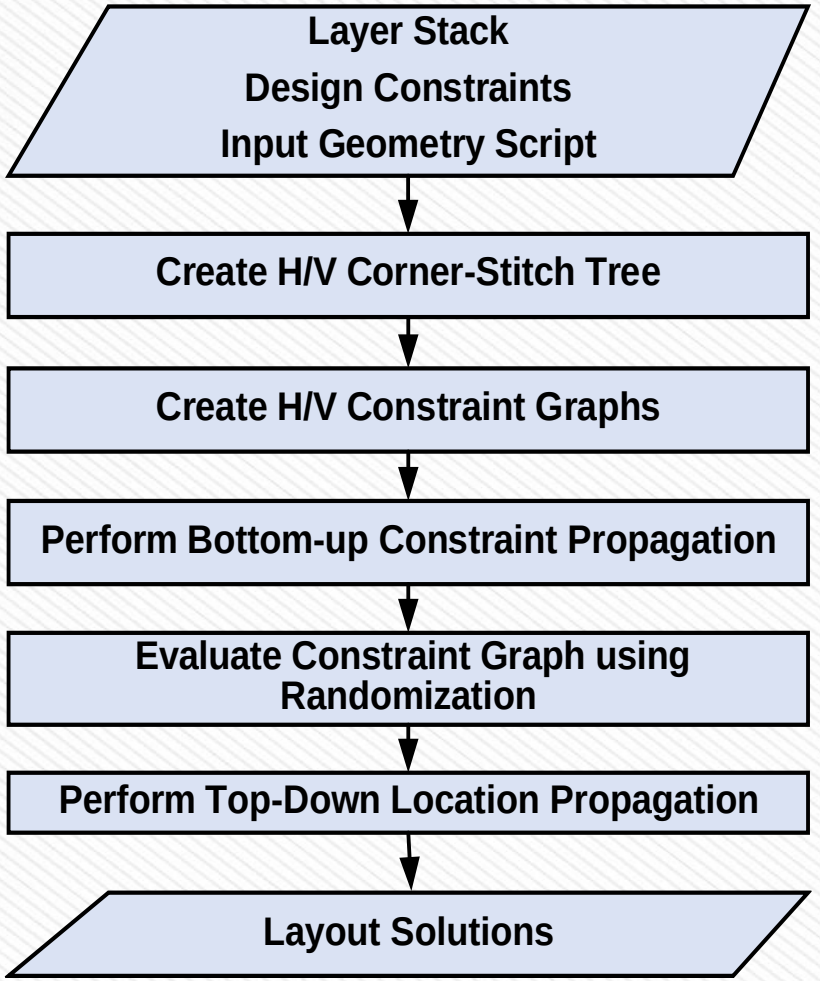


PowerSynth v2.0 GUI

Constraint-Aware Layout Engine

Features:

- Generic, hierarchical layout description script
- Generic, scalable layer stack
- Different types of constraints: design/reliability
- 100% DRC-clean solutions
- Hierarchical approach: 2D/2.5D/3D layout handling
- Generic, scalable, and efficient methodology→ SOTA 2D/3D packaging solutions
  - Hierarchical corner stitch data structure
  - Layer based geometry representation
  - Hierarchical constraint graph evaluation
- Three types of layout generation capability:
  - Minimum-size/Variable-size/Fixed-size



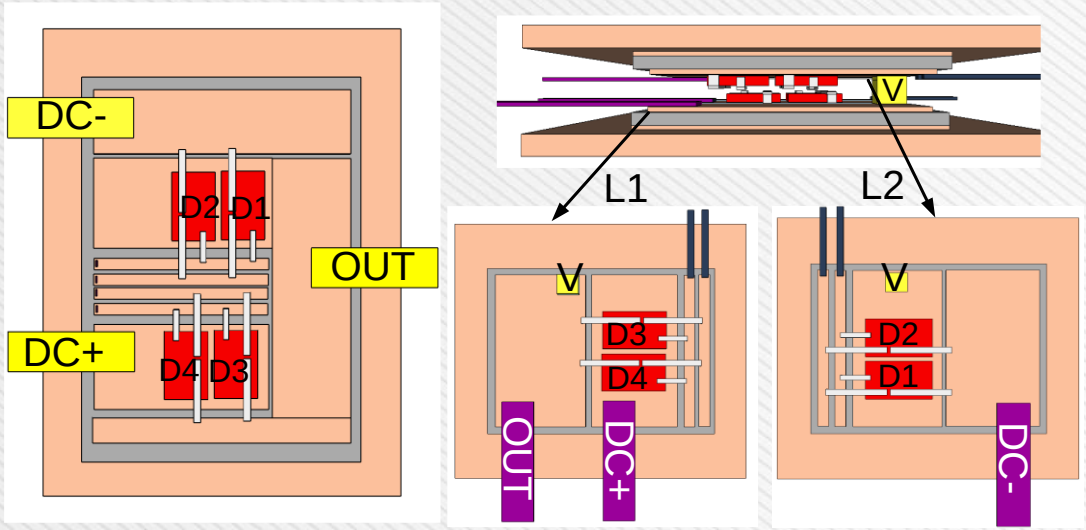
Layout generation workflow

[1] Imam Al Razi, Quang Le, H. Alan Mantooth, and Yarui Peng, “Hierarchical Layout Synthesis and Optimization Framework for High-Density Power Module Design Automation”, ICCAD, Nov 2021.

UNIVERSITY OF ARKANSAS

2D vs. 3D Layout

❑ Initial Layout

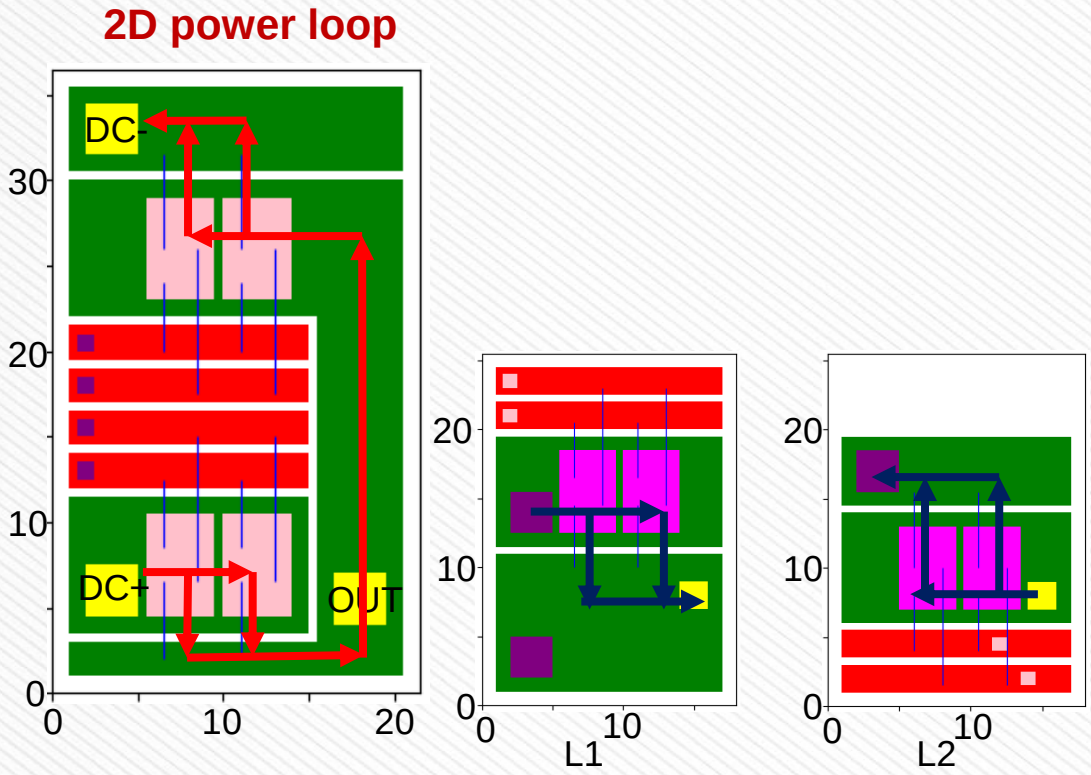


Half-bridge MCPM: 2D structure (left), 3D structure (right)

Performance comparison

Metric	2D	3D
Loop Inductance	15.93 nH	6.104 nH
Max Temperature	332.15 K	370.29 K (single-side cooling)
		328.38 K (dual-side cooling)

● Min-Sized layout:



2D layout **3D layout**

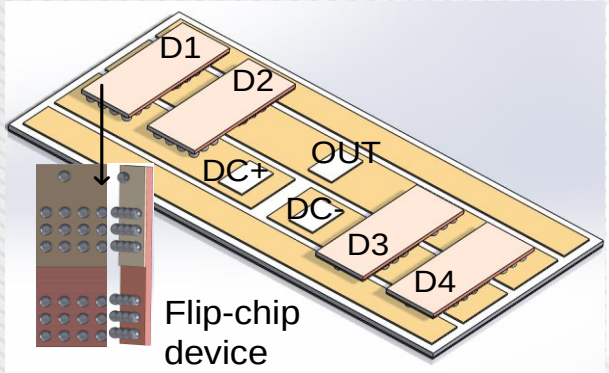
Imam Al Razi et.al, “Physical Design Automation for High-Density 3D Power Module Layout Synthesis and Optimization”, in ECCE , pp. 1984–1991, Oct 2020

UNIVERSITY OF ARKANSAS

High-Density SOTA Packaging Layouts

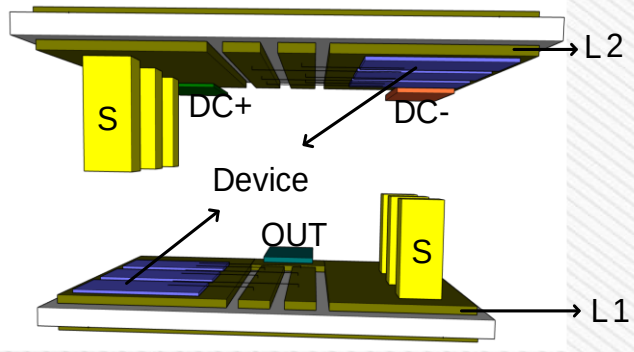
Layout Types:

- 2D/2.5D/3D wire bonded, wire bondless, hybrid, Flip-chip
- Generic algorithm to generate all types of solutions



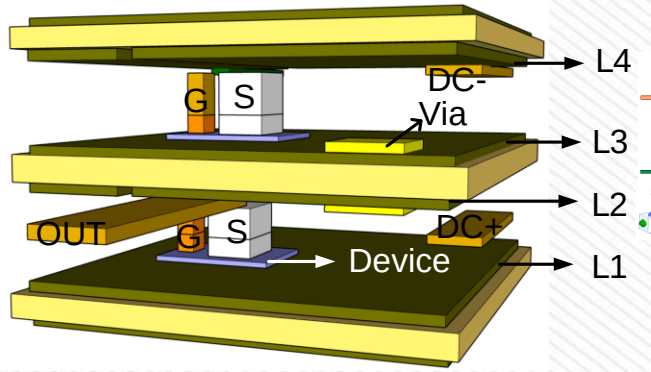
2D Flip-chip Half-bridge

- One device layer
- Solder ball array
- Extended drain connector
- Planar power loop
- Double-sided cooling



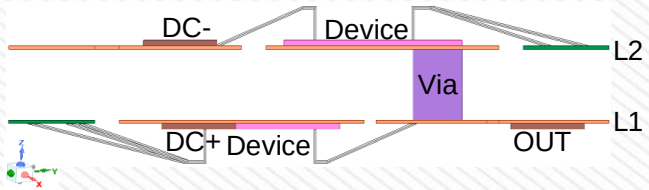
3D Hybrid Half-bridge

- Two device layers
- Wire bond (gate loop)
- Metallic post (power loop)
- Hybrid power loop
- Double-sided cooling



3D Wire-bondless Half-bridge

- Two device layers
- Metallic post (power & gate loop)
- Vertical power loop
- Double-sided cooling



3D Wire-bonded Half-bridge

- Two device layers
- Wire-bond (power & gate loop)
- Vertical power loop
- Embedded cooling

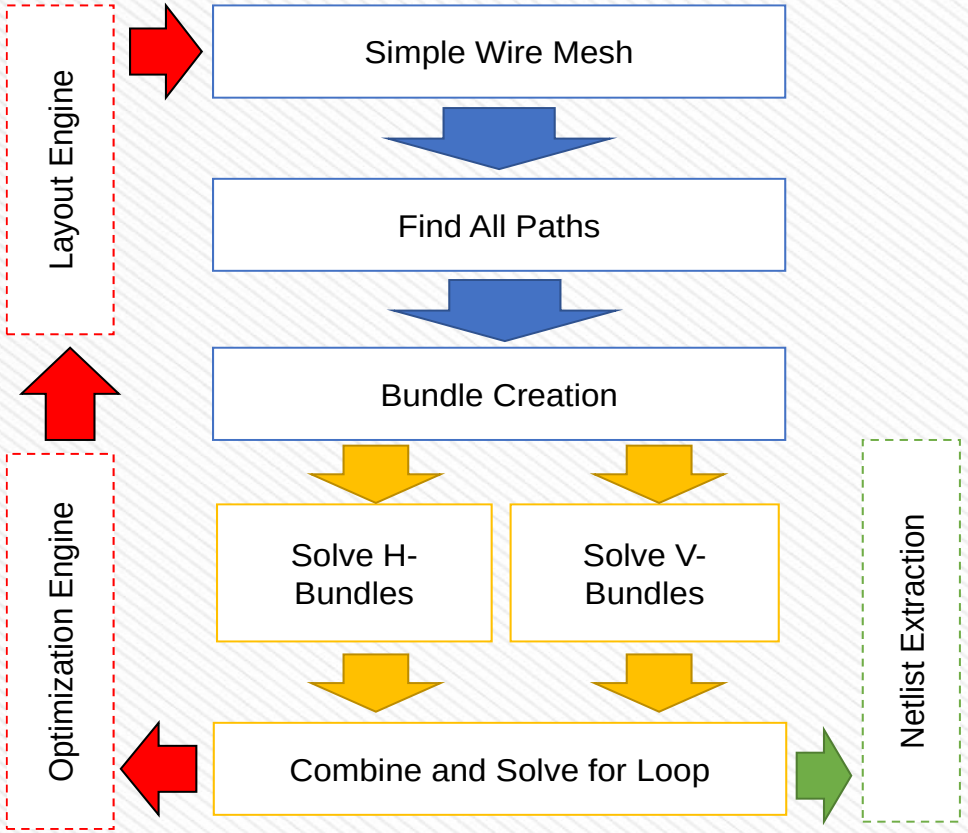
Loop-Based Electrical Modeling

Features:

- Efficient mutual inductance calculation
- Divide and conquer strategy during evaluation
- Less elements in the extracted netlist
- Suitable for post-layout analysis while fast and accurate for layout optimization purpose

Workflow [1]:

- Find the forward and return path from the layout
- Form a directed graph to store information
- Divide the layout into two groups: Horizontal and Vertical bundles
- Evaluate parasitic parameters for each bundle
- Combine both into the total loop result

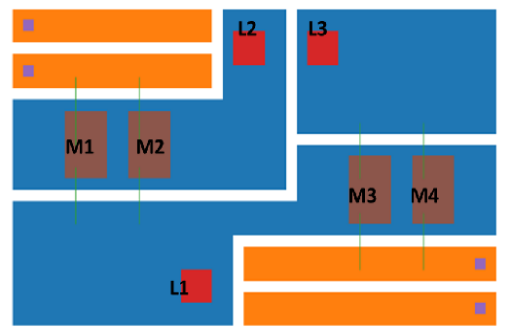


[1] Quang Le, Imam Al Razi, Tristan Evans, Shilpi Mukherjee, Yarui Peng, and H. Alan Mantooth, “Fast and Accurate Parasitic Extraction in Multichip Power Module Design Automation Considering Eddy-Current Losses”, (accepted) IEEE JESTPE, 2022.

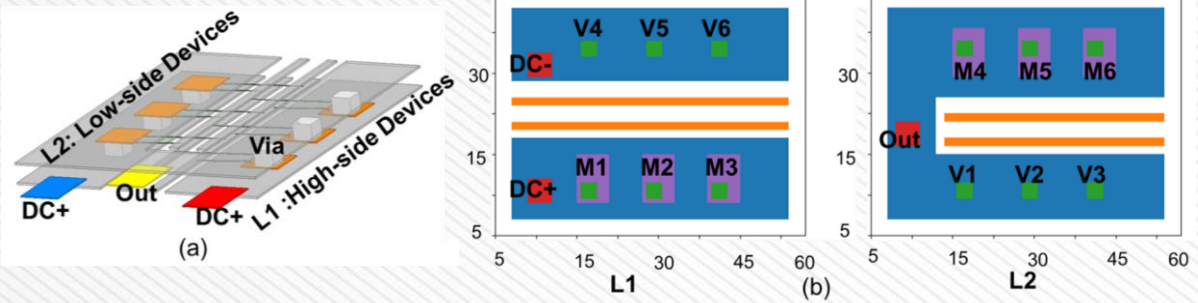
Example for 2D and 3D Layouts

- **Loop-model vs FastHenry: 7% error**
  - Shows up to 800× speed up for matrix evaluation
  - Netlist size reduction: >1000x versus PEEC

2D layout case



3D layout case: (a) structure, (b) planar view



Layout Case	Methods	L_{Loop} (nH)	Run Time (s)			Netlist size	Speed up	Error
			Formulation	Evaluation	Total Time			
2D case	FastHenry	17.3	---	---	8	1	---	---
	PEEC	16.1	0.5	0.345	0.8345	1820	9.6×	6.9%
	PowerSynth	16.5	0.42	1.4m	0.434	9	18.6×	4.6%
3D case	FastHenry	7.93	---	---	25	1	---	---
	PowerSynth	8.54	0.8	2.43m	0.824	50	30×	7.1%

Reliability Optimization Using PowerSynth

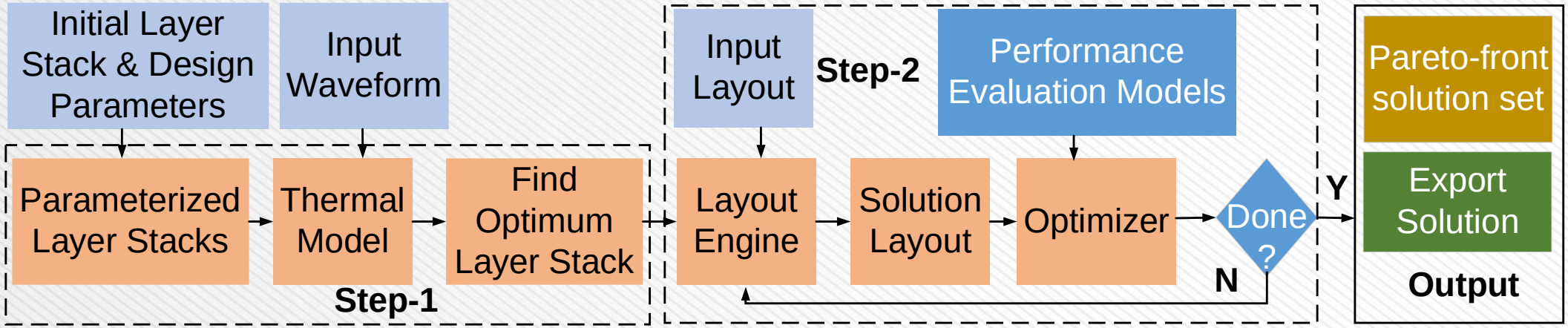
- **PowerSynth 2 allows:**
  - **Integration external modeling efforts/tools through APIs**
    - ParaPower: Army Research Lab (ARL) developed thermal and stress evaluation tool
  - **Handling both types of interconnects (i.e., wire bonds and solder joints)**
  - **Considering arbitrary layer stack**
  - **Material library modification**
- **To perform reliability optimization, it requires efficient, and accurate models**
- **In this work, MCPM layouts are optimized for two major reliability threats:**
  - **Thermal cycling impact minimization**
    - Transient thermal model for 2D MCPM layouts
    - Phase change material (PCM) consideration
  - **Electromigration associated risk assessment**
    - Current density modeling through Z-Mesh tool

[1] ARL ParaPower, "https://github.com/USArmyResearchLab/ParaPower".

Transient Thermal Optimization

❑ Two-step optimization flow:

- **Step-1: Layer stack optimization**
  - Material, thickness variation
- **Step-2: Layout optimization**
  - Placement of devices & routing of traces
  - Variable floorplan sizes



- **Newly developed transient thermal model:**
  - Max, average, peak-to-peak temperature evaluation
  - Both static and transient thermal evaluation
  - Interaction among three tools

ARL ParaPower

POWERSYNTH

HSPICE

[1] Imam Al Razi, David Huitink, and Yarui Peng, "PowerSynth-Guided Reliability Optimization of Multi-Chip Power Module", in Proc. IEEE Applied Power Electronics Conference, pp. 1516-1523, Jun 2021.

EM-Aware Reliability Optimization

❑ Implementation using PowerSynth 2 APIs:

❑ Mean Time To Failure (MTTF) Calculation :

- **Closed-formula approach (Black's Equation for Electromigration)**

  $MTTF = A\, j^{-2} \exp(E_a/kT)$,

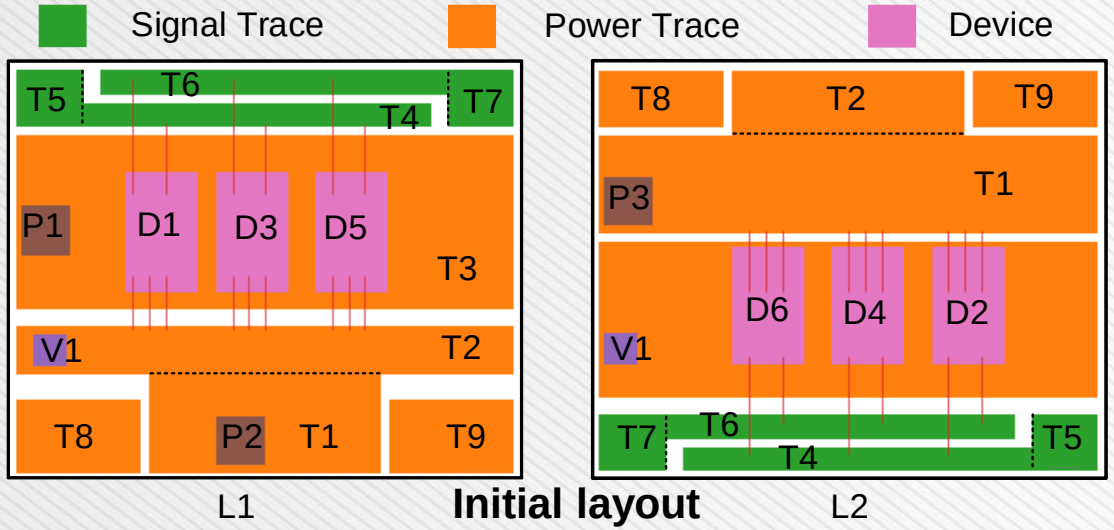
  where, A = constant, j = current density, E_a = Activation energy, k = Boltzman constant, T= Temperature

- **Data-Driven Model**
  - Look-up table from experimental results
  - Parameter tuning on analytical models from experimental results

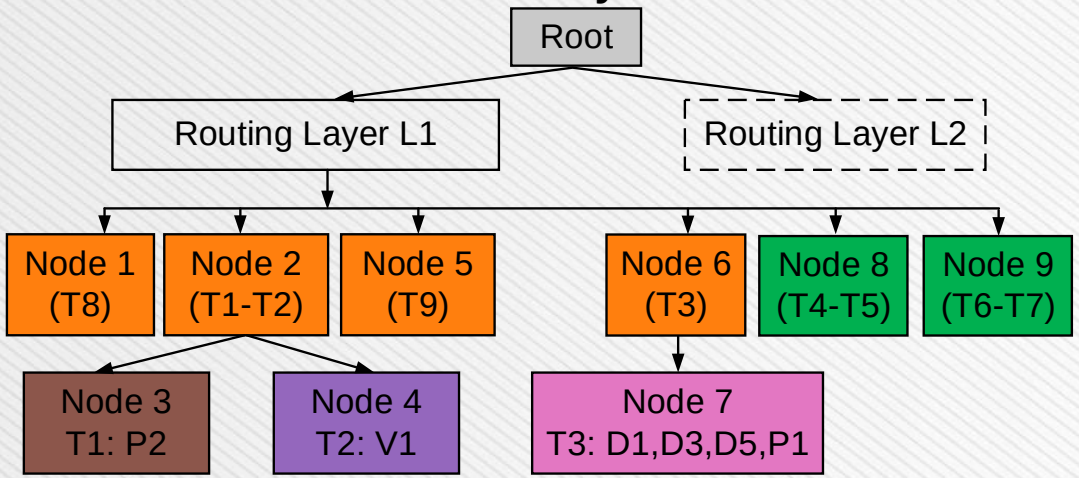
[1] Imam Al Razi, Whit Vinson, David Huitink, and Yarui Peng, "Electromigration-Aware Reliability Optimization of MCPM Layouts Using PowerSynth", in Proc. IEEE Energy Conversion Congress and Exposition, pp. 1-8, Oct 2022.

Hierarchical Layout Representation

❑ 3D Wire-Bonded half-bridge MCPM layout



Initial layout



Hierarchical tree

```
# Via Connectivity Information
L1 L2: V1  Through

# Layout Geometry
L1 Z-
+ T8 power 7 7 7.5 4.5
+ T9 power 29.5 7 7.5 4.5
+ T1 power 15 7 14 6
- T2 power 7 13 30 3
    + B11 power 14 15.75
    + B28 power 20 15.75
    + B36 power 26 15.75
    + P2 power_lead 19 7.5
    + V1 Via 8 13.5
+ T4 signal 11 28 21 1.5
- T5 signal 7 28 4 3.5
    + B7 signal 16 28.25
    + B27 signal 22 28.25
    + B40 signal 28 28.25
+ T6 signal 12 30 21 1.5
- T7 signal 33 28 4 3.5
    + B8 signal 14 31
    + B29 signal 20 31
    + B41 signal 26 31
+ T3 power 7 17 30 10.5
    + P1 power_lead 7.5 21
    + D1 MOS 13.5 18
        + B1 signal 16 24
        + B2 power 14 19
        + B3 power 14 24
    + D3 MOS 19 18
        + B24 signal 22 24
        + B25 power 20 19
        + B26 power 20 24
    + D5 MOS 25 18
        + B37 signal 28 24
        + B38 power 26 24
        + B39 power 26 19
```

Developer mode

```
# Via Connectivity Information
L1 L2: V1 Through

# Layout Geometry
L1 Z-
+ T8 power 7 7 7.5 4.5
+ T9 power 29.5 7 7.5 4.5
+ T1 power 15 7 14 6
- T2 power 7 13 30 3 BW3 BW6 BW9
    + P2 power_lead 19 7.5
    + V1 Via 8 13.5
+ T4 signal 11 28 21 1.5 BW1 BW4 BW7
- T5 signal 7 28 4 3.5
+ T6 signal 12 30 21 1.5 BW2 BW5 BW8
- T7 signal 33 28 4 3.5
+ T3 power 7 17 30 10.5
    + P1 power_lead 7.5 21
    + D1 MOS 13.5 18 BW1 BW2 BW3
    + D3 MOS 19 18 BW4 BW5 BW6
    + D5 MOS 25 18 BW7 BW8 BW9
```

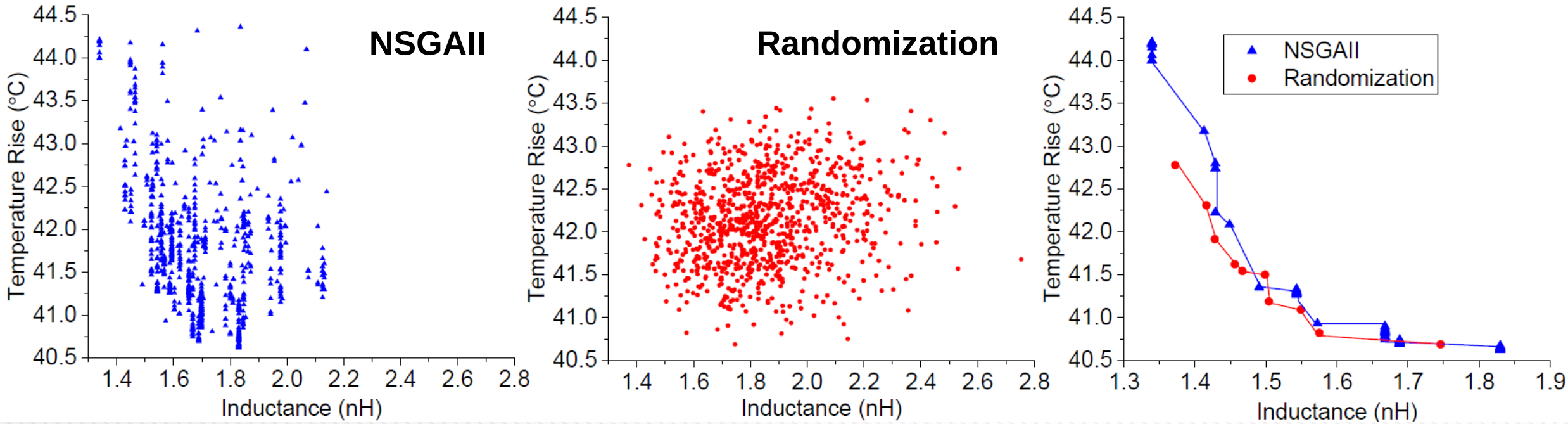
User mode

Input geometry script for L1

Layout Optimization Algorithms

❑ Comparison for wire-bond less 3D module

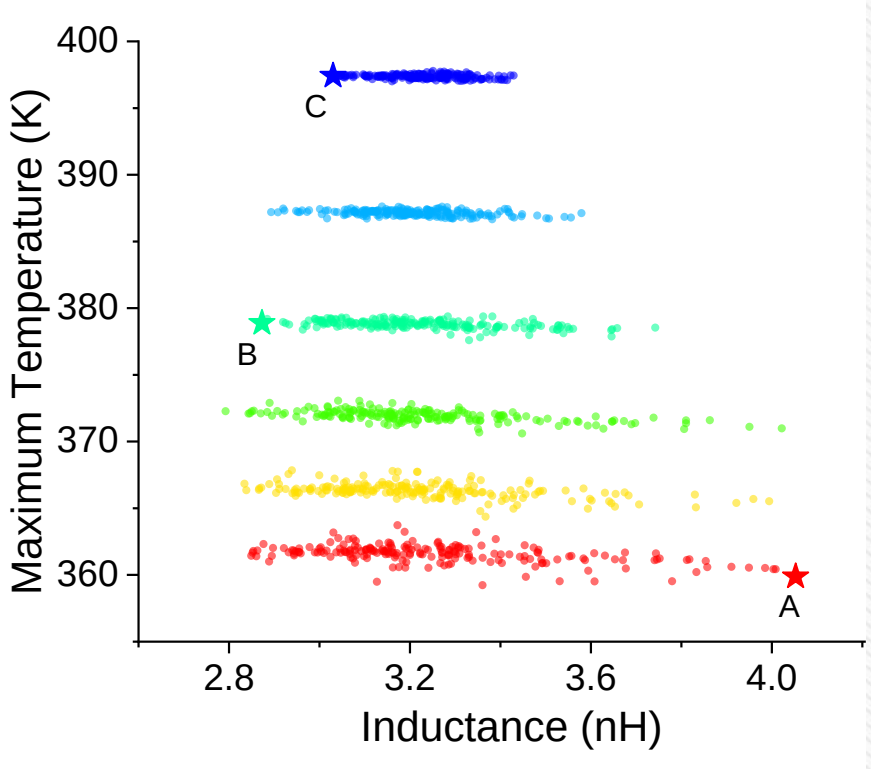
Algorithm	Total Layouts	Approximate runtime(min)		On Pareto-front
		Generation	Evaluation	
NSGAII	937	25	206	148
Randomization	937	1	212	10



3D Layout Optimization Results

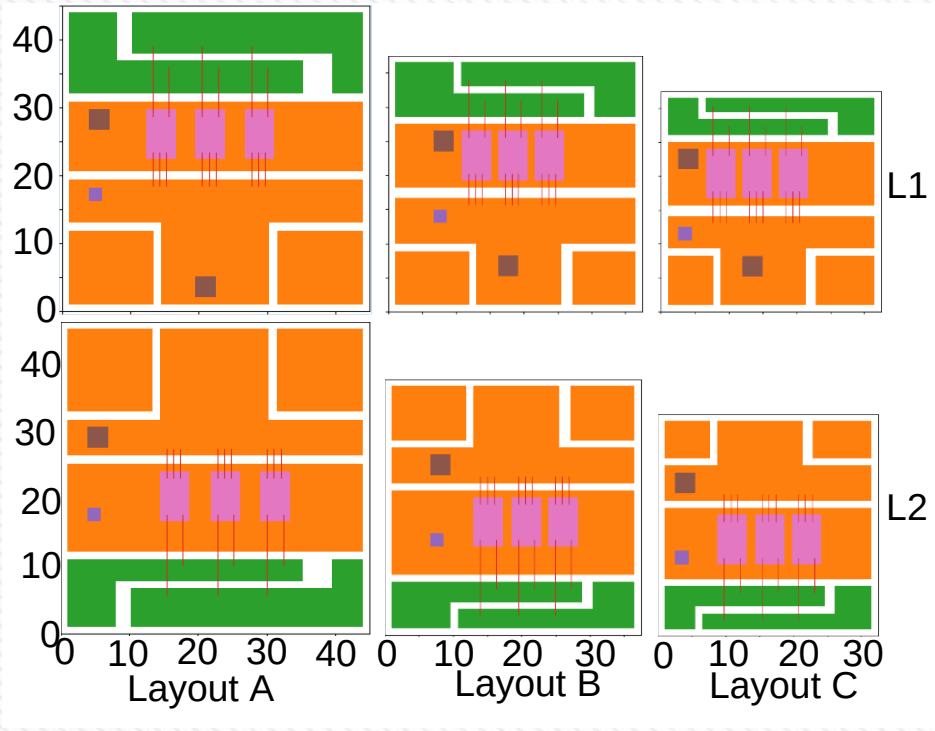
3D Wire-Bonded Layout Case

- **Electro-thermal optimization**
  - Six floorplan sizes
  - 1200 total layout solutions
  - 43 min total runtime



Performance Values

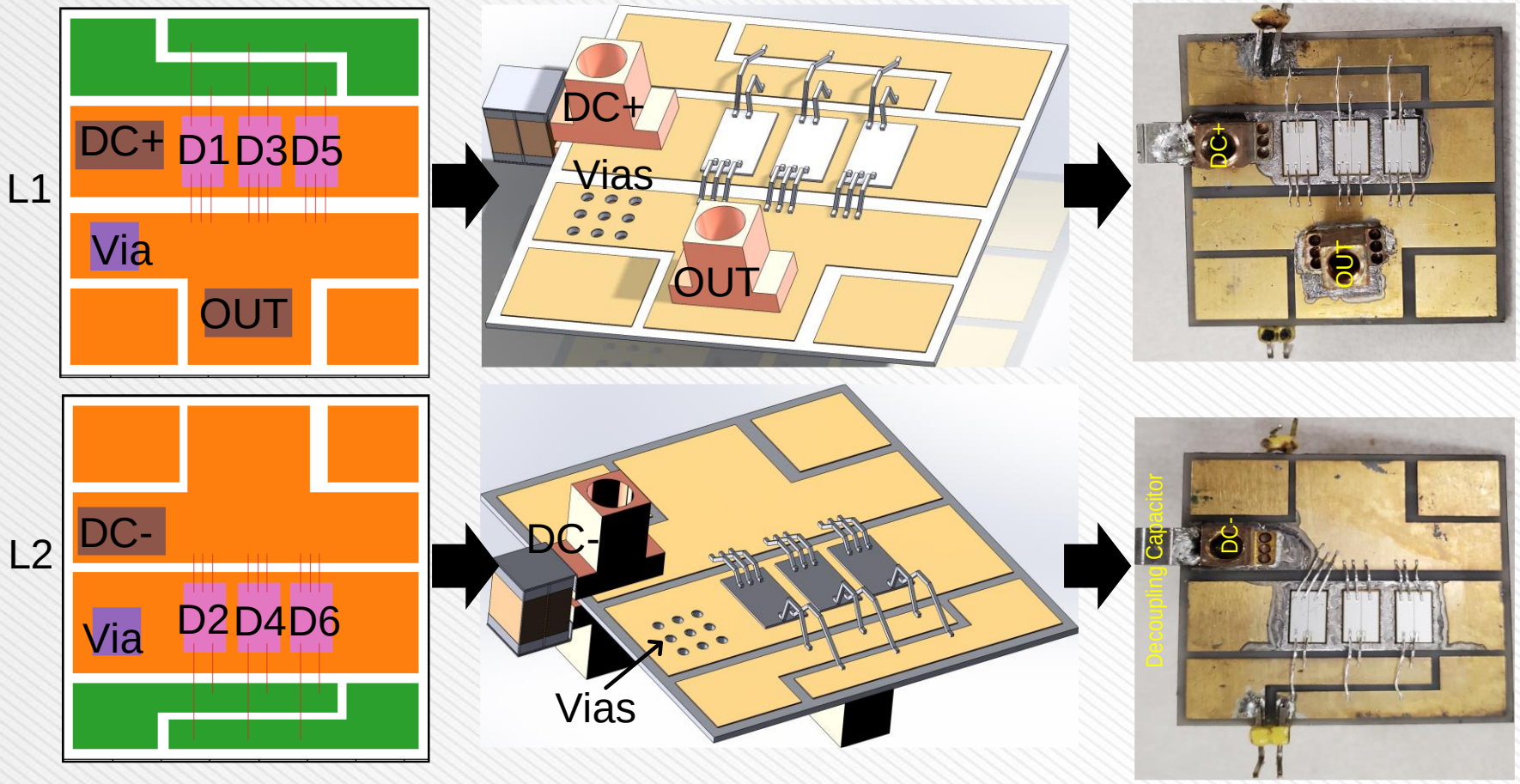
ID	L (nH)	Max T (K)	Size (mm²)
A	4.05	359.87	45 × 45
B	2.87	378.88	37.5 × 37.5
C	2.54	397.41	32.5 × 32.5



Experimental Design Fabrication

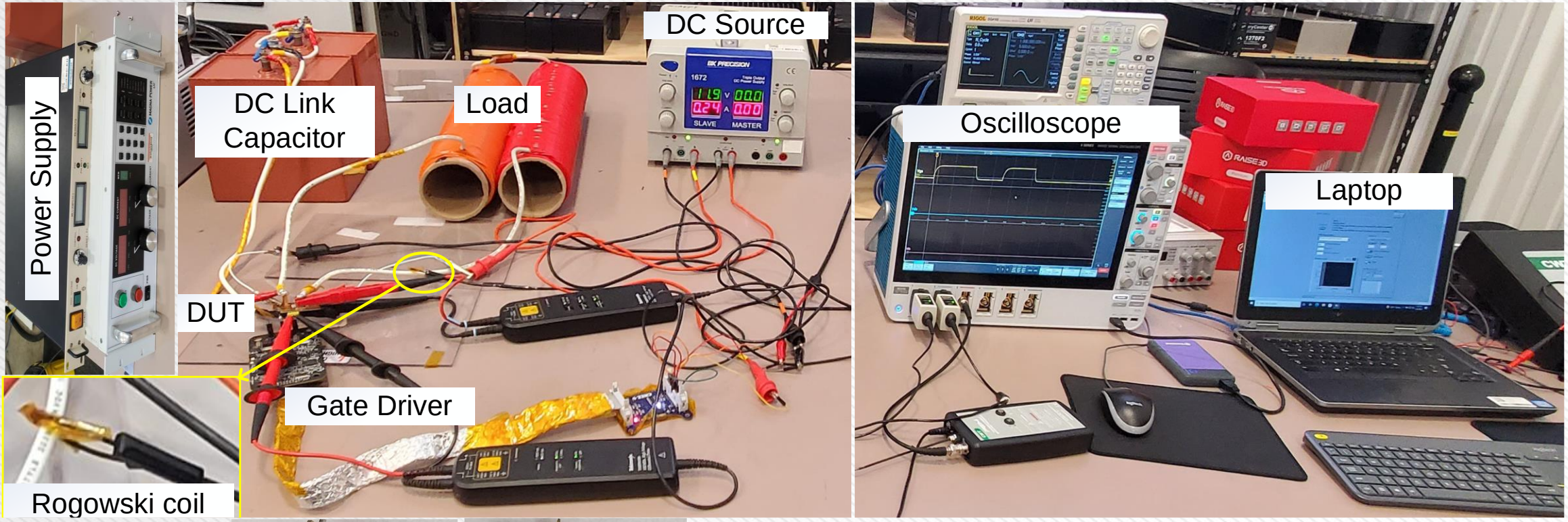
❑ Post-Layout Optimization

- Solution layout B has been tuned for gate loop optimization
- Modified solution is exported to SoliDWorks and taped out for fabrication

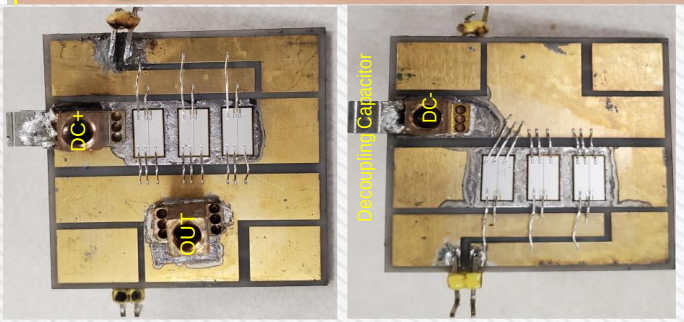


Experimental Design Validation

❑ Double Pulse Test (Experimental Setup)



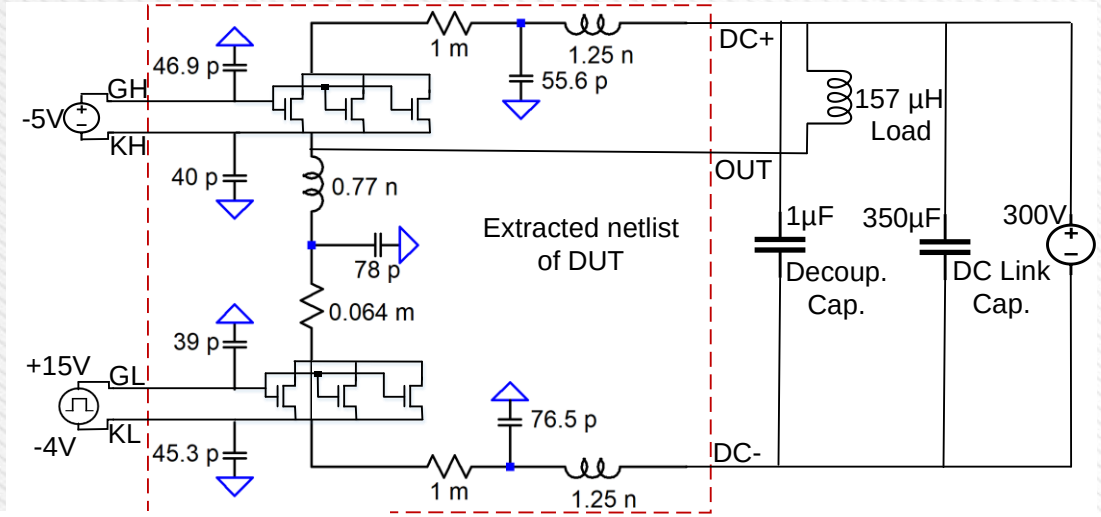
DUT

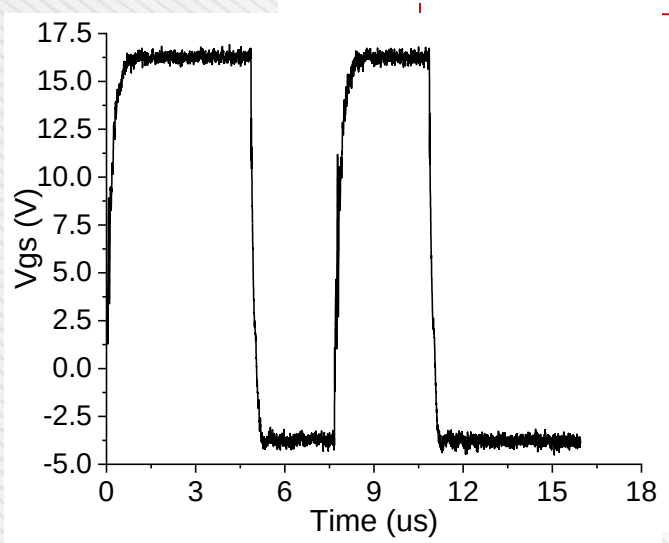


UNIVERSITY OF ARKANSAS

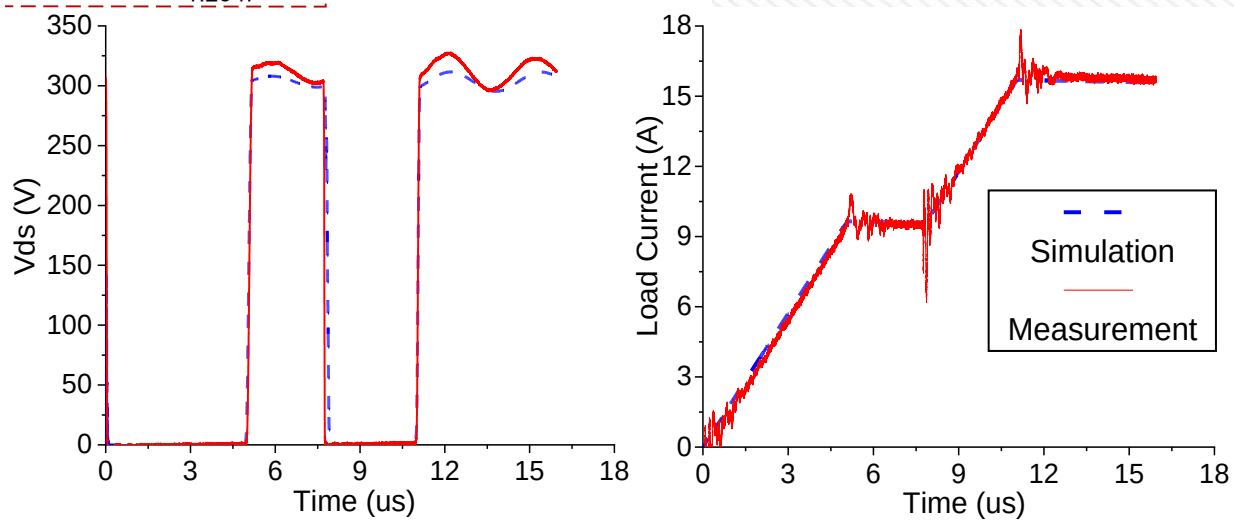
Module Functionality Validation

❑ Double Pulse Test Results





Gate Pulse



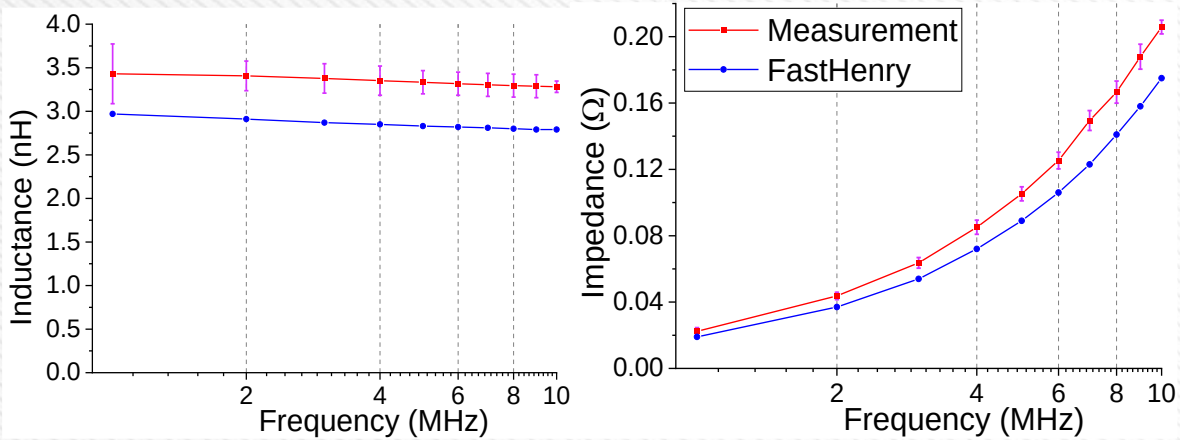
DPT Results

Electrical Model Validation

❑ Impedance Measurement

- Setup

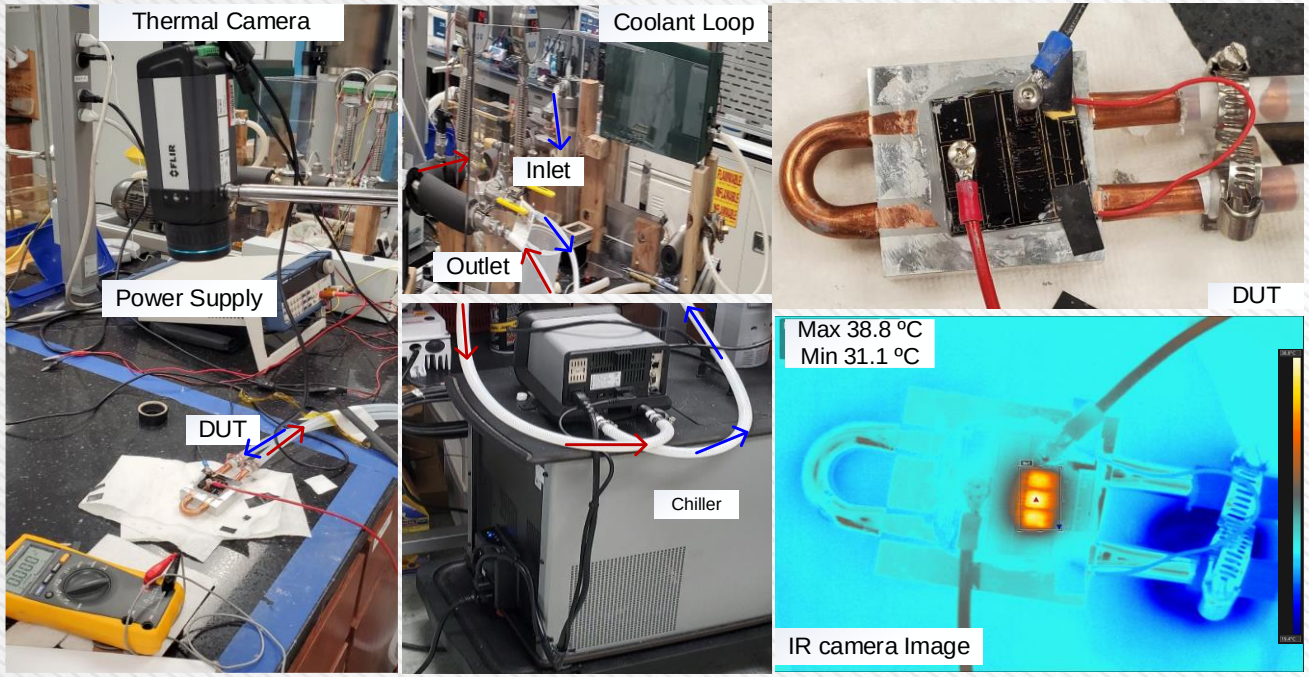
- Results

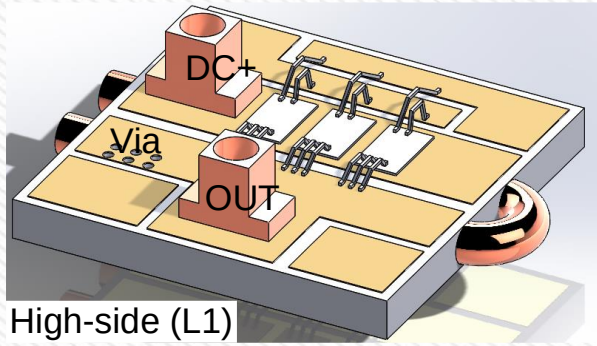


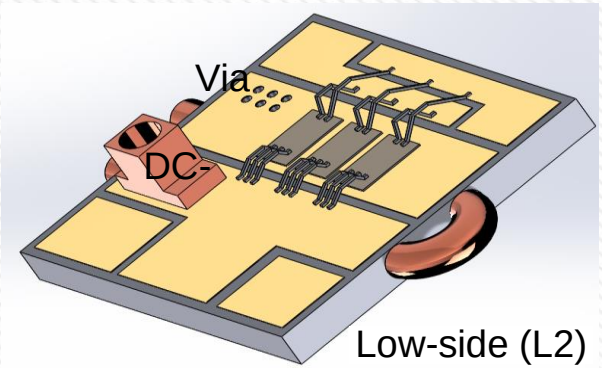
Metric	Frequency	FastHenry	Measurement	Mismatch%
L (nH)	1 MHz	2.97	3.43	13.4%
Z (Ω)	10 MHz	0.175	0.20	12.5%

Thermal Model Validation

❑ Embedded Cooling Concept







Boundary Conditions:

- Heat dissipation/die: 10.2 W
- Effective h: 7394 W/m^{2}K
- Ambient T: 297 K

Case	Maximum Temperature (ºC)			% of Mismatch
	D1	D3	D5	
Measurement	37.00	38.80	37.90	-
ParaPower	40.75	42.30	40.78	9.02%

UNIVERSITY OF ARKANSAS

Optimization Validation & Comparison

Source	Architecture	Packaging	Power Loop Inductance (nH)	Cooling	Device Rating	Devices/ Sw. Position	Area ($mm \times mm$)
[84]	2D Phase-leg	Wire-Bonded	9.7 (Planar loop)	Single	1200 V/ 100 A	5 SiC MOS	88.1 × 50.1
[85]	2D Half-bridge	Wire-Bonded	7.5 (Vertical loop)	Dual	650 V/ 200 A	3 SiC MOS	60 × 80
[86]	2.5D Half-bridge	Hybrid	2.60 (Vertical loop)	Dual	1200 V/ 90 A	1 SiC MOS	40 × 37
[87]	2.5D Half-bridge	Hybrid	3.38 (Vertical loop)	Single	1200 V/ 24 A	1 SiC MOS	21 × 11.5
[88]	2.5D Half-bridge	Hybrid	4.3 (Vertical loop)	Single	1200 V/ 40 A	2 SiC MOS	23.7 × 14.2
[89]	2.5D H-bridge	Wire Bondless	4.5 (Vertical loop)	Dual	1200V/ 50A	4 SiC MOS	76.9 × 74.9
PS v1.9	2D Half-bridge/ 2.5D Full-bridge	Wire-Bonded	7.58 (Planar loop)	Single	1200 V/ 40 A	2 SiC MOS	40 × 40
[90]	3D Half-bridge	Wire-Bondless	0.93 (Vertical loop)	Dual	650 V/ 60 A	2 GaN HEMT	45 × 35
[91]	3D Half-bridge	Wire Bondless	4 (Vertical loop)	Dual	1200 V/ 50A	2 Si IGBT	42.5 × 40.1
[92]	3D Half-bridge	Flip-chip	4.5 (Vertical loop)	Dual	900 V/ 194 A	2 SiC MOS	28 × 50.5
[92]	3D Half-bridge	Wire Bondless	5.1 (Vertical loop)	Dual	3300 V/ 50 A	2 SiC MOS	27 × 46.4
PS v2.0	3D Half-bridge	Wire-Bonded	3.43 (Vertical loop)	Embedded	900 V/ 194 A	3 SiC MOS	37.5 × 37.5

[1] Imam Al Razi, “Constraint-Aware, Scalable, and Efficient Algorithms for Multi-Chip Power Module Layout Optimization”, Ph.D. Dissertation, July 2022.

Conclusions

- **PowerSynth is the first power module layout synthesis and optimization framework promising for design automation in the power electronics industry.**
- **PowerSynth 2 improves scalability, accuracy, efficiency, and handles 3D layouts**
  - Generic, Scalable, and hierarchical representation technique → All 2D/2.5D/3D
  - Design and reliability constraints → 100% DRC-clean and reliable solutions
  - Both 2D/2.5D and 3D CAD flow have been hardware-validated
  - PowerSynth flow vs. traditional→ Order of magnitude productivity improvement
    - Accuracy: 10-15%, Speedup: X1000, Memory reduction: X100
  - First tool to consider electro-thermo-mechanical and reliability co-optimization.
  - Both GUI and command-line interfaces for users
  - Release Package, Manual, Design Cases, Source Code Available to public
- **Current Limitations:**
  - Initial layout template dependency & Limited to Manhattan layouts

UNIVERSITY OF ARKANSAS

Thank You

Release Webpage: https://e3da.csce.uark.edu/release/PowerSynth/
Source Code on Github: https://github.com/e3da