HiTEC & APPE Joint Session
Albuquerque, NM
3:45 - 4:15PM
Thursday, April 20, 2023

International Microelectronics Assembly & Packaging Society

Factoring Interacting Stress Mechanisms in Design for Reliability of Extreme Environment Power Modules

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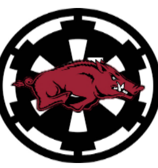
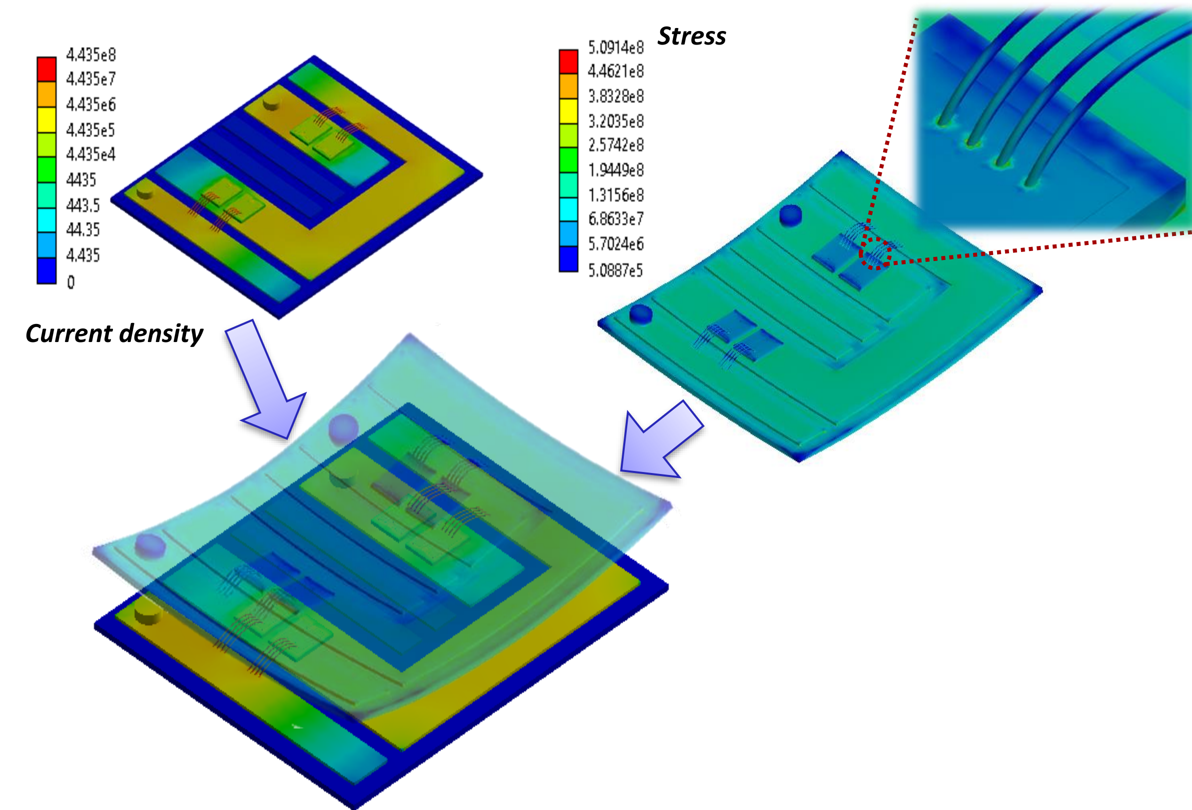
University of Arkansas
Mechanical Engineering[1], Computer Science & Computer Engineering[2], Electrical Engineering[3]



Content Overview

- Power Electronics SoA & Challenges
- Reliability Modeling & Considerations
- Performance & Optimization w/ EDA
- Case Study
- Conclusions & Outlook
- Q&A



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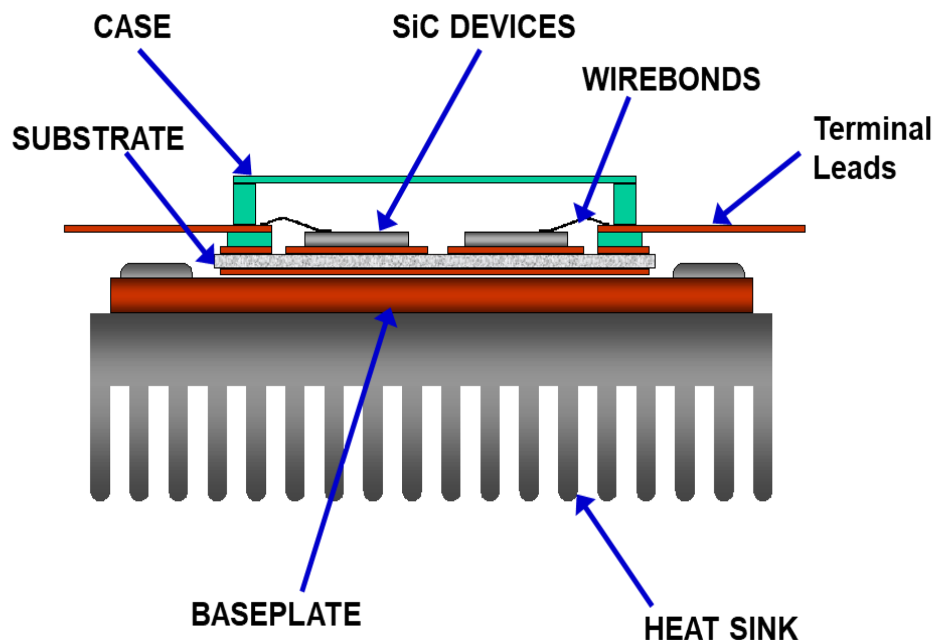
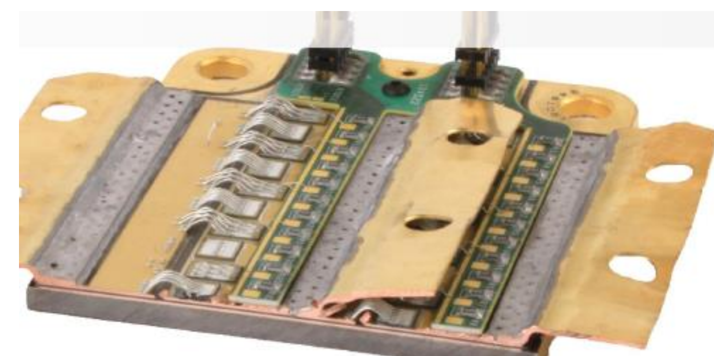
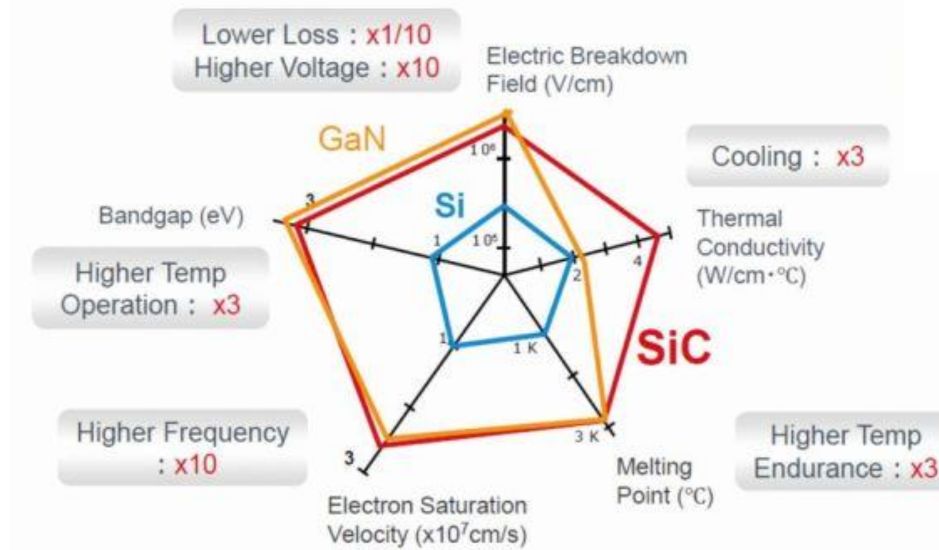
Power Electronics SoA & Challenges

- **State of the Art: Wide Bandgap Power Modules Tech for high amperage**
  - **Challenges**
    1. **Parasitic Control**
    2. **Thermal Management vs. High loss density**
    3. **Reliability & Manufacturability vs WBG Characteristics**



[1] e.g. Wolfspeed high Performance HT-3000 module & cutaway
https://s3.i-micronews.com/uploads/2019/02/SP19416-YOLE_Wolfspeed-CAS325M12HM2-1200V-SiC-Module_SAMPLE.pdf





[2] "Demystifying SiC MOSFETs challenges," July 22, 2020, Power Electronics News: Technical Articles, https://www.powerelectronicsnews.com/demystifying-sic-mosfets-challenges/

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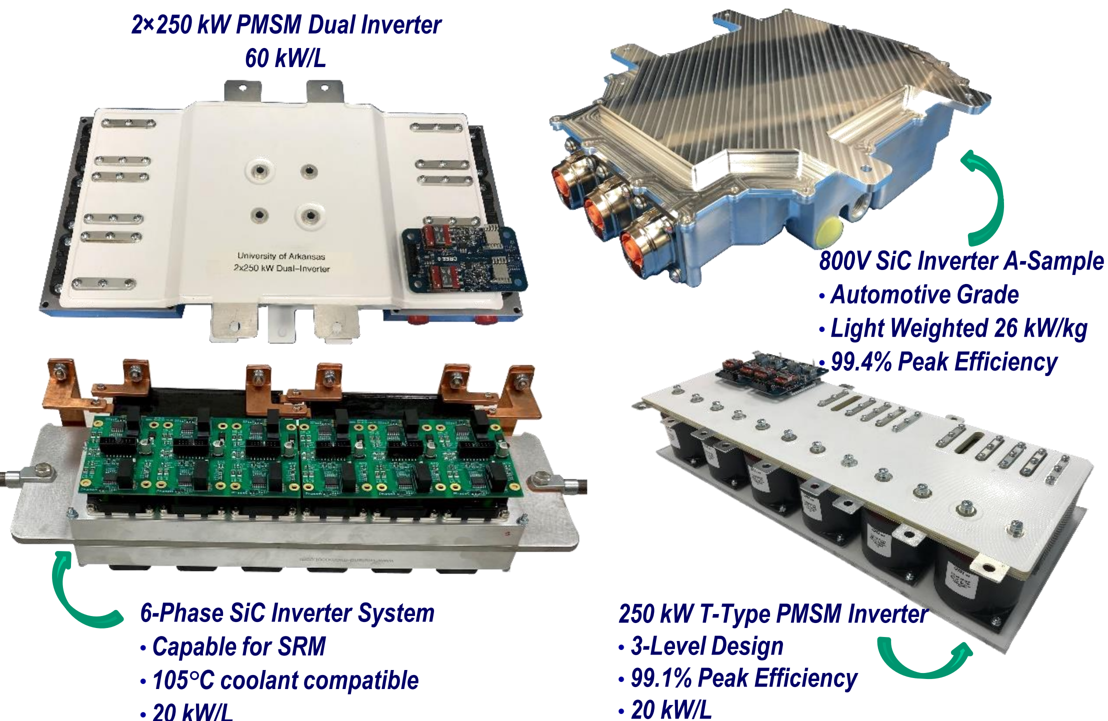
Power Electronics: UAPG Contributions

➢ University of Arkansas Power Group

- **History of PE Module and System Development & Integration**



[3] https://news.uark.edu/articles/63737/electric-motor-drive-takes-off-in-test-flight-of-passenger-hybrid-electric-plane

Wolfspeed HT-3000 commercial module within which we integrated the single-chip SiC gate drivers shown on the distribution board.

We achieved > 99% efficiency using these gate drivers with higher power density & reliability.

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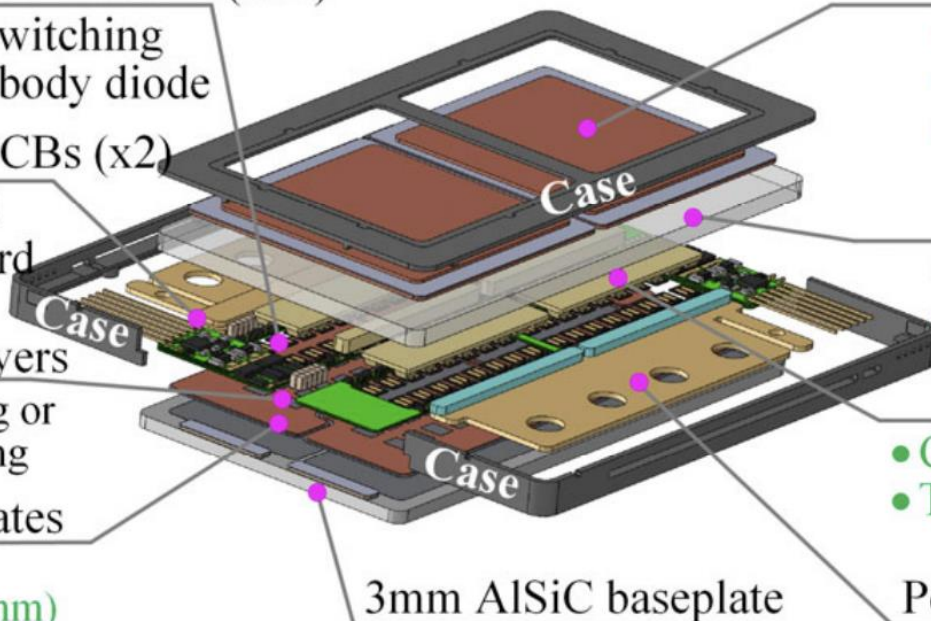

HiDEC
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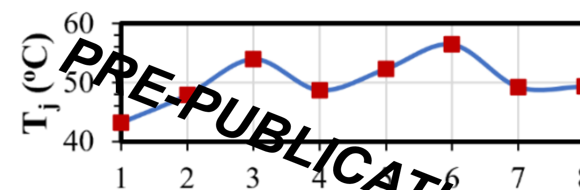
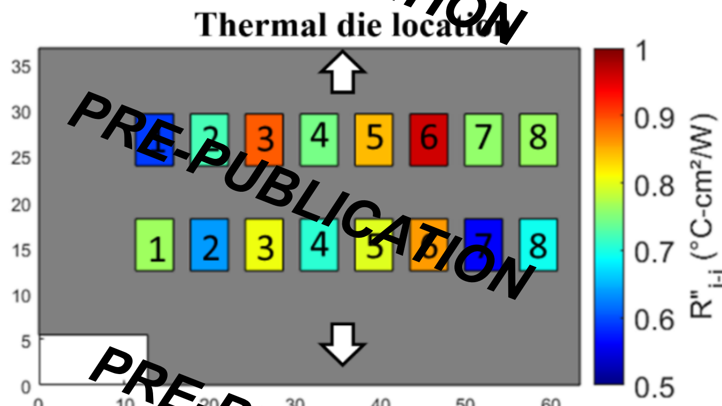
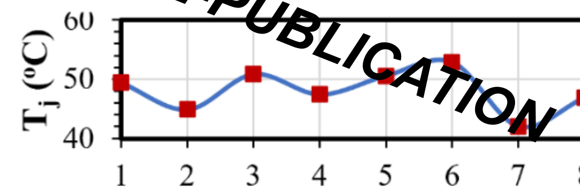


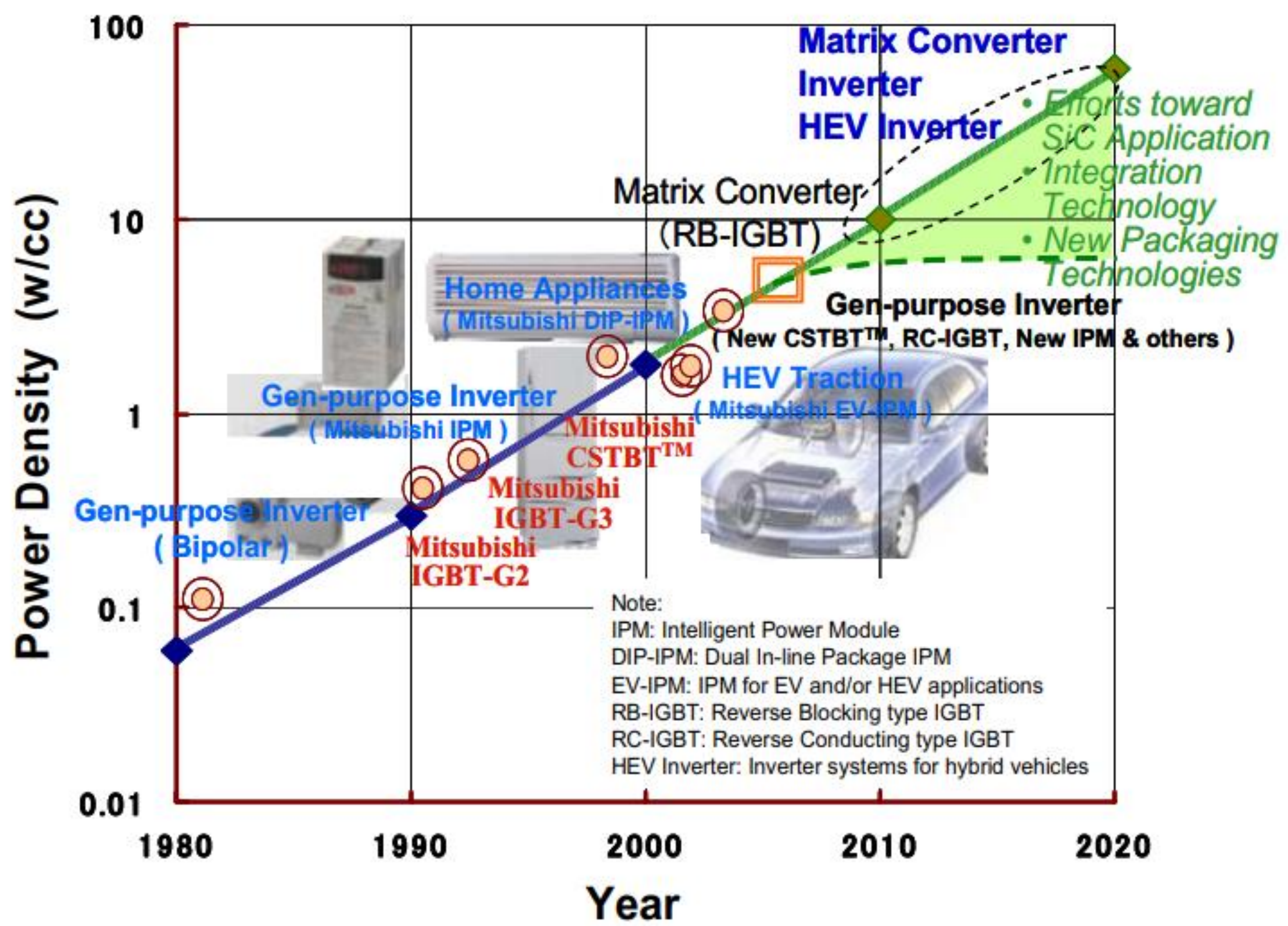




[4] Y. Chen, A. Iradukunda, H. A. Mantooth, Z. Chen and D. Huitink, "A Tutorial on High Density Power Module Packaging," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2022.3232691.

Power Electronics: WBG trajectory toward higher T

- PE devices are increasing in power density
  - Higher power requirements
  - Desired size and weight reductions
- A slew of downstream effects will occur as a result of increased power density, all related to package reliability



[5] G. Majumdar, "Recent technologies and trends of power devices," 2007 International Workshop on Physics of Semiconductor Devices, Mumbai, India, 2007, pp.787-792, doi: 10.1109/IWPSD.2007.4472635.

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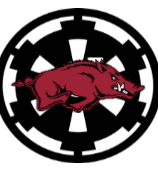
Reliability: Temperature as a core driver



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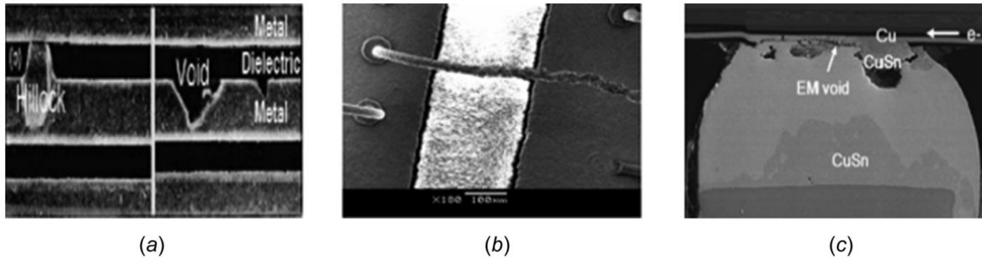
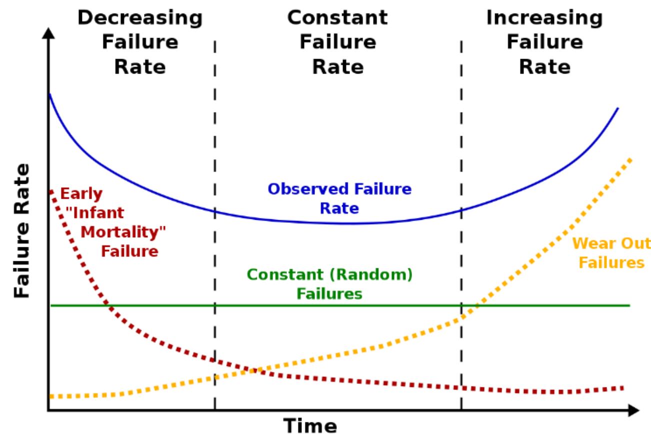
- **Single stress reliability risks are easily identified after use condition analyses, even for optimized designs**
  - **For example, regions on a layout where temperatures are relatively high and stresses are present would be an indicator that fatigue failure may ultimately be the downfall of that design**



(a) (b) (c)

Cu interconnect, wire bond, and solder ball EM failure images

[6] Gabriel, O. E., and Huitink, D. R. (October 22, 2022). "Failure Mechanisms Driven Reliability Models for Power Electronics: A Review." ASME. *J. Electron. Packag*. June 2023; 145(2): 020801. https://doi.org/10.1115/1.4055774



- Failure Mechanisms
  - Overstress
    - Mechanical
      - Brittle Fracture
      - Plastic Deformation
      - Interfacial Delamination
    - Electrical
      - Gate Oxide Breakdown
      - Interconnect Breakdown
      - EMI
      - ESD
      - Radiation
    - Chemical
      - Liquid Exposure & Shorting
  - Wear-out
    - Mechanical
      - Fatigue
      - Creep
      - Wear
      - Stress-driven Voiding
    - Electrical
      - Hillock Formation
      - Junction Spiking
      - Electromigration
    - Chemical
      - Corrosion
      - Diffusion
      - Dendritic Growth

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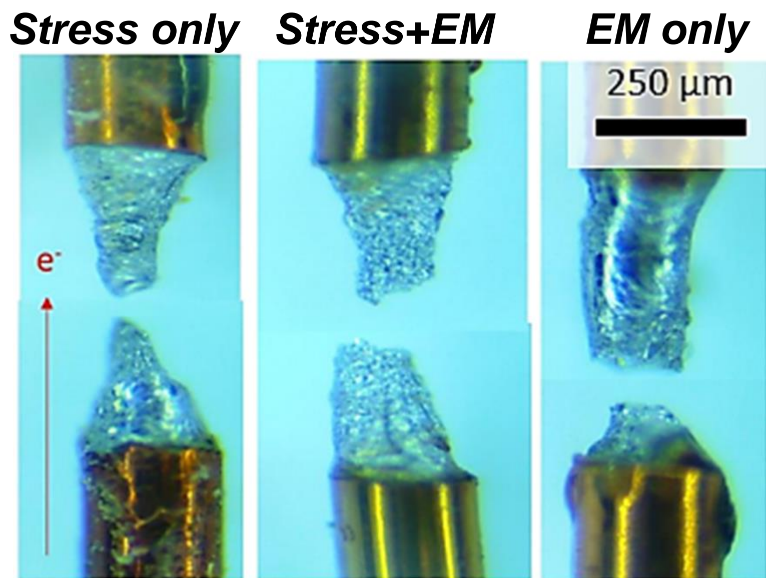
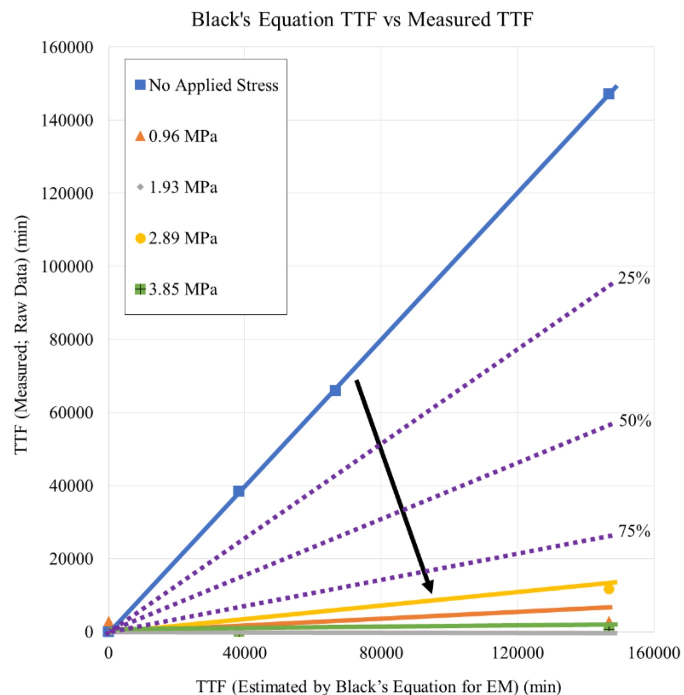
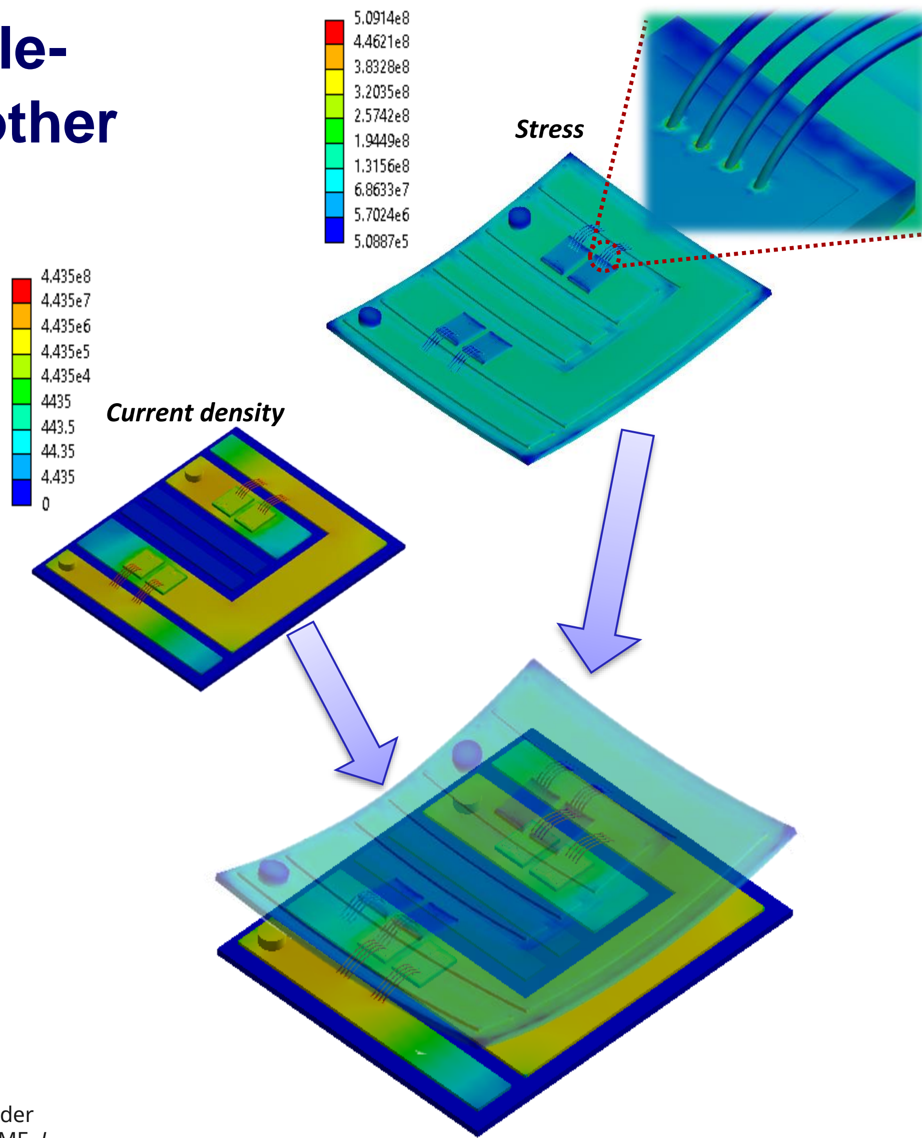
Motivation for Combo-Stress + EDA

- **As power density continues to increase, many single-stress failure regions begin to overlap with one another**
  - **How will this impact the overall reliability?**
  - **How do we deal with multi-stress scenarios?**



PbSn eutectic Solder Spheres after Creep stress, EM+Tensile Stress, and EM conditions (Temp. + Current) (left to right)





[7] Montazeri, M., Vinson, W. M., and Huitink, D. R. (August 8, 2022). "Accelerated Solder Interconnect Testing Under Electromigratory and Mechanical Strain Conditions." ASME. *J. Electron. Packag*. June 2023; 145(2): 021002. https://doi.org/10.1115/1.4055024

Factoring Combo-Stress Effects into Test Planning

- **Simply applying multiple stresses simultaneously will not necessarily provide useful data for life prediction → we want to also understand *interaction***
  - **Testing at appropriate levels**
  - **Appropriate Number of samples**

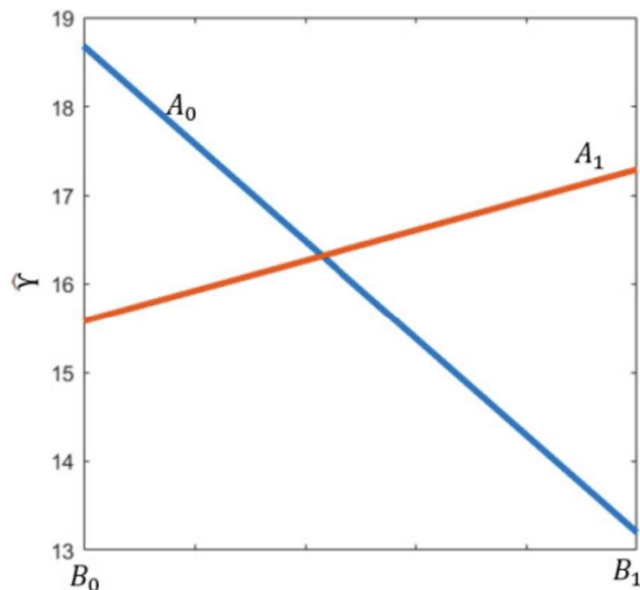


Figure 6. Interaction plot between stress factors A and B.

Table 8. LHD Case I optimized sample allocation.

	Without Interaction					With Interaction				
Experimental Runs	T °C	j(A)	σ (MPa)	P_j	Optimized Sample Allocation	T °C	$j(\frac{A}{cm^2})$	σ (MPa)	P_j	Optimized Sample Allocation
z_1	1	2	3	**0.40**	**20**	1	2	3	**0.48**	**24**
z_2	2	1	4	**0.16**	**8**	2	1	4	**0.24**	**12**
z_3	3	4	2	**0.12**	**6**	3	4	2	**0.12**	**6**
z_4	4	3	1	**0.32**	**16**	4	3	1	**0.16**	**8**

Table 9. LHD Case I optimized stress levels.

Stress Factor	Without Interaction ψ_{i0}	ψ_{i1}	ψ_{i2}	ψ_{i3}		With Interaction ψ_{i0}	ψ_{i1}	ψ_{i2}	ψ_{i3}
T °C	75.42	85.76	97.27	119.52		84.97	96.41	108.23	119.52
$j(\frac{A}{cm^2})$	3651.0	3670.81	5585.16	6848.23		3651.07	4519.44	5583,16	6848.23
σ (MPa)	48.94	98.68	201.30	390.76		3.95	197.35	296.03	390.76

Table 12. Optimized stress levels for without interaction for Case I and Case II.

Experimental Runs	Proposed LHD Case I T °C	j(A)	σ (MPa)		Optimized Stress Levels T °C	j(A)	σ (MPa)
z_1	1	1	4	➡	1	1	4
z_2	2	4	3	➡	2	3	3
z_3	3	3	2	➡	3	2	2
z_4	4	2	1	➡	4	1	1

[8] E. G. Okafor, W. Vinson, and D. R. Huitink, "Effect of Stress Interaction on Multi-Stress Accelerated Life Test Plan: Assessment Based on Particle Swarm Optimization," *Sustainability*, vol. 15, no. 4, p. 3451, Feb. 2023, doi: 10.3390/su15043451.

Can we utilize this understanding to design Reliable high density power modules?

EDA Design flow - PowerSynth

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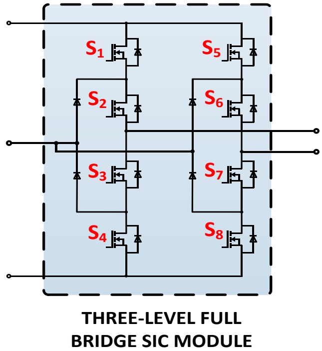
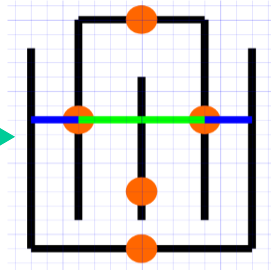
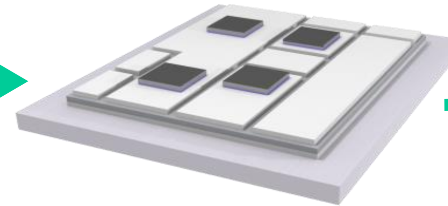
Circuit Schematic



Layout template



Select substrate and components

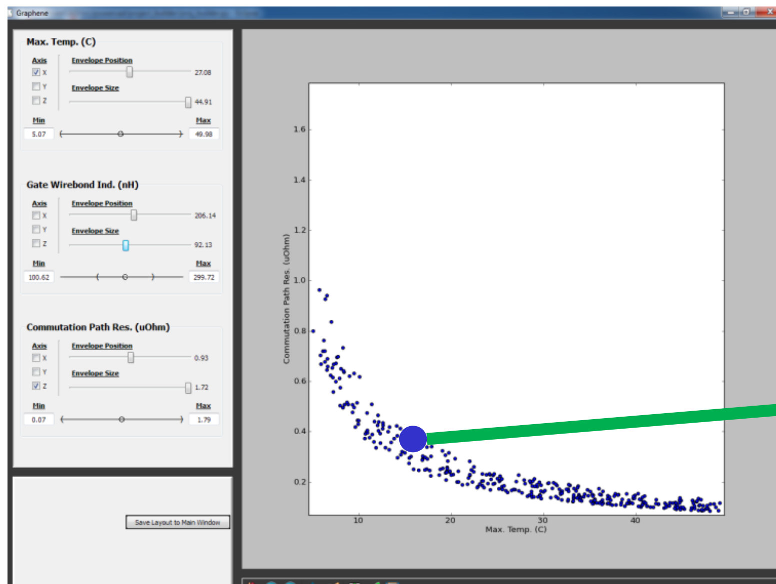


Assign performance measures (objectives)

Step 3: Add Performance Measure

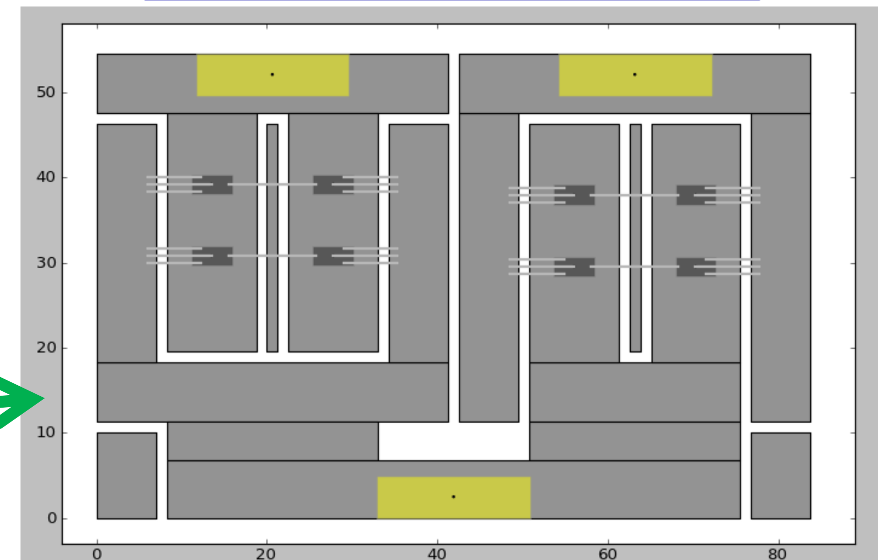
Max. Temp.	Thermal	Max	X
Loop Ind.	Electrical	Inductance	X
Loop Res.	Electrical	Resistance	X
Sub. Cap.	Electrical	Capacitance	X

Perform Layout Optimization



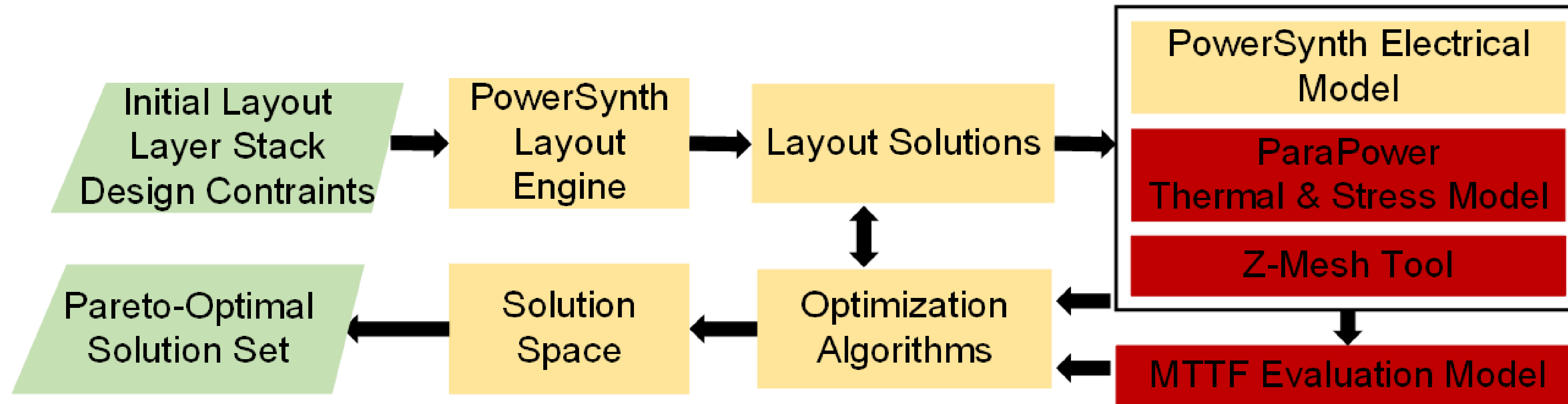
Explore solution set

Export solutions



Automated Design for Reliability

- To handle combo-stress & reliability we should Design for Reliability (DfR)
  - Think of this as an additional step in optimization, where not only are we searching for reduced stressors, but we are also examining the impact that reducing the stressor has on the lifetime of a design



  - This method can also be adapted to account for the potential interaction between multiple stresses if the severity of this interaction is known, *helping to reveal a more wholistic representation of a device's expected life*

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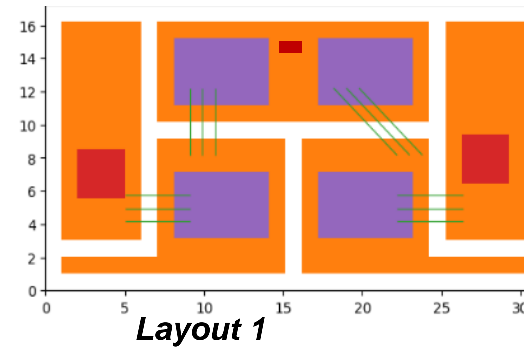
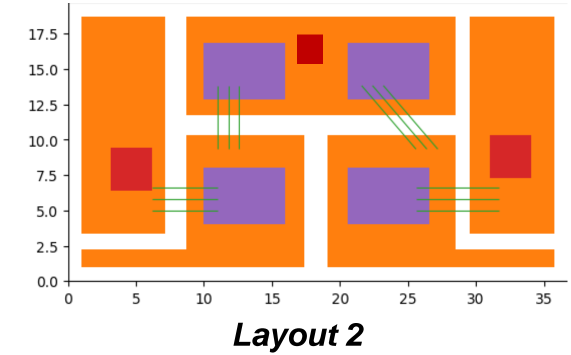
Performance & Optimization Example

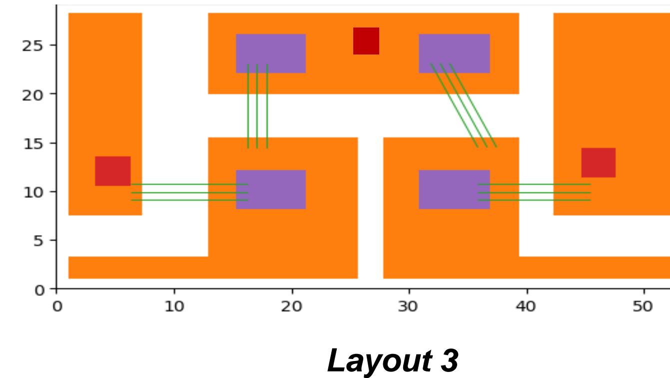
- **Optimization techniques/methods can help to reduce the *severity* of specified stressors, which can improve the expected lifetime of a package**



Layout 1



Layout 2



Layout 3

Layout ID	Parasitic Inductance , nH	Stress, MPa	Wire bond Temperature, C
Layout 1	3.30	198.56	333,58
Layout 2	4.09	166.52	279.75
Layout 3	7.66	137.65	231.25

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Reliability Risk Estimation

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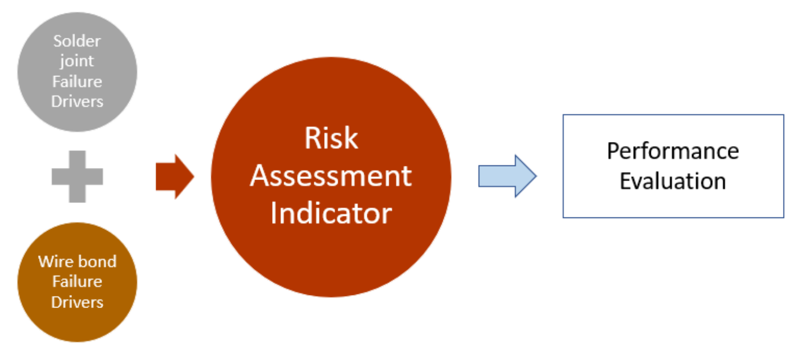
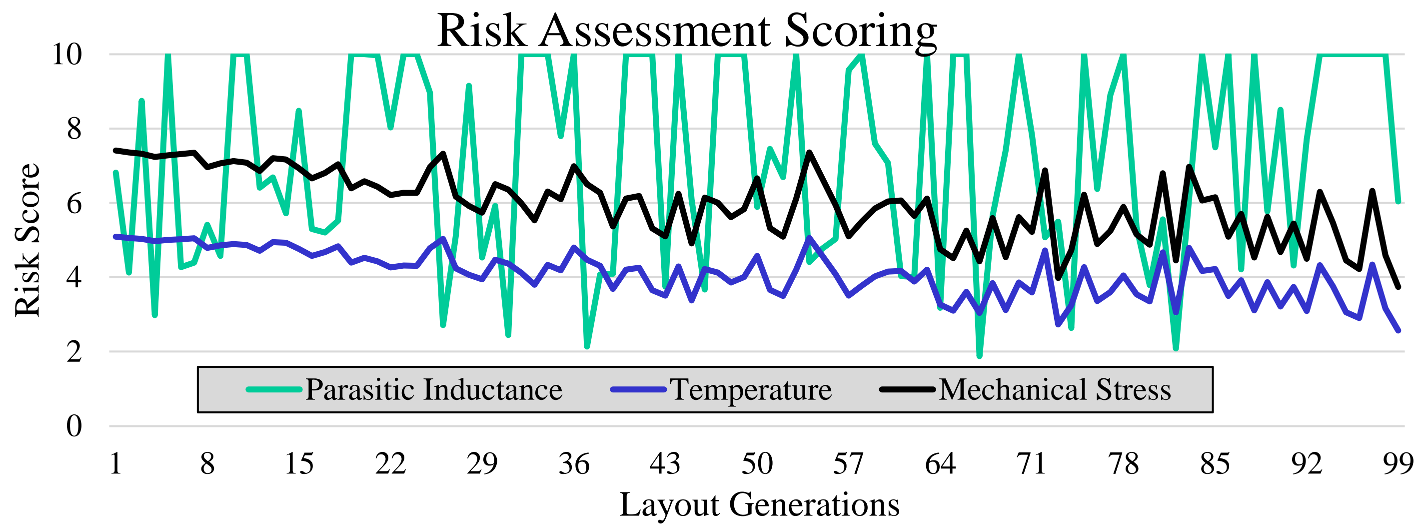
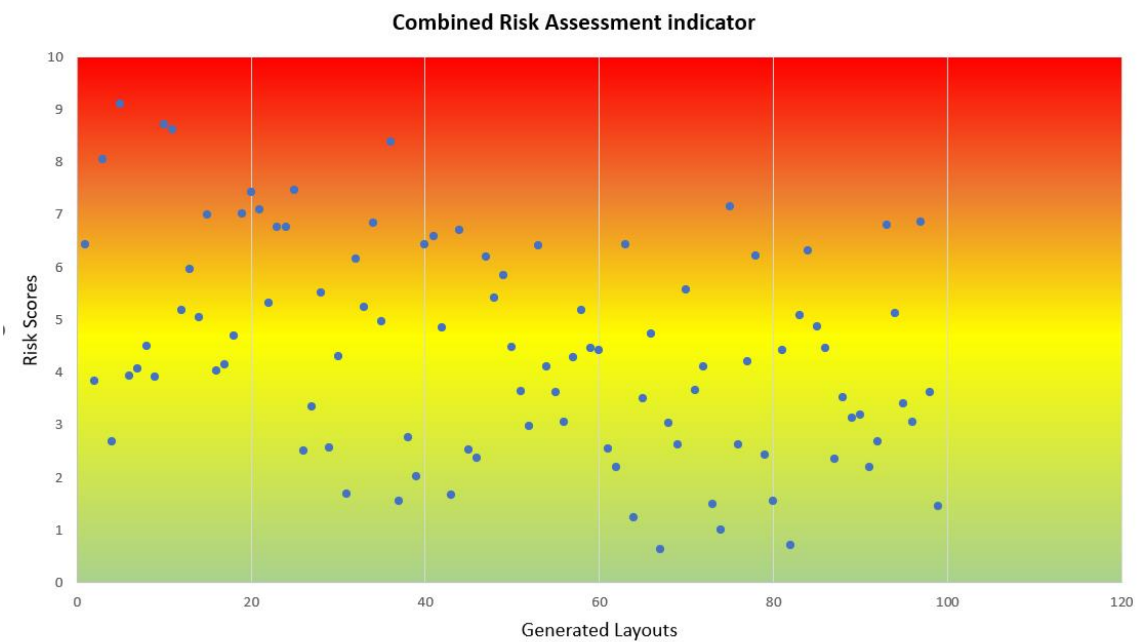
- **Multi-stress interactions and reliability risks**
  - **Package size, power req., & op. cond. w.r.t. power density**
  - **After opt. for any number of factors, reliability will be assessed**
  - **For high power density, overlapping stressors potentially reduce lifetime compared to single stressors → analysis becomes more cumbersome**
  - **Emerging techniques can shed light on this behavior**
    - **A. Designed Accelerated Tests**
    - **B. Module layout risk assessment techniques**
    - **C. Integration of both A. & B.**

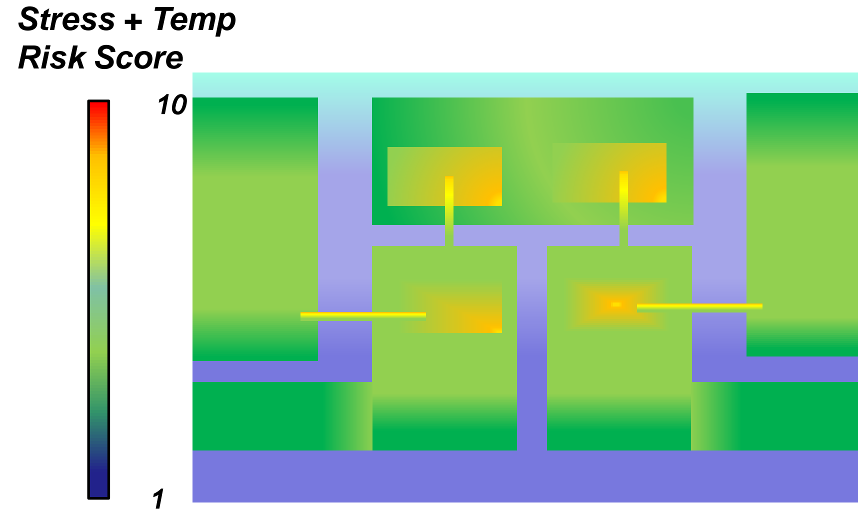


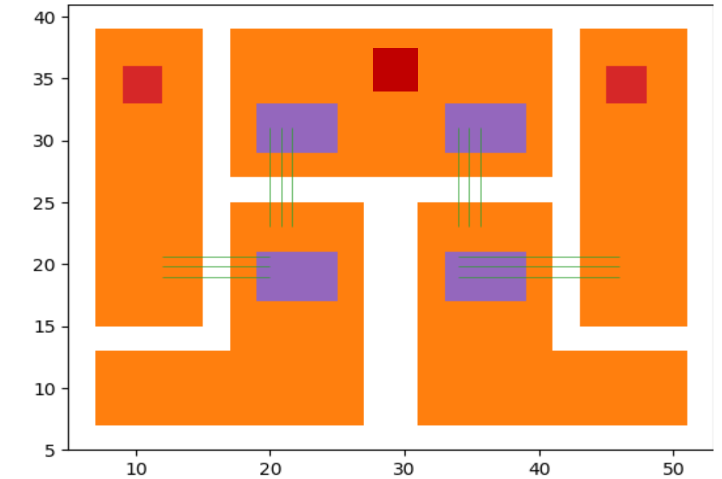




Performance & Optimization in Automated Design

- Reliability risks can be estimated for a designed package at it's expected operating conditions through simulation

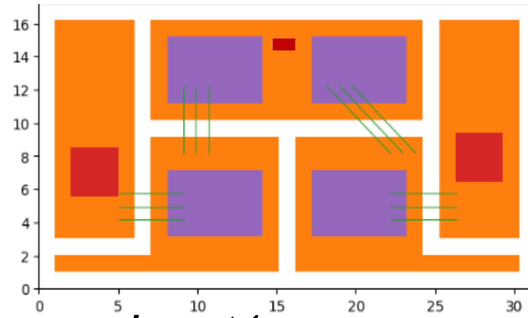




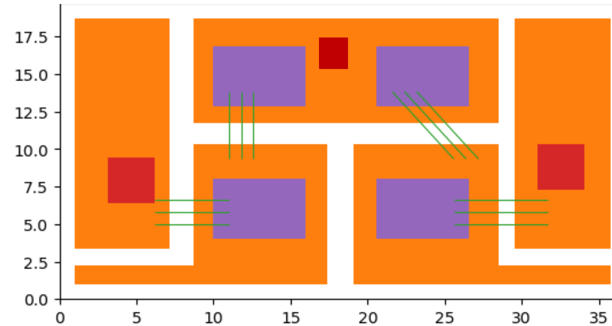
Initial layout

Parasitic Inductance	• 6.82 nH
Stress	• 200 MPa
Wire bond Temperature	• 336 C

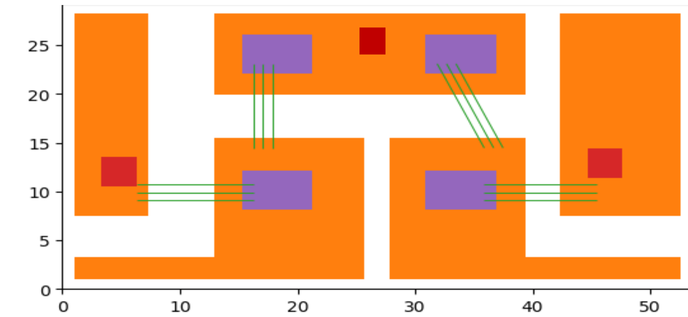
Performance & Optimization



Layout 1

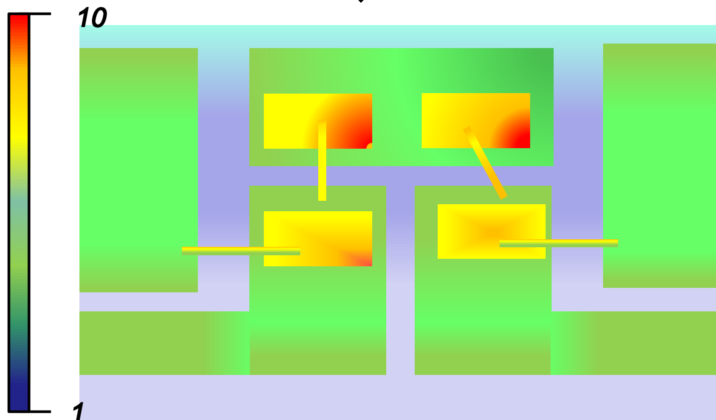


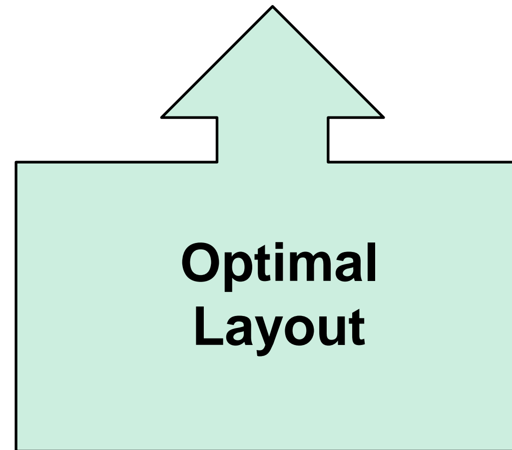
Layout 2

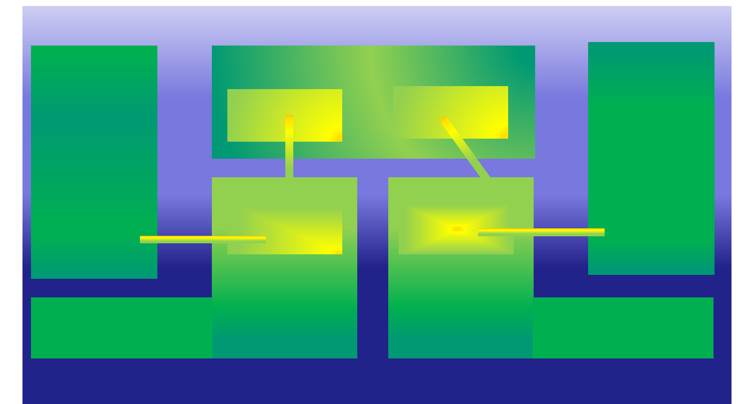


Layout 3

Stress + Temp Risk Score





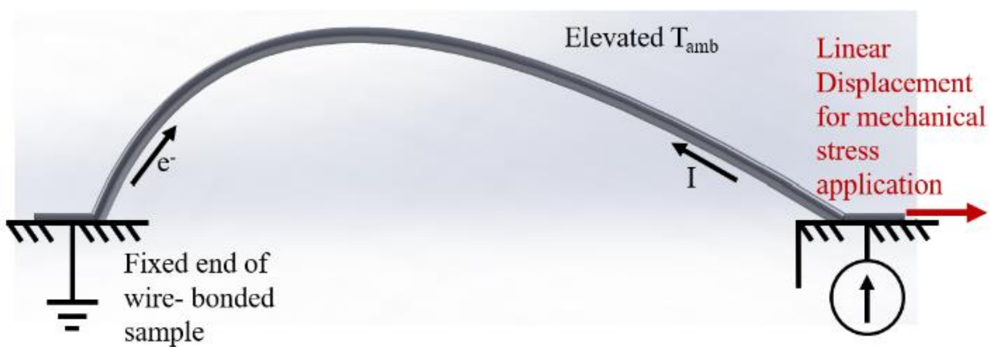


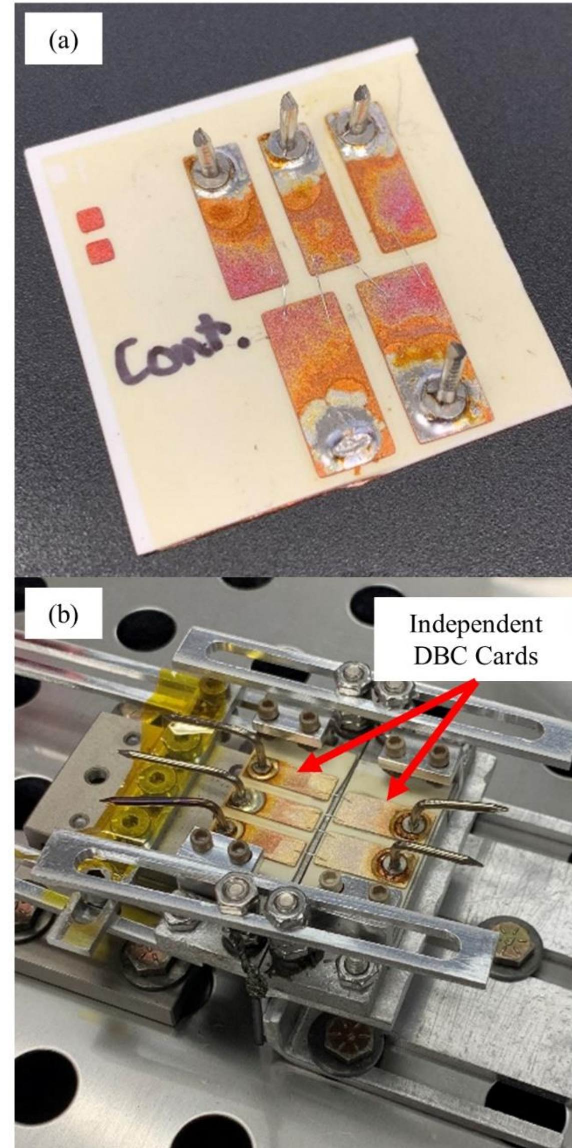
Low Parasitic Inductance

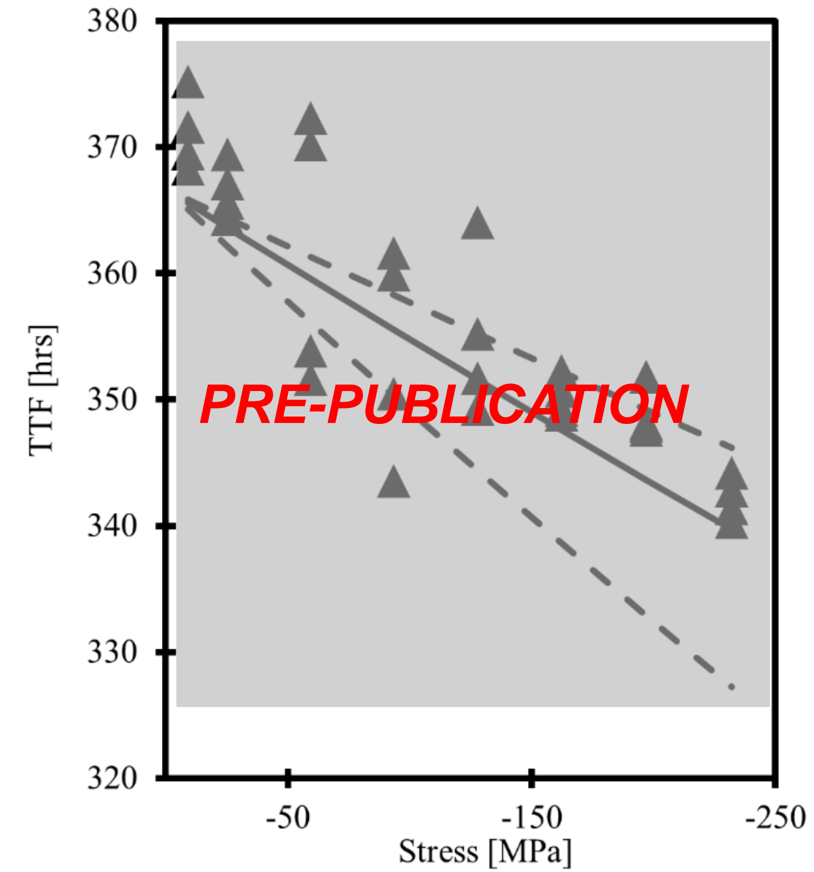
High Parasitic Inductance

How to identify interacting stress effects?

- **Al wire-bonded test vehicle**
  - **Temp., current density, mechanical strain**
  - **Accelerated testing → Life Model**







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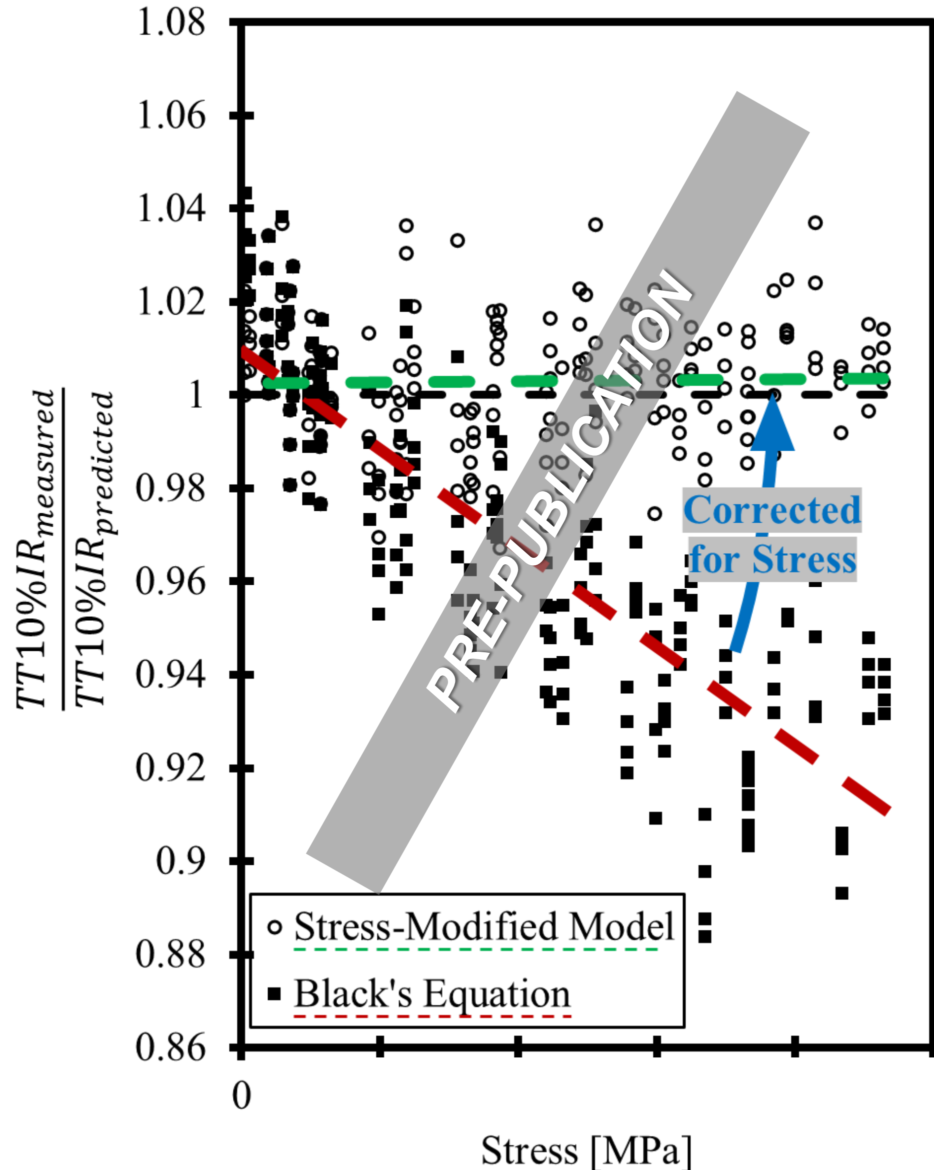
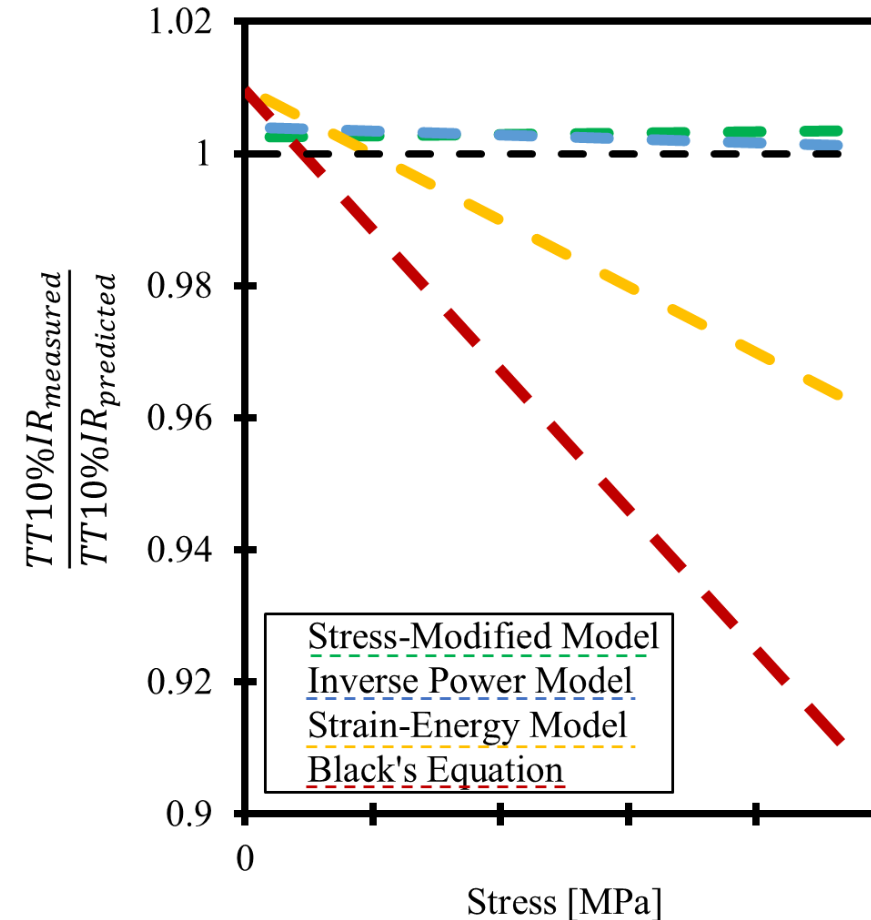
Modeling Stress-altered WB Electromigration



Impact to the predictive quality of EM models

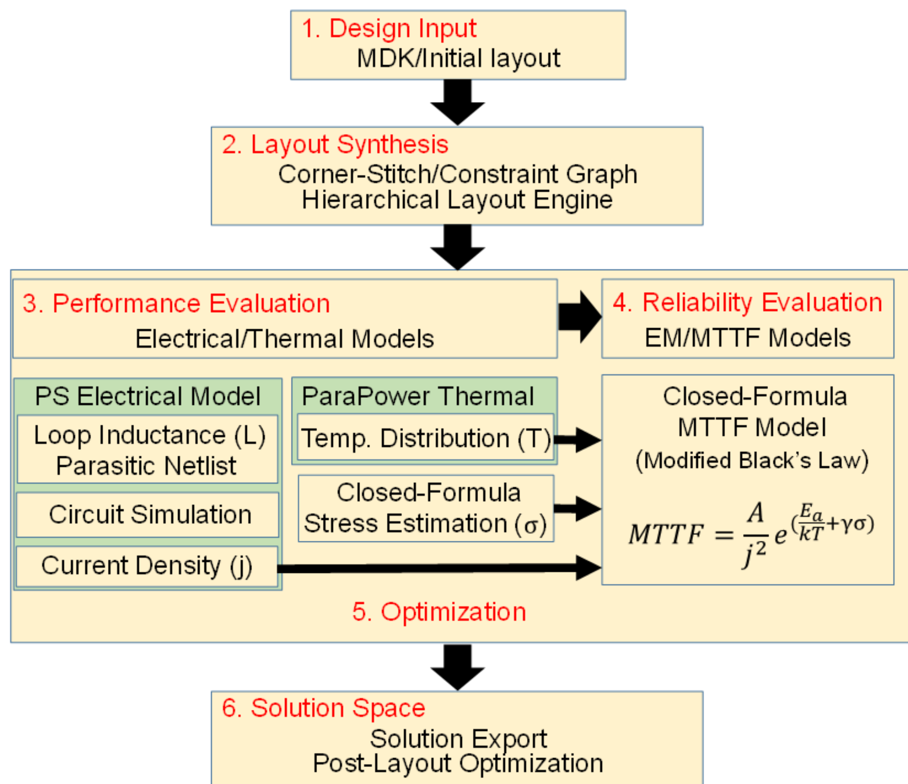
- **Life Model Selection & Significance**

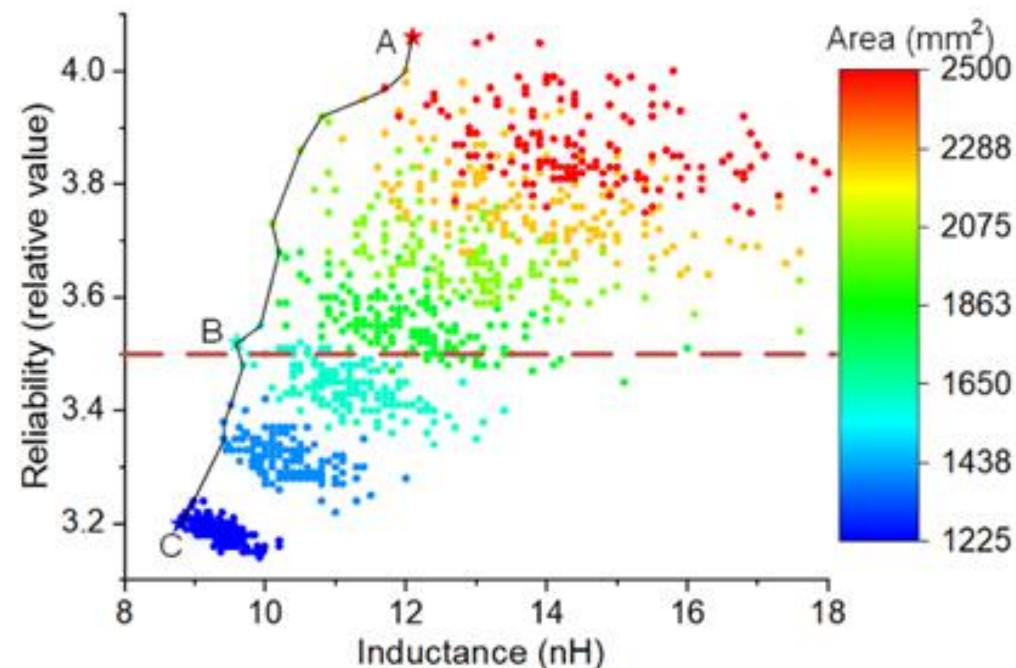


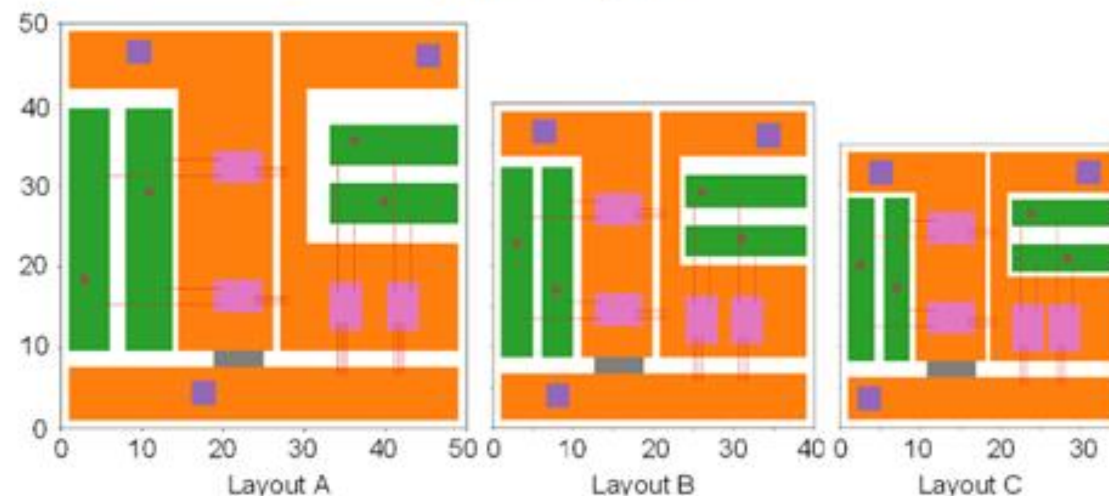
Applying to E-DfR-A: Case Study

➢ Al wire-bonded Multi-chip Power Module

- Integration of results into optimization framework & output results







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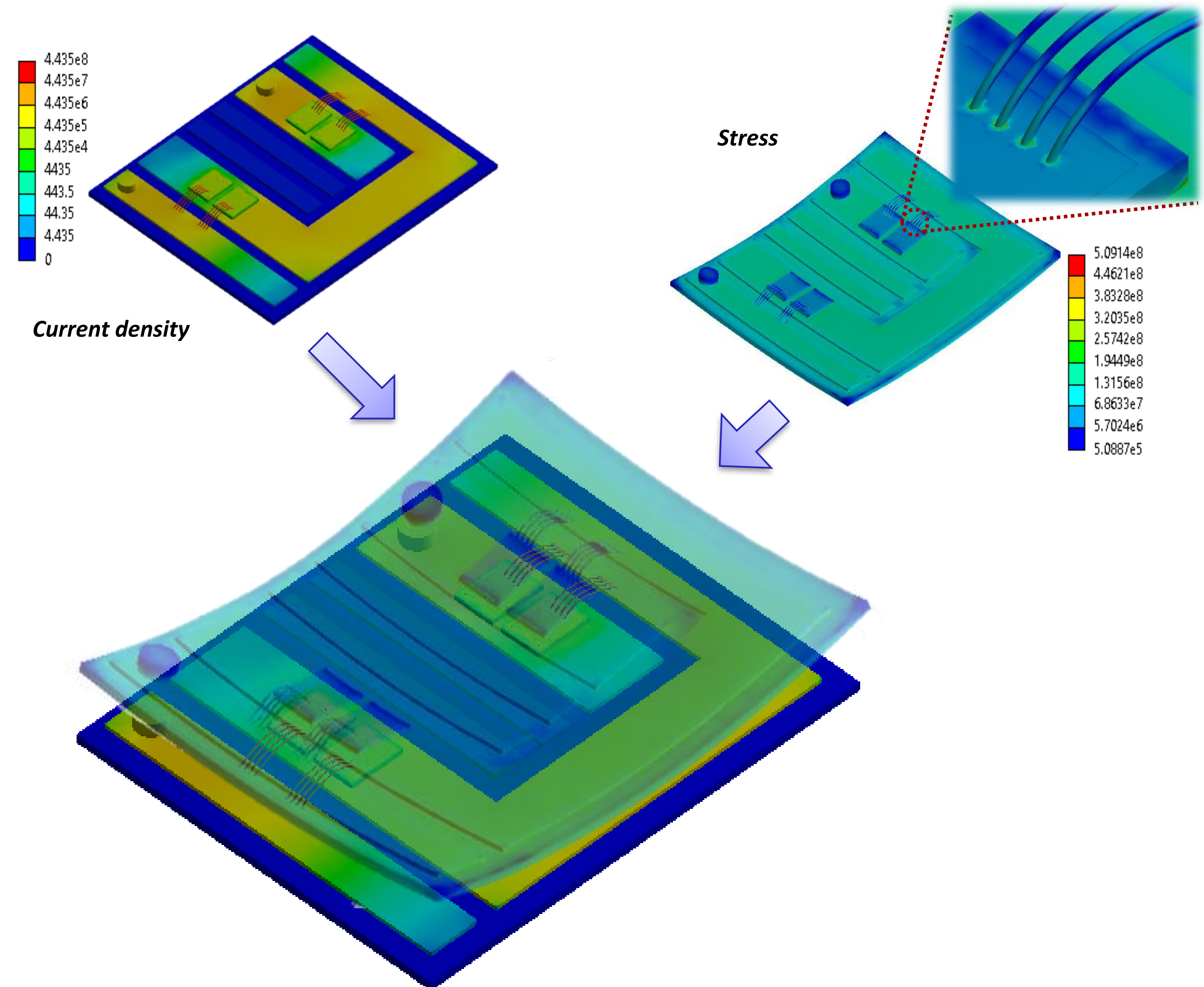
Conclusions & Outlook

- **As power density increases, potential for interaction between multiple stressors will increase**
- **Multi-mechanism failures can reduce the expected lifetime of a component compared to the expectation for a single-mechanism**
- **Accounting for interacting/multi –stress scenarios will be beneficial for next-generation devices**
- ***Development and use* of reliability tools for single & multi-stress analyses will enable the production of robust, power dense, systems**



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Q&A

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