Thermal Runaway Mitigation through Electrothermal Constraints Mapping for MCPM Layout Optimization

Quang Le[1], Md Maksudul Hosain[1], Tristan Evans[1], Yarui Peng[2], H. Alan Mantooth[1]

[1]Electrical Engineering Department
[2]Department of Computer Science and Computer Engineering

Motivation

- SiC bare dies can handle very high operating temperature up to 400°C
- Due to the self-heating effect, before a SiC die gets to this temperature, the materials around it has failed (e.g: solder attach)

→ We would like to consider this in a layout optimization tool such as PowerSynth

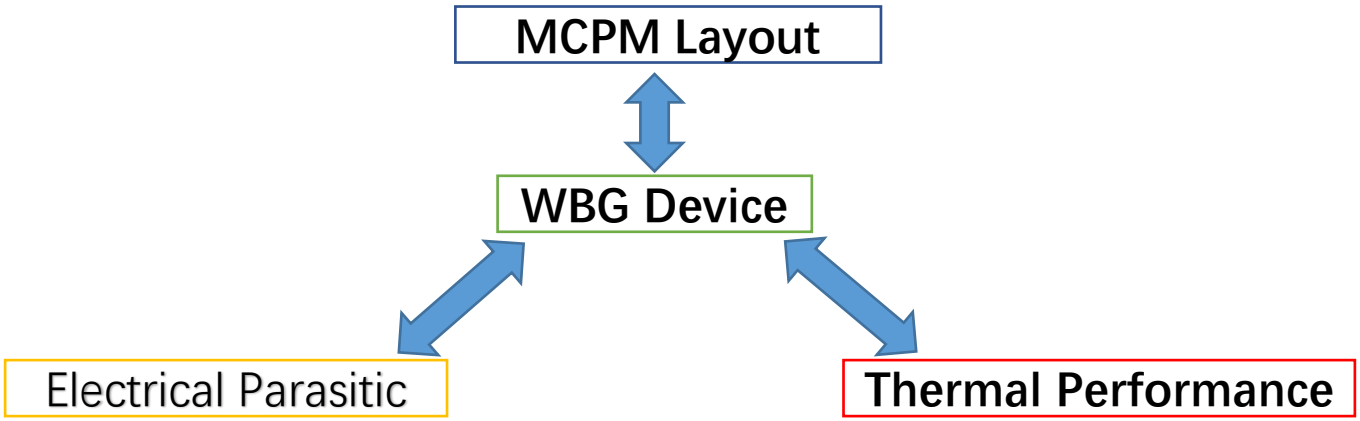
PowerSynth Overview

A layout optimization tool from the University of Arkansas MSCAD group:

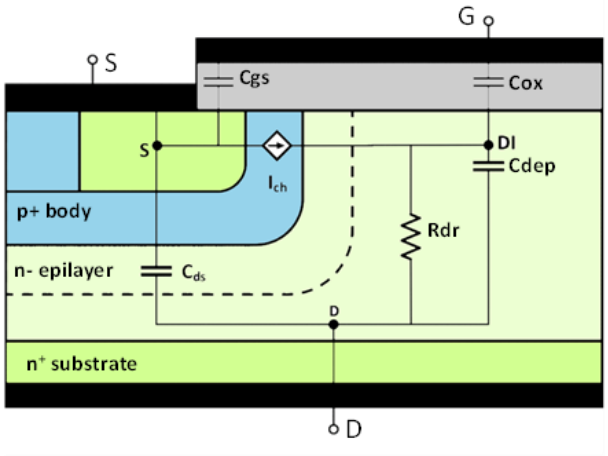
- Automatic Layout Generation and Optimization
- Electrical Parasitic Extraction, Maximum Temperature Analysis
- A Pareto-Front for Solution Space with Trade-offs

In this work:

We combine the knowledge of electrical parasitic, thermal management, and Wide bandgap device modeling for an Electrothermal optimization of the layout.



Incorporation of UA SiC model in Python



SiC Power MOSFET device structure with corresponding parasitic elements

This model considers temperature impact on:

- R_{dson}
- Transconductance (g_{fs})
- Threshold voltage (V_{th})

Has been proven to be accurate for power-loss analysis (within 15%)

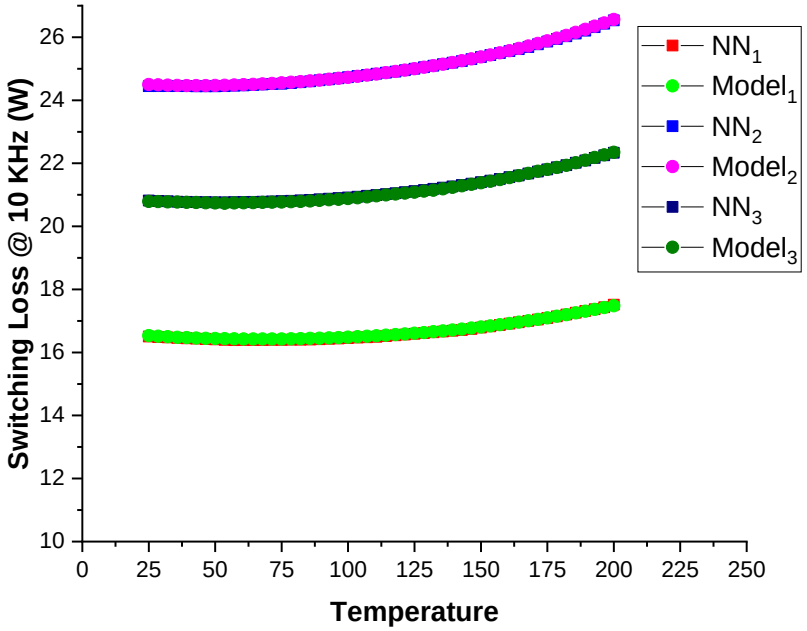
M. Mudholkar et al., “Datasheet driven silicon carbide power MOSFET model,”IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2220–2228, 2014.

ANN-based Model for Switching Loss Table

An analytical power loss model [1] has been reimplemented for the study.

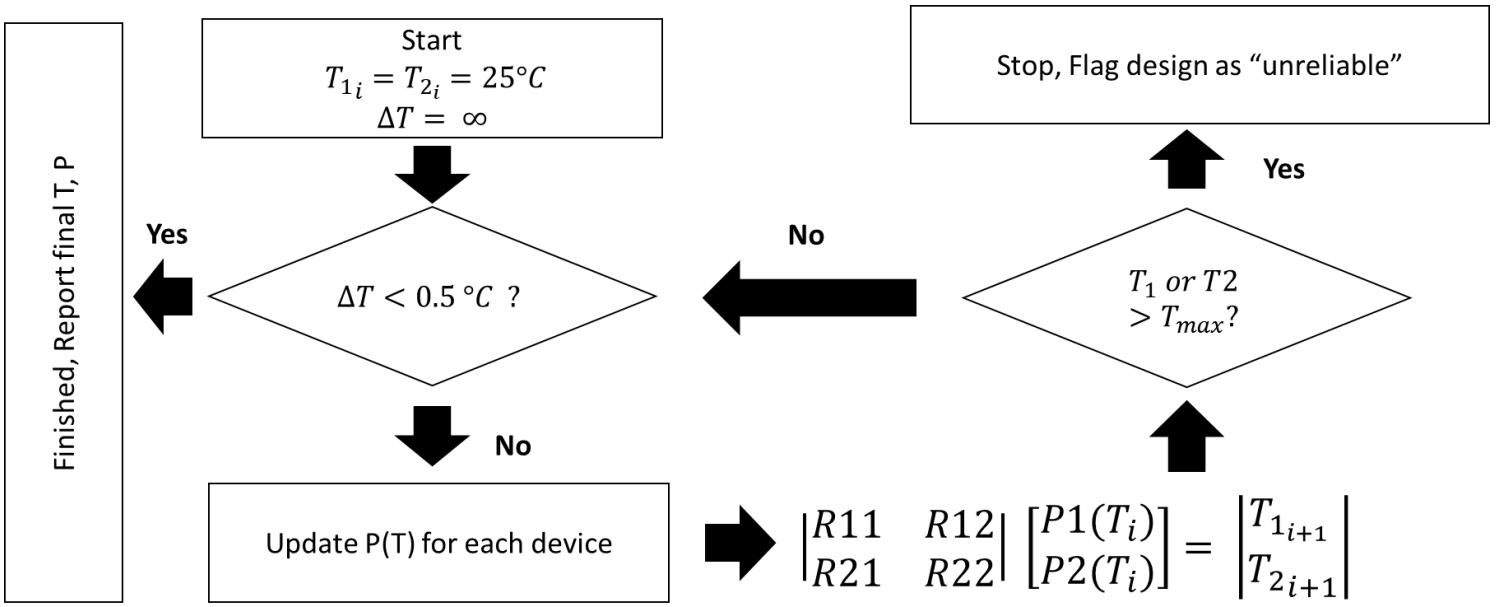
A Neural Network model has been used as a Look Up Table (LUT) to store the relationship among parasitics elements and temperature on switching loss.

- Remove some computational overhead in Python
- Can be stored and reused for a different layout with the same circuit



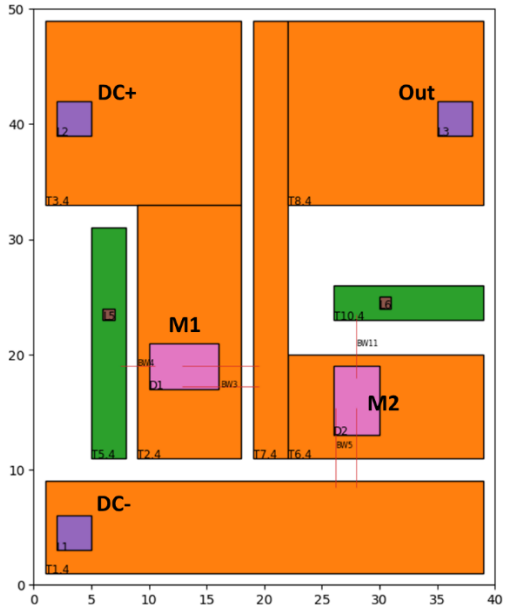
[1] D. Christen and J. Biela, “Analytical Switching Loss Modeling Based on Datasheet Parameters for mosfets in a Half-Bridge,”IEEE Trans. Power Electron., vol. 34, no. 4, pp. 3700–3710, 2019.

Successive Approximation Method

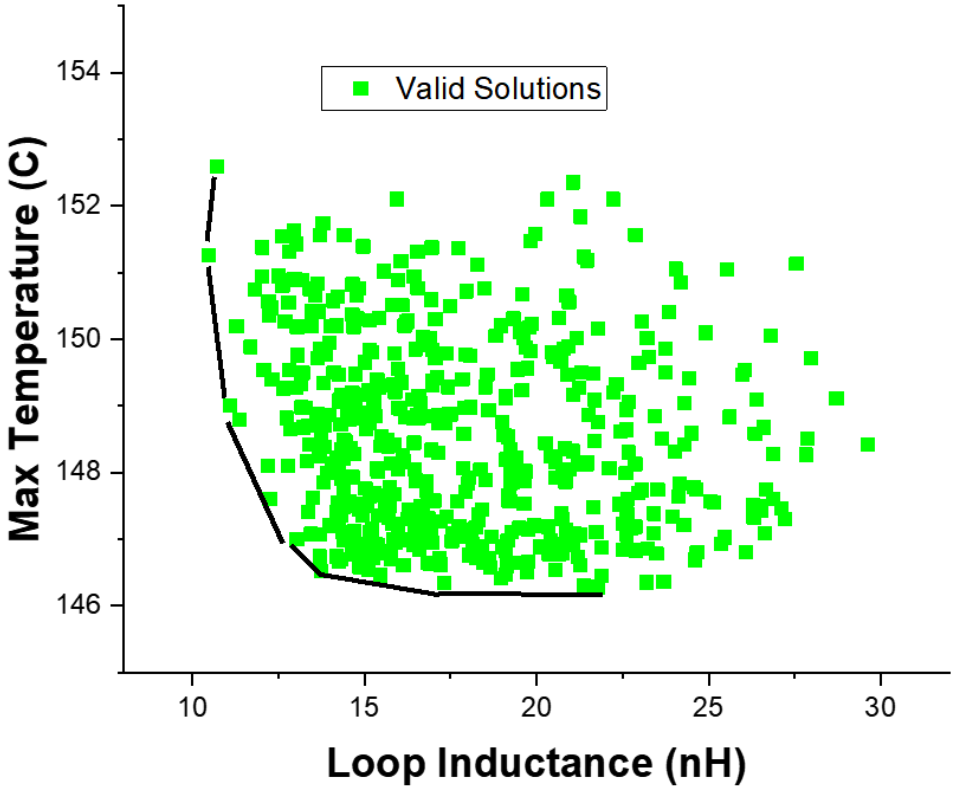


The successive approximation method

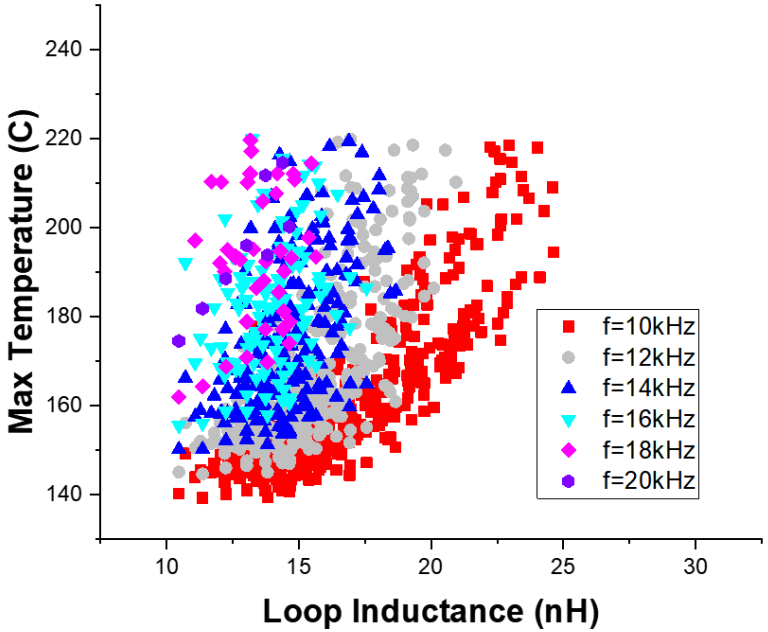
Electrothermal Optimization Study (1/2)



Half-bridge Layout for the study



Electrothermal Optimization Study (2/2)



Solution spaces for various operating frequencies

Load current is 60 A and DC-DC voltage is 600V

- Electrical and thermal netlist are extracted.
- Successive approximation model has been run for all layouts.
- Max temperature is 220 °C
- h_{conv} set to 500 (W/m^2K) (air flow).

Conclusion and Future Work

In this study:
We have combined the electrical parasitic and thermal models in PowerSynth and performed a Co-Electrothermal Optimization to find the true trade-off between electrical and thermal aspects.

Key takeaways from the study:
- Layout with higher loop inductance has worsened thermal performance.
- The model allows us to push the limit of the circuit through the switching frequency sweep.

Future Work:
- Possible to include heatsink study in the future.
- Incorporates current sharing among different devices.

PowerSynth References

[1] Tristan Evans, Quang Le, Shilpi Mukherjee, Imam Al Razi, Tom Vrotsos, Yarui Peng, and H. Alan Mantooth, “Powersynth: A Power Module Layout Generation Tool”, IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5063–5078, Jun 2019, Highlighted Paper.

[2] Imam Al Razi, Quang Le, Tristan Evans, Shilpi Mukherjee, H. Alan Mantooth, and Yarui Peng, “PowerSynth Design Automation Flow for Hierarchical and Heterogeneous 2.5D Multi-Chip Power Modules”, IEEE Transactions on Power Electronics, vol. 36, no. 8, pp. 8919-8933, 2021.

[3] Quang Le, Imam Al Razi, Tristan Evans, Shilpi Mukherjee, Yarui Peng and H. Alan Mantooth, "Fast and Accurate Parasitic Extraction in Multichip Power Module Design Automation Considering Eddy-Current Losses," in *IEEE Journal of Emerging and Selected Topics in Power Electronics. Sept 2022.*

Thank you ! Questions ?