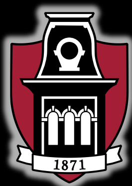
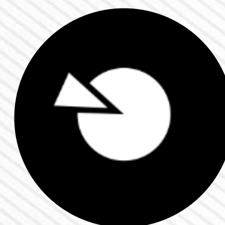


Ph.D. Dissertation



Constraint-Aware, Scalable, and Efficient Algorithms for Multi-Chip Power Module (MCPM) Layout Optimization

Imam Al Razi

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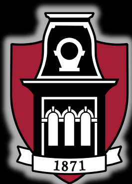

Power Electronics is Everywhere

- ❑ Electric automobiles
- ❑ Aircrafts
- ❑ Smart grid
- ❑ Consumer electronics
- ❑ ....

ELECTRIC GENERATION

COMMERCIAL

INDUSTRIAL

RESIDENTIAL

Power converters are essential parts of power systems

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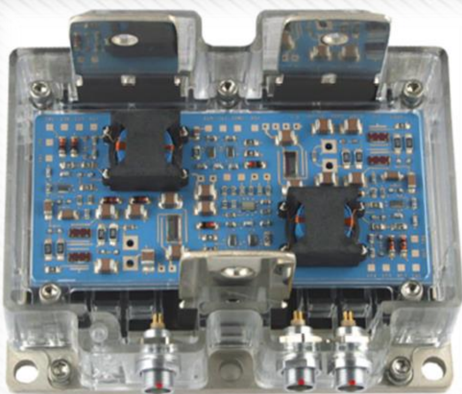
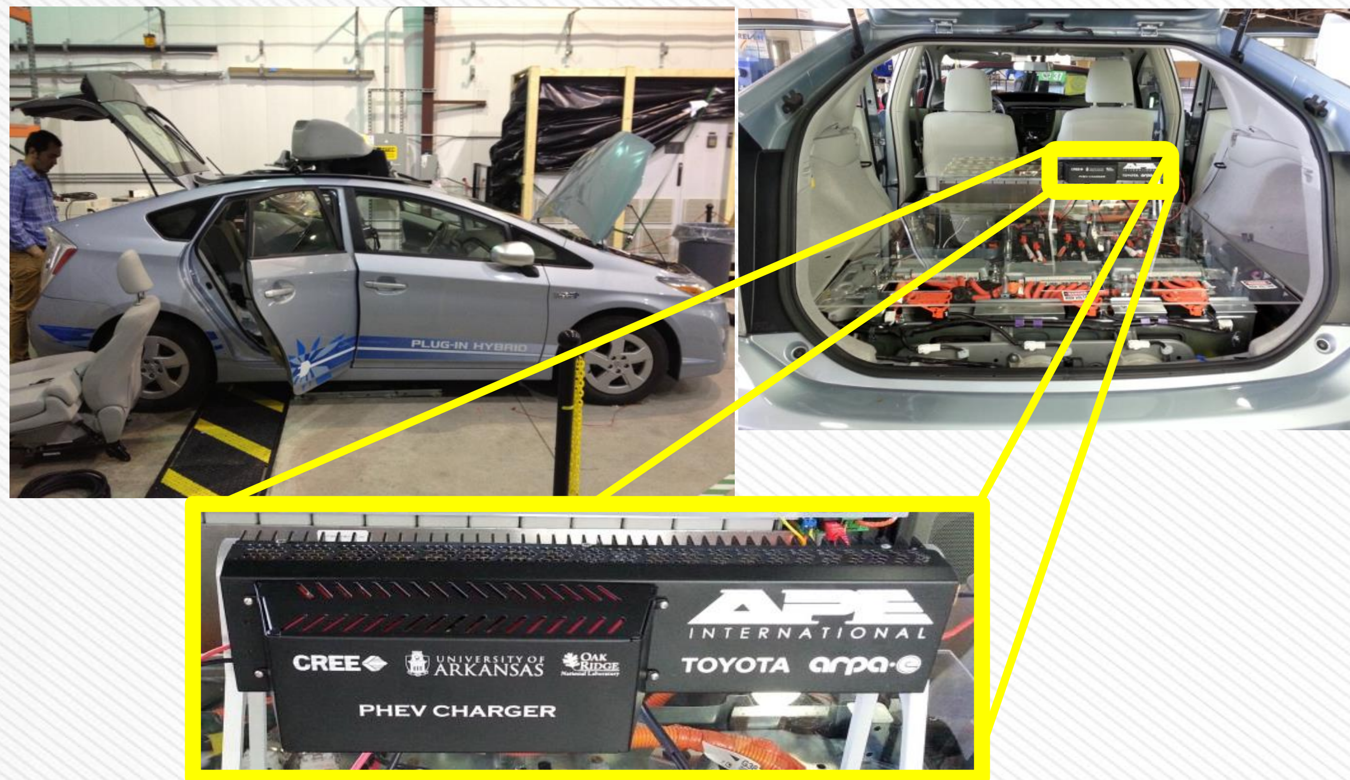
Multi-Chip Power Modules

- ❑ **Foundation element of power converters**
- ❑ **Integrates power devices and control circuitry in a single package**
- ❑ **Wide Bandgap Devices (SiC/GaN)**
  - Increased power density
  - New packaging technologies
  - Heterogeneous integration



R&D 100 Award-Winning MCPM Design



MCPM layout design complexity is increasing

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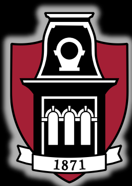
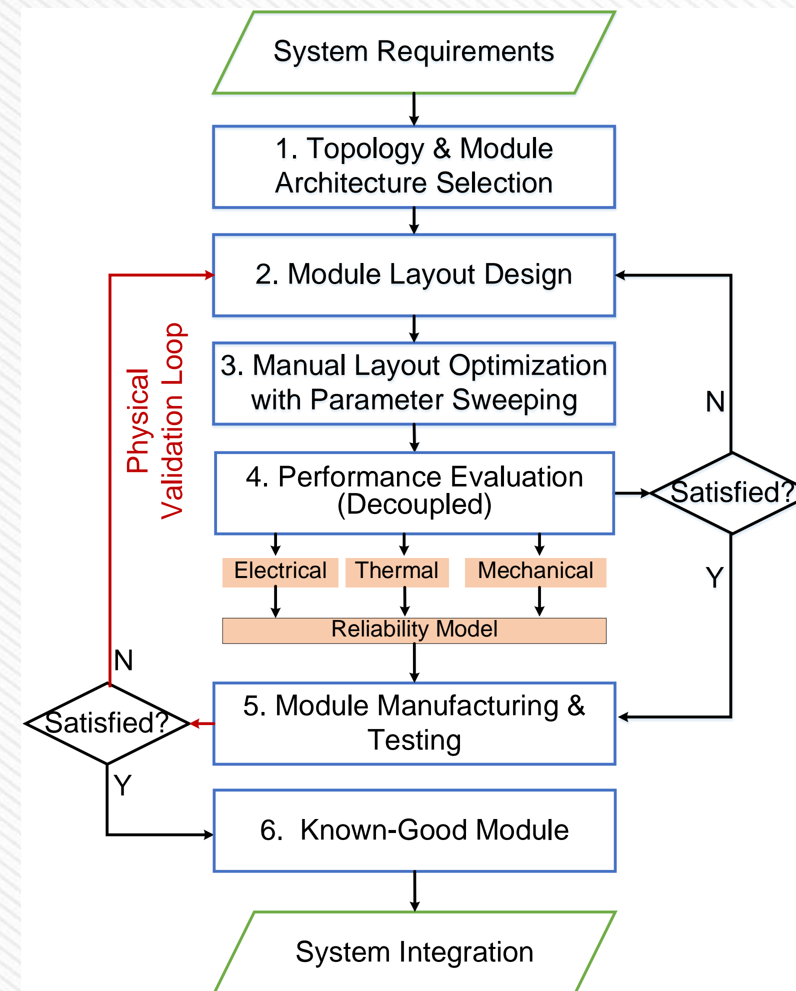


Traditional Design Flow

❑ Traditional:

- Manual, iterative
- Computationally expensive
- Single solution at a time
- Interaction with multiple FEA tools
- No known-good module before fabrication and testing
- Requires human expertise



Traditional design flow

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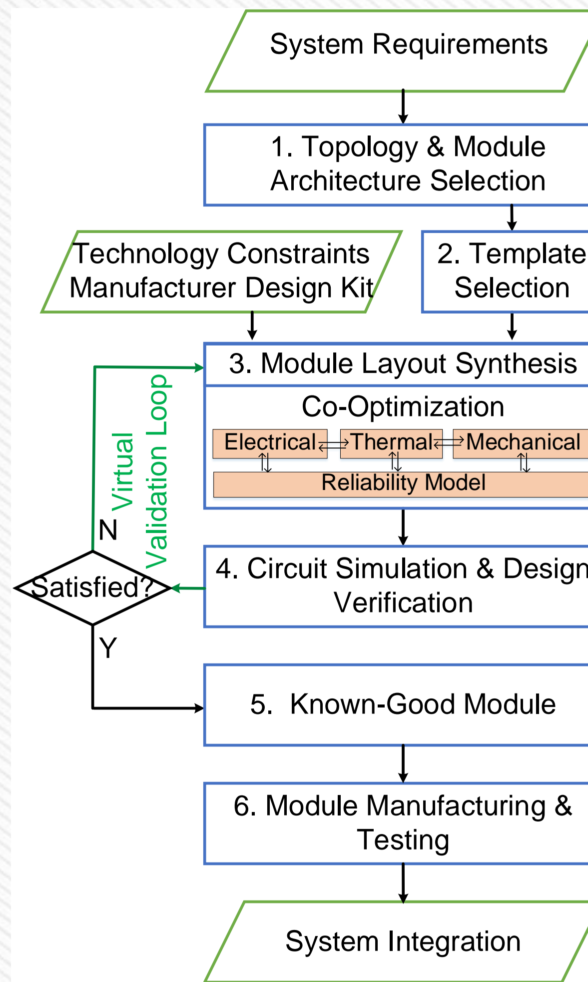
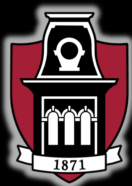
Automated Design Flow

- **Automated:**
  - Reduced time and cost
  - Reduced-order modeling
  - Large solution space at a time
  - Multi-objective optimization
    - Electrical
    - Thermal
    - Mechanical
    - Reliability
  - Known-good module before fabrication

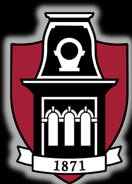


Automated design flow



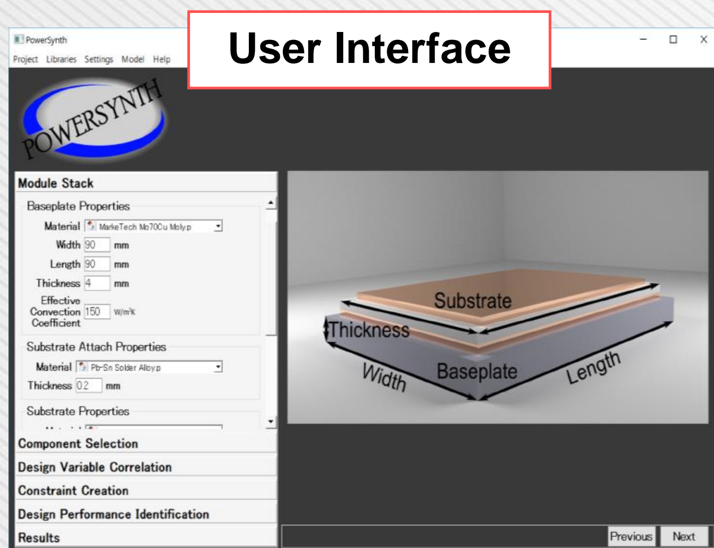
Power Module Design Automation Efforts

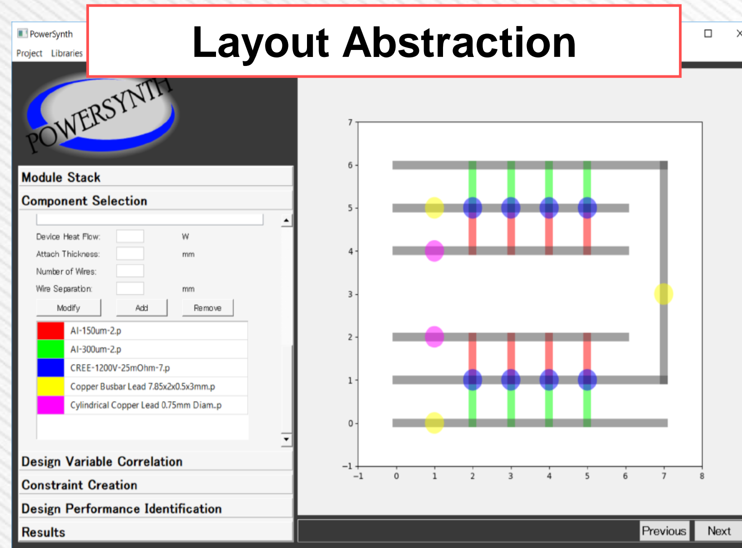
Methodology Features	Puqi Ning et. al. (2017)	Shuhei et. al. (2021)	Zhou et. al. (2022)
Initial layout	Simplified	Simplified	Not required (Template library & Netlist)
Layout generation method	Sequence pair	Parameter sweep	Integer linear programming & Block graph model
Layout types	2D	2D	2D
Scalability	N/A	N/A	N/A
Interconnection technology	Wire bond	Wire bond	Wire bond
DRC checking	Required	Required	Not required
Solution space	Limited	Limited	Limited
Hierarchical optimization	N/A	N/A	N/A
Performance evaluation	Discrete model	Finite element analysis	In-house model
Objectives	Area and power loop inductance	Power loop inductance & Junction temperature	Multiple loop inductance & Junction temperature
Reliability optimization	N/A	N/A	N/A
Optimization algorithm	Evolution (GA)	Evolution (NSGA II)	Evolution (NSGA II)

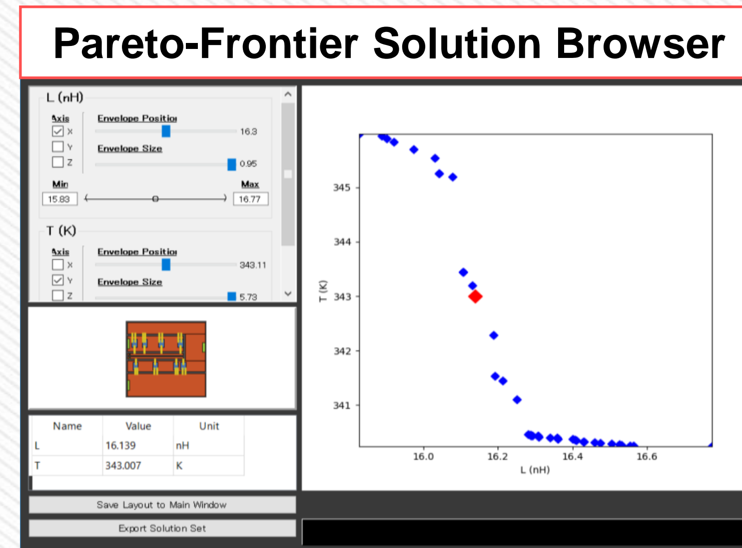


Layout Synthesis and Co-Optimization

- PowerSynth: An EDA tool with the goal streamlining the MCPM design process in a multi-objective optimization framework.







T. M. Evans *et al.*, "PowerSynth: A Power Module Layout Generation Tool," in *IEEE Transactions on Power Electronics,2019* (Highlighted paper)

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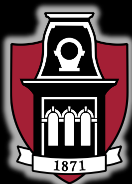
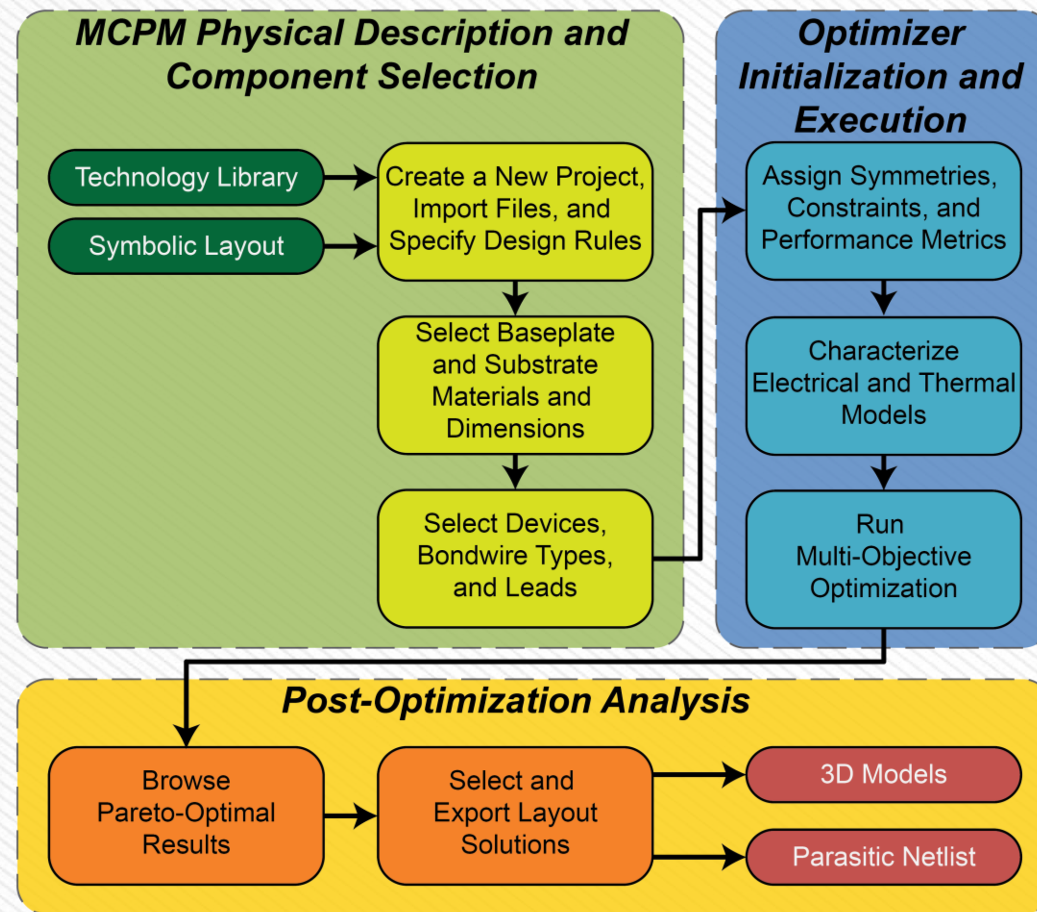


First PowerSynth Version & Motivations

- **Features:**
  - Built-in technology library
  - Symbolic layout input
  - Matrix-based layout generation
  - Reduced-order and fast electrical, thermal models
  - Multi-objective optimization through GA
  - Pareto-front solution browser
  - Export solution to commercial FEA tools
  - Post-layout optimization: filleting sharp corners
  - Parasitic netlist extraction
- **Limitations:**
  - Fixed layer stack
  - Simple 2D layout geometry only
  - Limited solution space
  - Requires iterative DRC



PowerSynth v1.1 work flow

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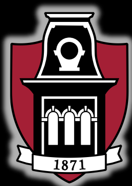

Outline

- Introduction
- Contributions
- Constraint-Aware Layout Engine
  - Layout Representation
  - Methodology
  - Results
    - Minimum-Sized Results
    - 2.5D MCPM Layout Optimization & Hardware Validation (Demonstrated in Proposal Defense)
    - 3D MCPM Layout Optimization & Hardware Validation
- Reliability Optimization
  - Thermal Cycling Impact Minimization
  - Electromigration (EM) Impact Minimization
- Conclusion & Future Work

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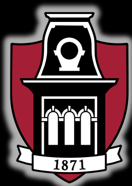

Dissertation Contributions

❑ PowerSynth 2 Architecture

Design Flow Core: 2D/2.5D/3D Designs, Python 3.8, QT 5.12, Windows/Linux External Tools

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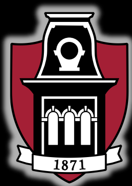

Other Group Members' Contributions

❑ PowerSynth 2 Architecture

Export & Simulation | Solution Database | Netlist Exporting | Simulation Export | Export Functions

Optimization Toolbox | Genetic Algorithms | Machine-Learning | Simulated-Annealing | Pre/Post-Layout Optimization

Layout Evaluation | Electrical model | Thermal model | Reliability models: Stress | EM | Transient Thermal | PD

Layout Synthesis | Constraint (DRC) | Connectivity (LVS) | Layout Generation

Data Input | Object-based layout representation | MFG Design Kit (MDK) | Embedded scripting environment

Graphical User Interface (GUI)

Command Line Interface (CLI)

External Tools: EMPro Q3D | Matlab Scikit-Learn | Z-Mesh Tool | ParaPower FastHenry | HSPICE | ANSYS

Design Flow Core: 2D/2.5D/3D Designs, Python 3.8, QT 5.12, Windows/Linux

External Tools

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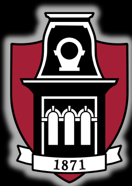

Contribution Outline

- **Layout Engine Updates**
  - Layout representation technique
  - Constraints
  - Layout generation
- **Optimization**
  - Genetic algorithm
  - Reliability optimization
    - Electromigration (EM)
    - Thermal cycling
- **Solution Database & Export**
- **User Interfaces: CLI & GUI**
- **PowerSynth v2.0 Release**

Design Flow

- Export & Simulation
- Optimization Toolbox
- Layout Evaluation
- Layout Synthesis
- Data Input

6 Graphical User Interface (GUI)

6 Command Line Interface (CLI)

Layer				
Export & Simulation	5 Solution Database	Netlist Exporting	Simulation Export	5 Export Functions
Optimization Toolbox	4 Genetic Algorithms	Machine-Learning	Simulated-Annealing	Pre/Post-Layout Optimization
Layout Evaluation	Electrical model	Thermal model	3 Reliability models: Stress, EM, Transient Thermal, PD	
Layout Synthesis	2 Constraint (DRC)	Connectivity (LVS)	2 Layout Generation	
Data Input	1 Object-based layout representation	MFG Design Kit (MDK)	Embedded scripting environment	

External Tools:

- EMPro Q3D
- Matlab Scikit-Learn
- 3 Z-Mesh Tool
- ParaPower
- FastHenry
- 3 HSPICE
- ANSYS

Core: 2D/2.5D/3D Designs, Python 3.8, QT 5.12, Windows/Linux

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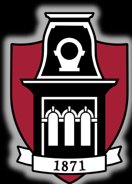
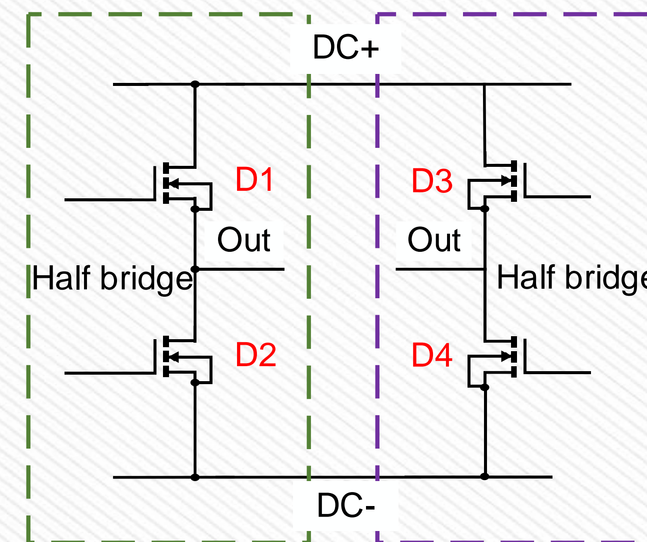


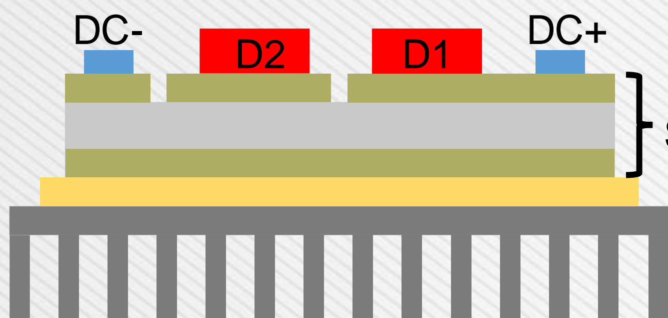
2D-2.5D-3D Module Definition

- **Definition under PowerSynth scope:**
  - 2D: One device layer with routing layers on the same substrate
  - 2.5D: Multiple 2D designs connected on a supporting 2D plane
  - 3D: Multiple device layers stacked vertically on the same substrate

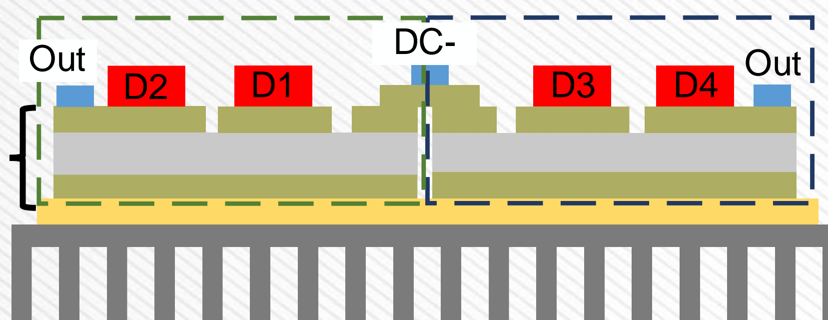


Circuit schematic of a full-bridge module

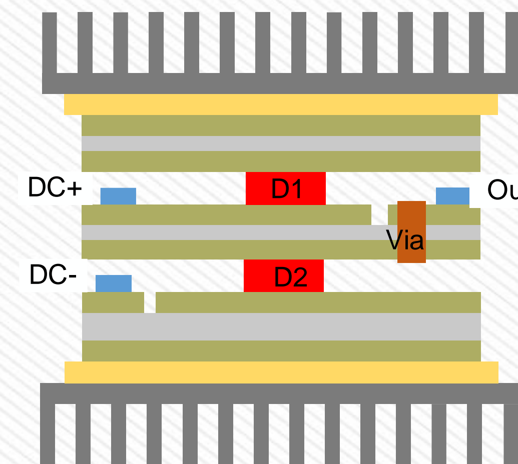
Lead Device Ceramic Copper Baseplate Heat Sink



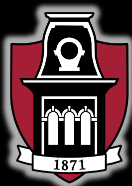
2D Half-bridge power module



2.5D Full-bridge power module



3D half-bridge power module



Preliminary Research and Proposal

❑ Already Presented in Proposal Defense

- **Flat-level 2D MCPM Layout Optimization**
  - Constraint-Aware Layout Engine Baseline Version
  - Reliability Constraints Implementation & Results
- **Hierarchical 2D/2.5D MCPM Layout Optimization**
  - Layout Engine Updates
    - Hierarchical layout geometry script
    - Hierarchical corner-stitch and constraint graph evaluation method
    - Benefits of hierarchy consideration
    - 2D/2.5D CAD flow with hardware validation

❑ Proposed for Dissertation

- **Algorithm updates for generic handling of state-of-the-art 3D packaging technologies**
- **Develop genetic algorithm framework for 2D/2.5D/3D layouts**
- **GUI for PowerSynth v2.0 release**
- **Hardware validation of 3D CAD flow**

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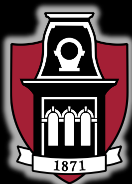

Outline

- Introduction
- Contributions
- **Constraint-Aware Layout Engine**
  - **Layout Representation**
  - Methodology
  - Results
    - Minimum-Sized Results
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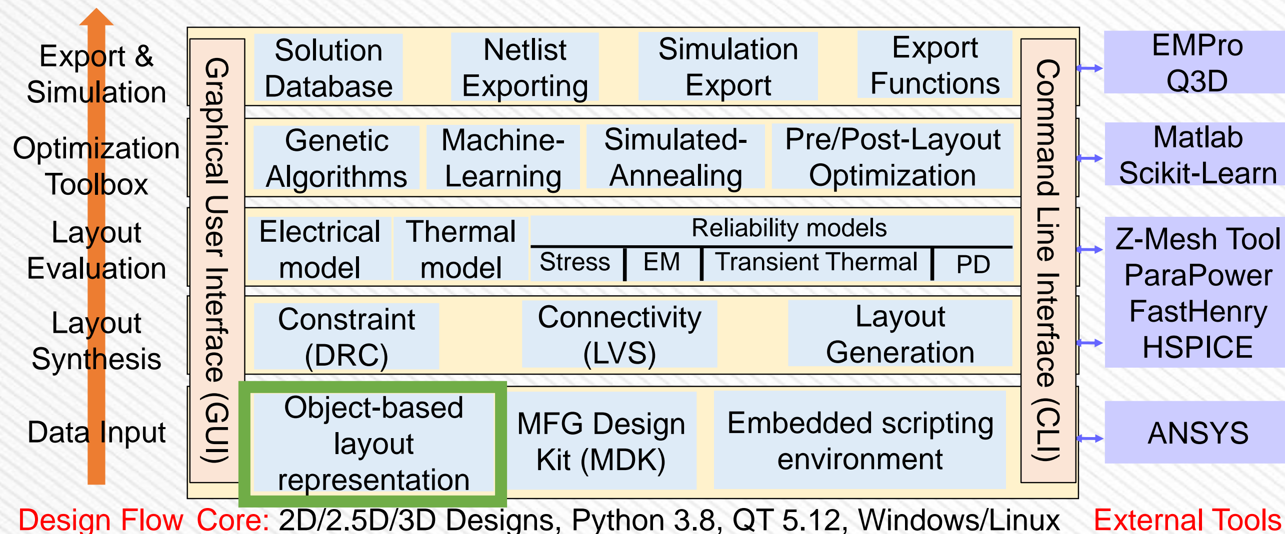
- Reliability Optimization
  - Thermal Cycling Impact Minimization
  - Electromigration (EM) Impact Minimization
- Conclusion & Future Work



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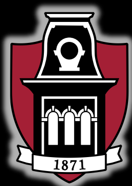
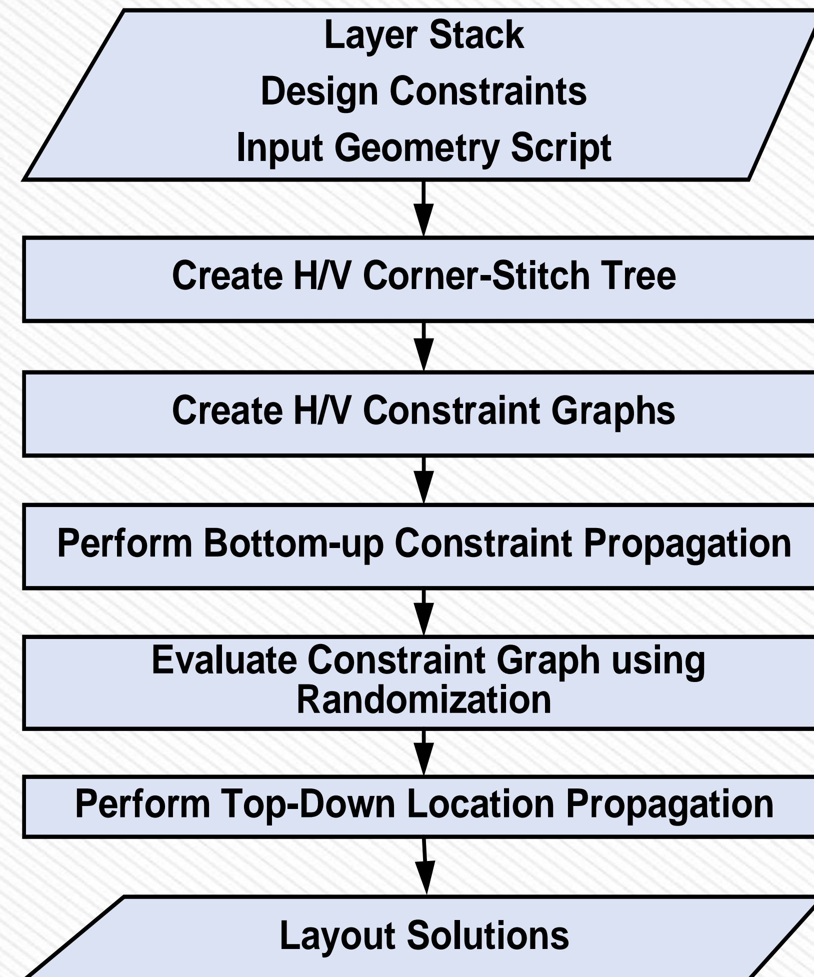


Constraint-Aware Layout Engine

- **Features:**
  - **Generic, hierarchical layout description script**
  - **Generic, scalable layer stack**
  - **Different types of constraints : design/reliability**
  - **100% DRC-clean solutions**
  - **Hierarchical approach: 2D/2.5D/3D layout handling**
  - **Generic, scalable, and efficient methodology→ SOTA 2D/3D packaging solutions**
    - Hierarchical corner stitch data structure: layer based geometry representation
    - Hierarchical constraint graph (CG) evaluation: guarantees DRC-clean solutions
    - Randomization: layout solution generation method (exhaustive search)
  - **Three types of layout generation capability:**
    - Minimum-sized (Mode 0)
    - Variable-sized (Mode 1)
    - Fixed-sized (Mode 2)



Layout generation workflow

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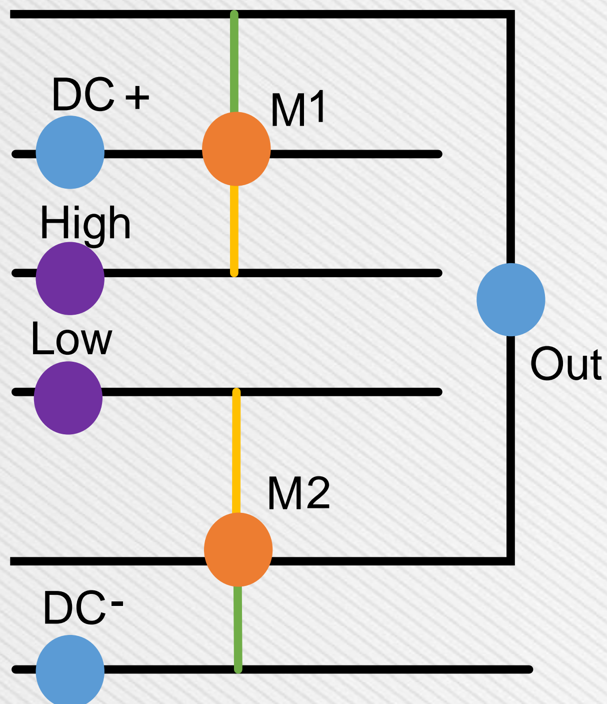
Layout Representation Technique

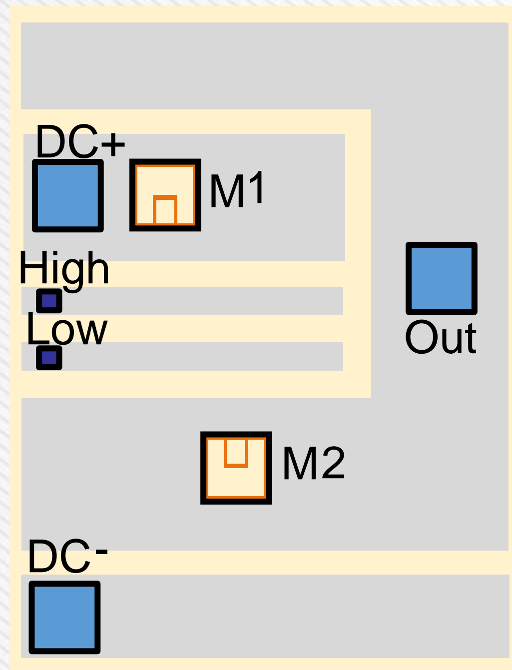
❑ Progression Timeline

PS v1.1 (Symbolic Layout)



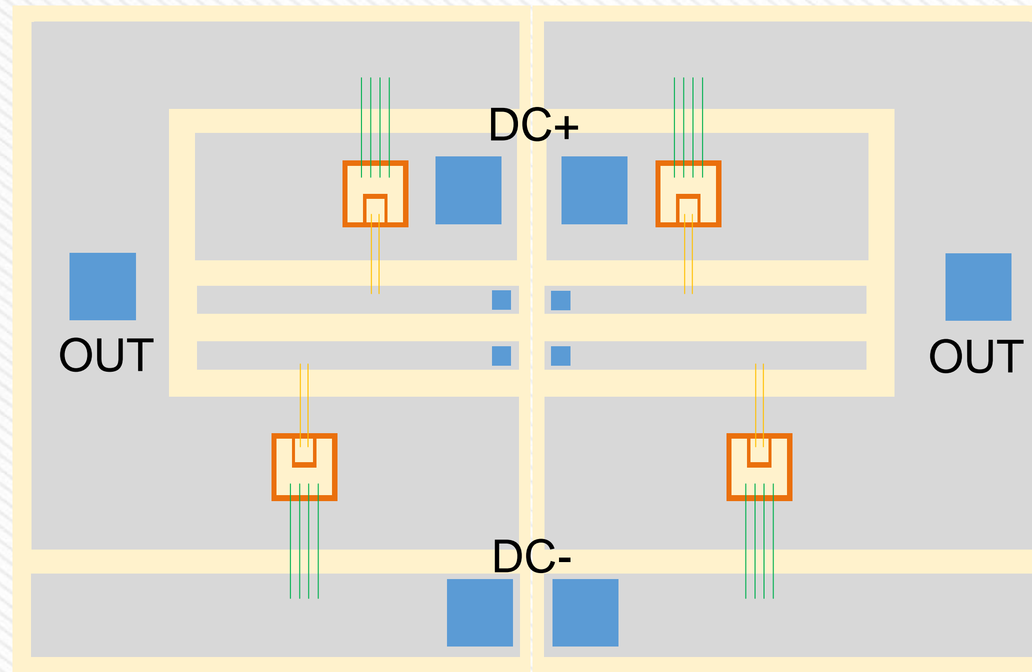
- Lines: Wire bond/ Trace
- Points: Lead
- Cannot represent multiple non-collinear components

PS v1.3 (Flat-Level Text Script)



- No wire bonds
- All components are on same plane
- Not very realistic
- Only Manhattan designs

PS v1.9/2.0 (Hierarchical Text Script)



- Wire bonds (v1.9, v2.0), Vias (v2.0)
- Hierarchical placement
- All 2D/2.5D/3D layout representation
- Only Manhattan designs

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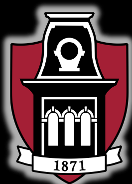
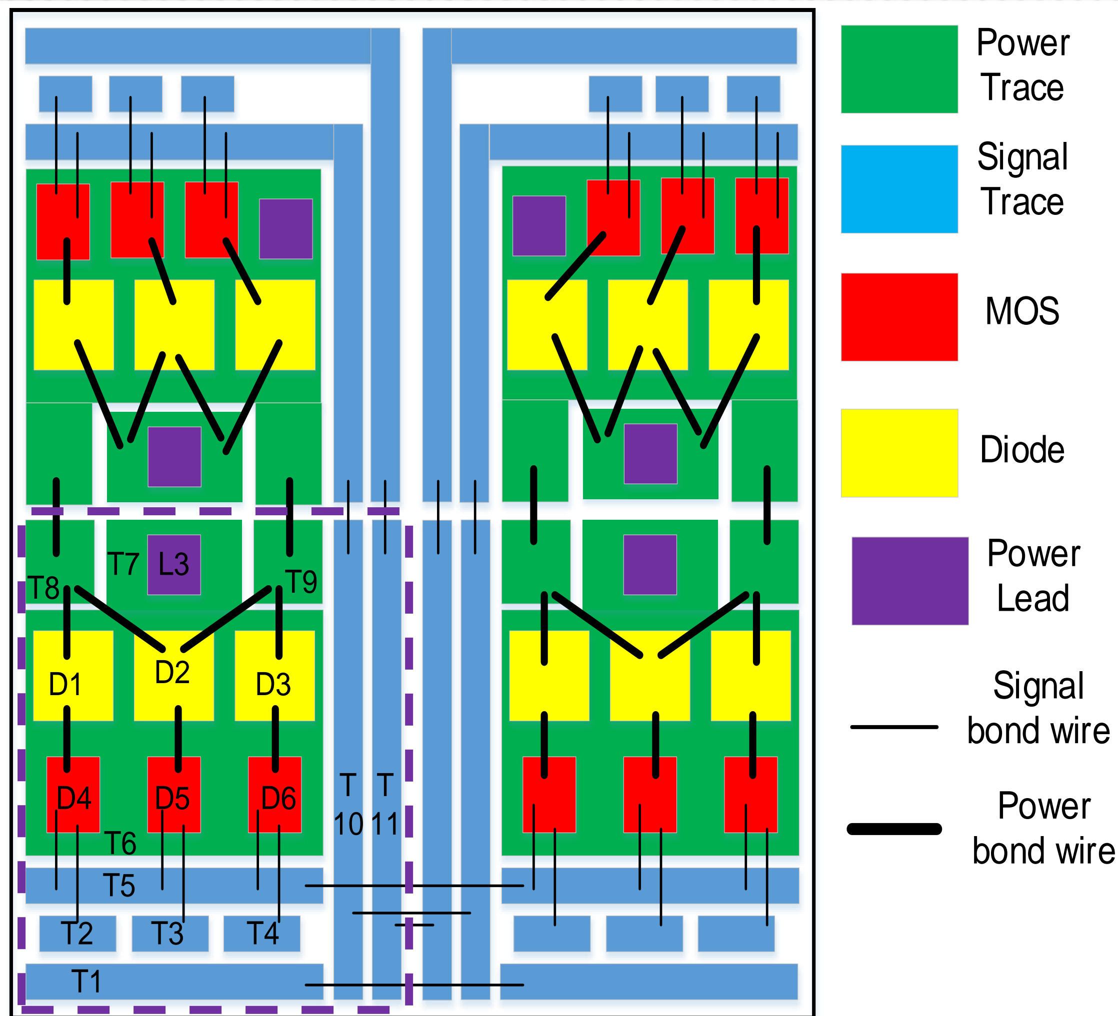


Flat-Level Vs. Hierarchical Text Script

- 2D rectilinear tile representation



Initial layout of a commercial module

Flat-level

```
+ T1 signal 2 2 26 2
+ T2 signal 4 6 6 2
+ T3 signal 12 6 6 2
+ T4 signal 20 6 6 2
+ T5 signal 2 10 26 2
+ T6 power 2 14 26 20
- T7 power 11 34 8 6
+ D1 Diode 3 26
+ D2 Diode 12 26
+ D3 Diode 21 26
+ D4 MOS 4 16
+ D5 MOS 13 16
+ D6 MOS 22 16
+ L3 power_lead 13 35
+ T8 power 2 35 7 5
+ T9 power 21 35 7 5
+ T10 signal 30 2 2 38
+ T11 signal 34 2 2 38
```

Hierarchical

```
+ T1 signal 2 2 26 2
+ T2 signal 4 6 6 2
+ T3 signal 12 6 6 2
+ T4 signal 20 6 6 2
+ T5 signal 2 10 26 2
+ T6 power 2 14 26 20
- T7 power 11 34 8 6
    + D1 Diode 3 26
    + D2 Diode 12 26
    + D3 Diode 21 26
    + D4 MOS 4 16
    + D5 MOS 13 16
    + D6 MOS 22 16
    + L3 power_lead 13 35
+ T8 power 2 35 7 5
+ T9 power 21 35 7 5
+ T10 signal 30 2 2 38
+ T11 signal 34 2 2 38
```

Layout geometry script

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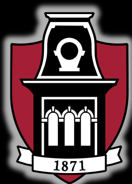

PowerSynth 2 User Interfaces

- **Command Line Interface (CLI)**
  - Linux compatibility
  - User input through terminal
  - Modes: Script-based or Step-by-step
- **Graphical User Interface (GUI)**
  - Two flows:
    - Creating new project
    - Run existing project through 'Macro script'
  - MDK editor
  - Optimization setup
  - Performance evaluation model setup
  - Interactive solution browser

Main Window | Layout Optimization | Thermal Model | Electrical Model | Solution Browser

PowerSynth v2.0 GUI

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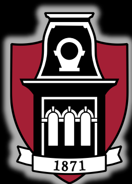

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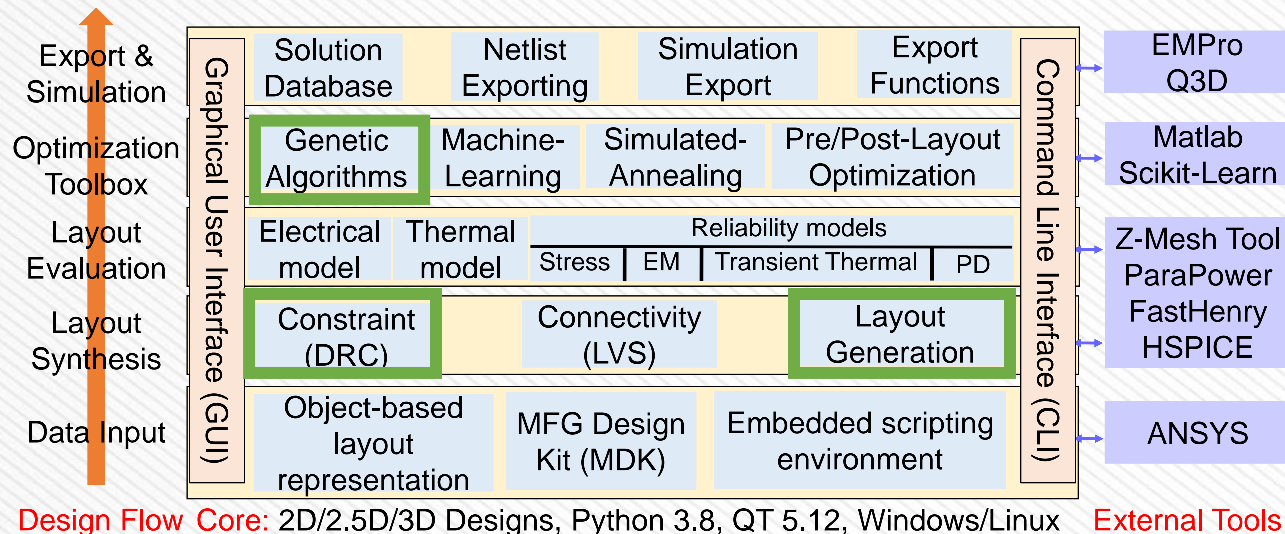
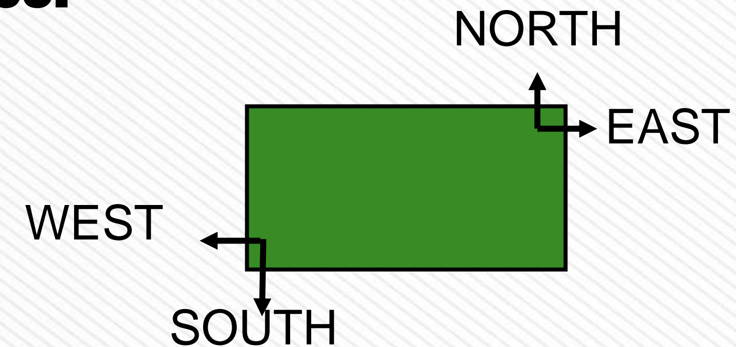
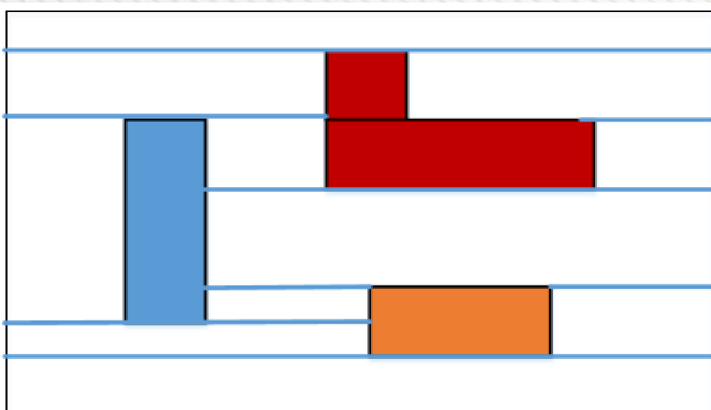


Corner Stitching

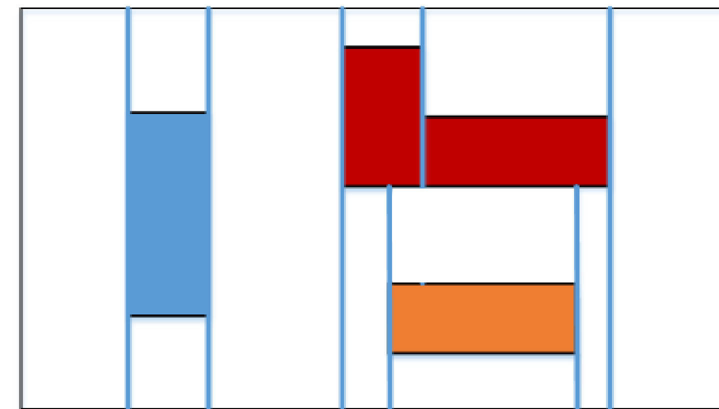
- **Layout area is tiled with non-overlapping rectangles:**
  - Empty tiles and different types of solid tiles
- **Each tile contains four pointers:**
  - Two at its top right corner, two at lower left
- **Rules for horizontal (vertical) corner stitch:**
  - Rule #1: First, each tile must be as wide (tall) as possible.
  - Rule #2: Then, each tile must be as tall (wide) as possible.





Horizontal corner stitch (HCS)

EMPTY → Not Filled
SOLID → Filled
Color → Type



Vertical corner stitch (VCS)

Ousterhout et. al., "Magic: a VLSI layout system", in Design Automation Conference. 152-159, 1984

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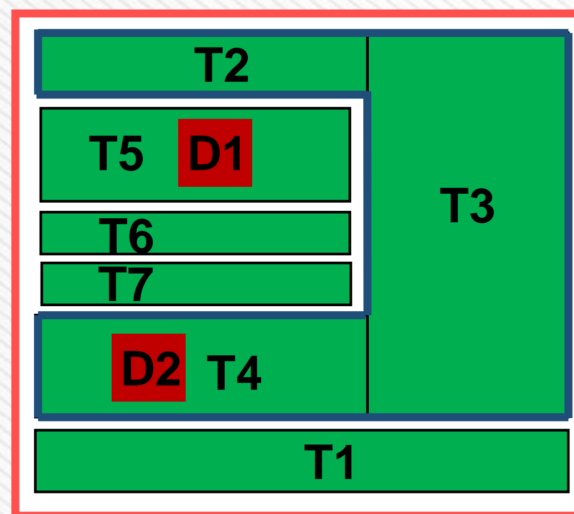
Hierarchical Corner Stitch

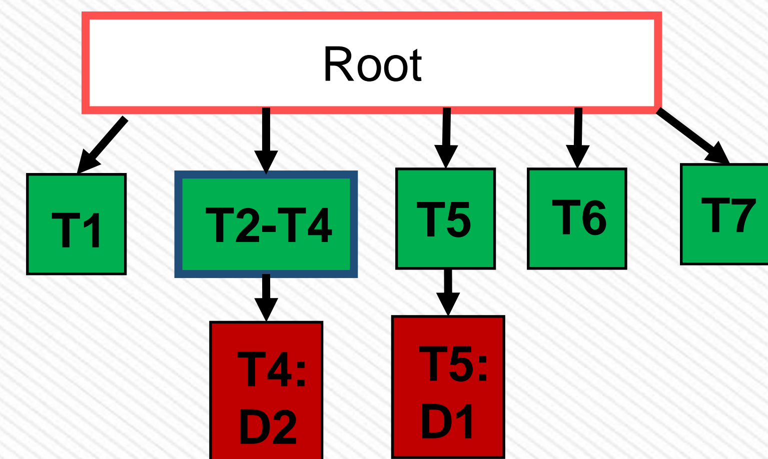
❑ **Tree structure is maintained to preserve component hierarchy**

- **Tree structure construction:**
  - The root is the initial empty tile (substrate rectangle).
  - All components are inserted in a group-wise manner.
  - Two types of tile in each node: parent (background tile) and children (foreground tile).
- **Two tree for each layout: HCS tree and VCS tree**

- **In the example:**
  - All traces are in the root.
  - T2,T3, and T4 are connected → Same group.
  - D1 is placed on T5, that makes D1 child and T5 parent.



2D power module Layout



Tree Structure

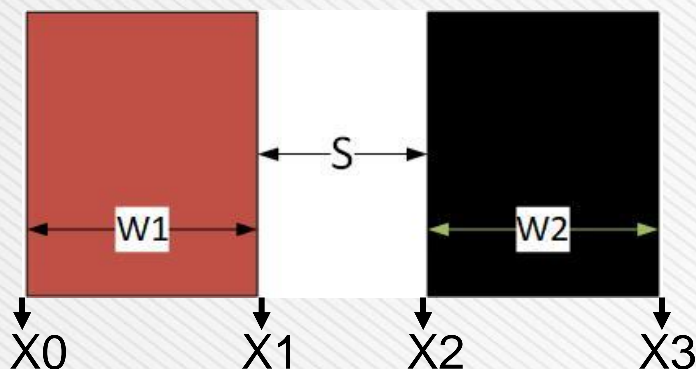
Imam Al Razi et. al., "Hierarchical Layout Synthesis and Design Automation for 2.5D Heterogeneous Multi-Chip Power Modules", in ECCE, pp. 2257–226, 2019.

Constraint Graph

- Computation technique for a set of inequalities
- Relationship between vertices with edges having minimum constraint value

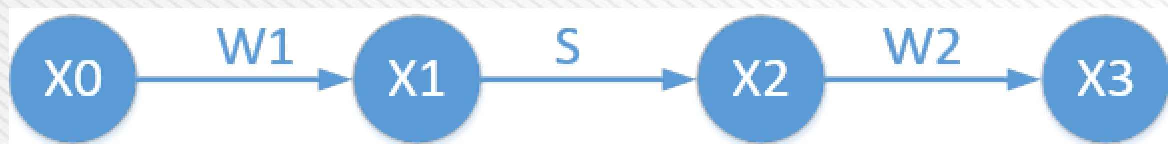
B>=A+W

- Two Types of Constraint Graphs:
  - Horizontal/Vertical constraint graph (HCG/VCG)



W1: Min width of block 1
W2: Min width of block 2
S: Min spacing between them

HCG:



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Constraints

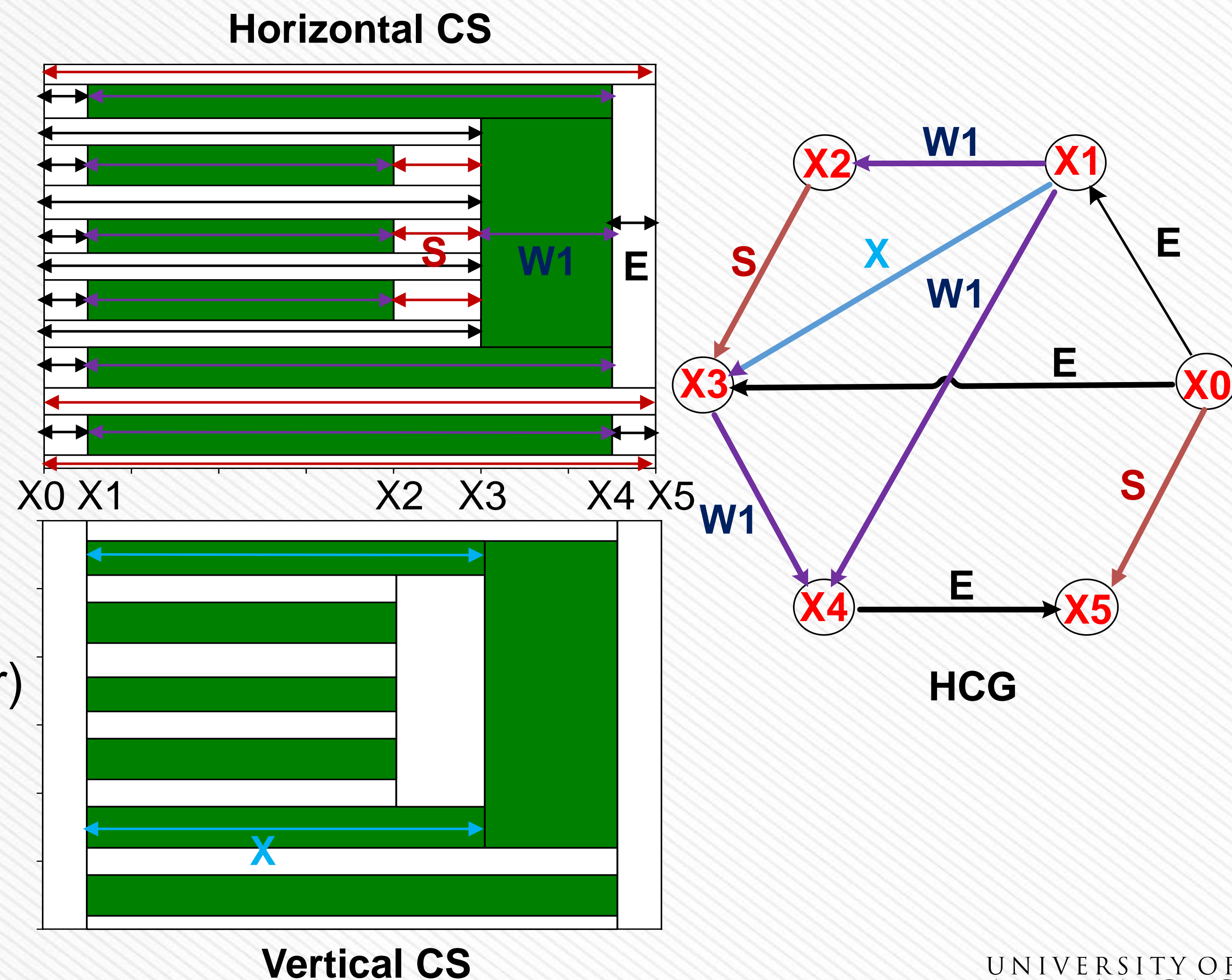
❑ Design Constraints:

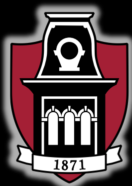
- **DRC-clean fabrication-feasible layouts:**
  - Minimum width (W)
  - Minimum spacing (S)
  - Minimum enclosure (E)
  - Minimum extension (X)

❑ Reliability Constraints:

- **Minimize thermal and electrical (i.e. partial discharge) concerns:**
  - Current-dependent minimum width (Wr)
  - Voltage-dependent minimum spacing (Sr)

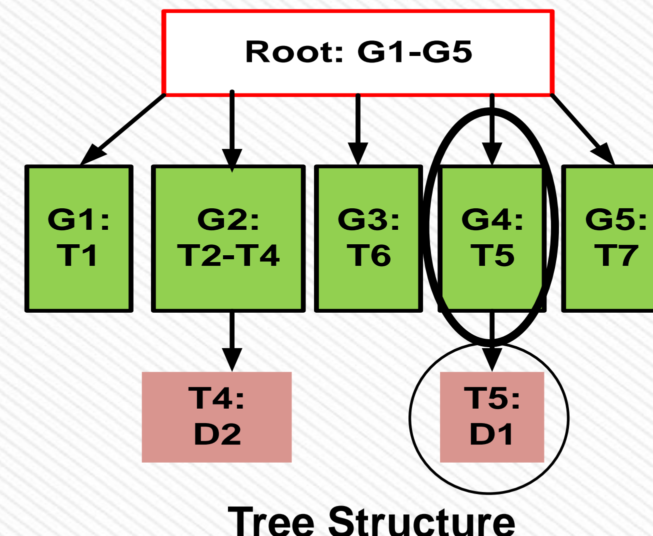
❑ Constraint Illustration

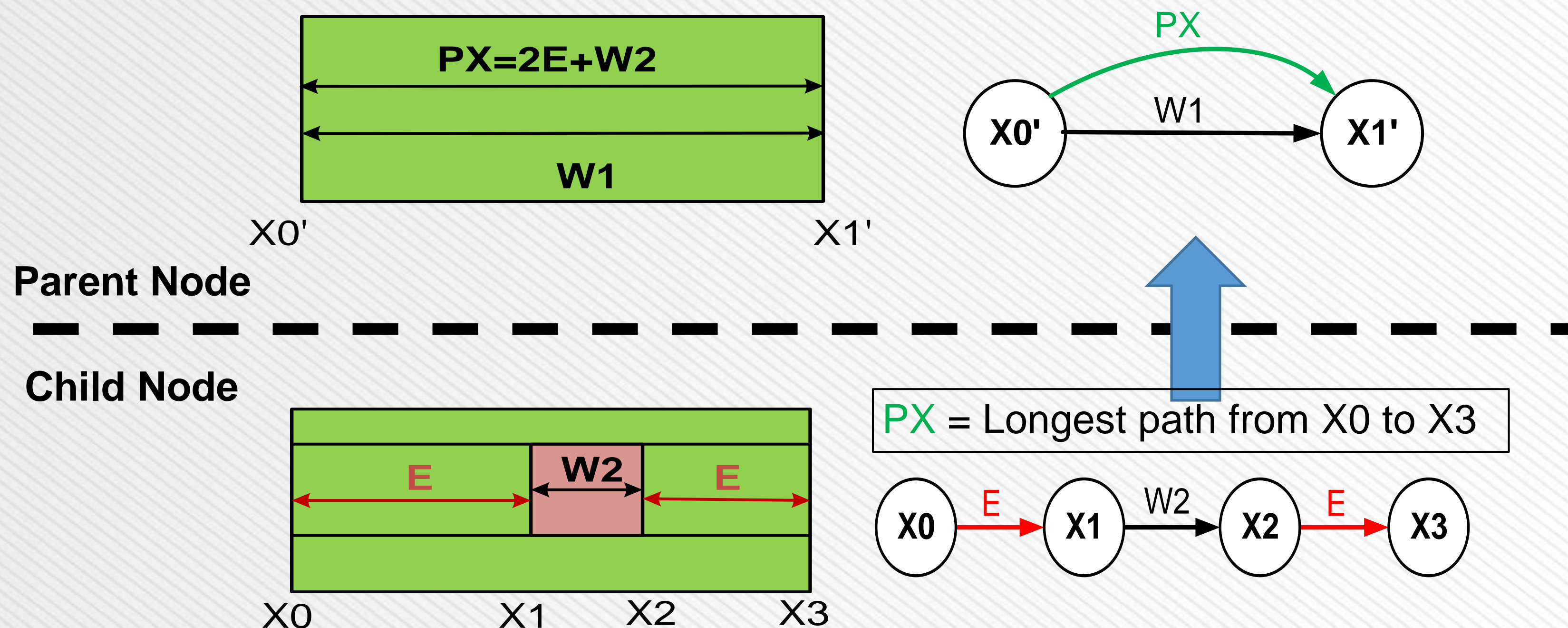




Hierarchical Constraint Graph

- **Each node in the tree → Constraint graph**
  - Mapping of the design constraints
- **Example**
  - From the tree, G4 (parent) and T5:D1 (child), hierarchical horizontal constraint graph is shown:

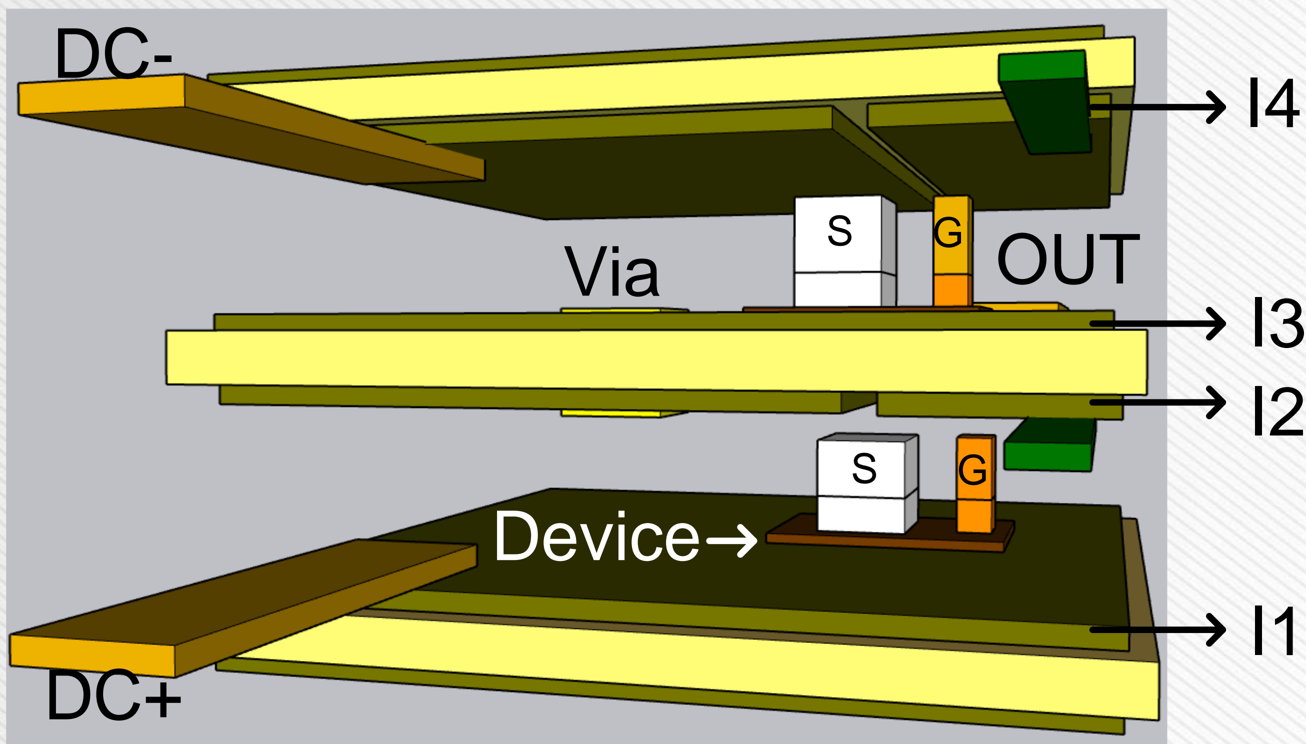




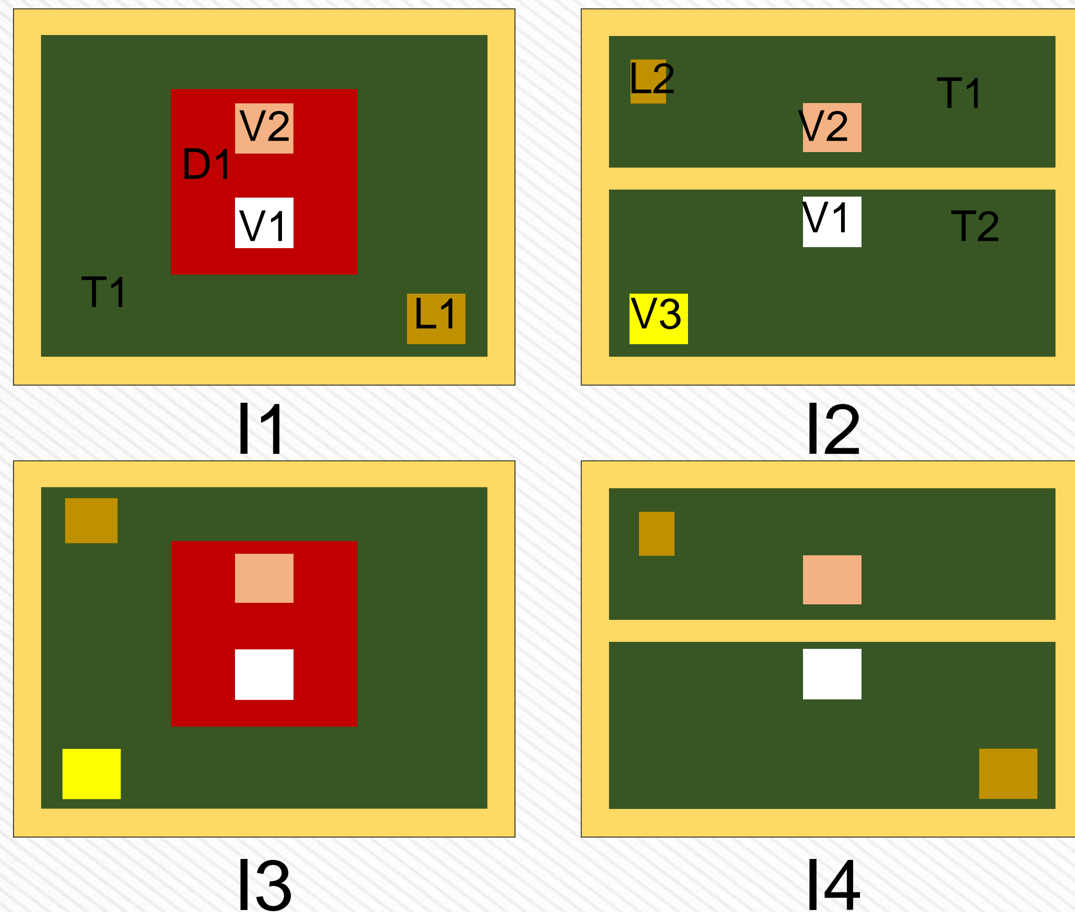
W2= min width of device (Child Node)
W1= min width of trace (Parent Node)

Imam Al Razi et. al., "Hierarchical Layout Synthesis and Design Automation for 2.5D Heterogeneous Multi-Chip Power Modules", in ECCE, pp. 2257–226, 2019.

Input 3D Layout



3D wire bondless half-bridge module



2D layout of each layer

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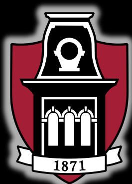
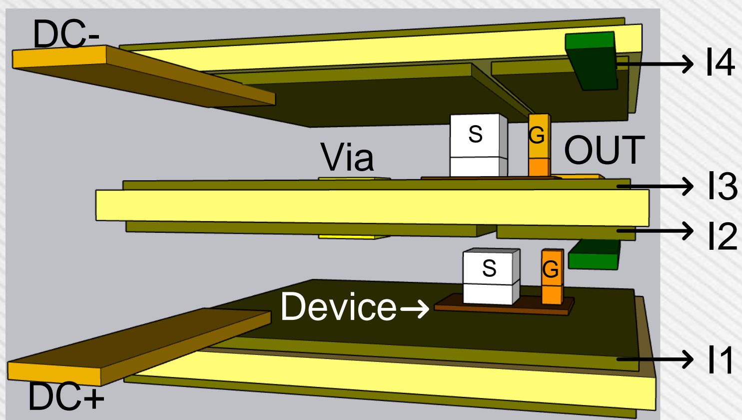
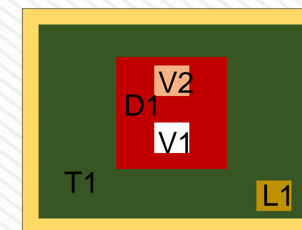
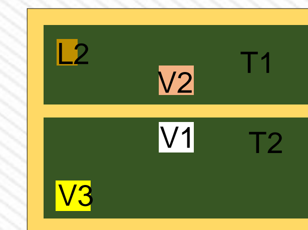


Input Layout Hierarchy

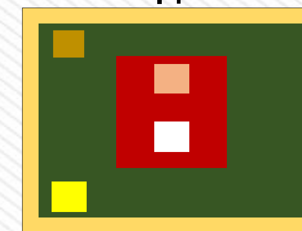




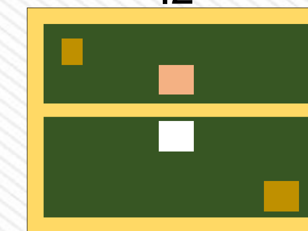
I1



I2



I3



I4

Root

Sub-Root

Abstract

Interfacing layer 1

Interfacing layer 2

I1 Substrate
I2 Substrate
I3 Substrate
I4 Substrate

T1
T1
T2
T1
T1
T2

D1
L1
V1
V3
V2
L2
D2
V3
L3
V4
L4
V5
L5

V1
V2
V4
V5

Physical

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Hierarchy Tree Creation

Substrate (B) + Trace (F)

Trace (B) + Device (F)

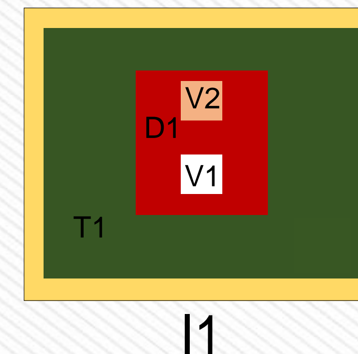
Device (B) + Via (F)

Interfacing Layer

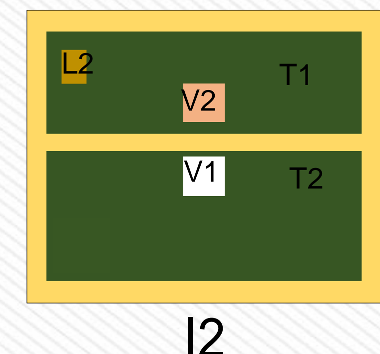
Substrate (B) + Trace (F)

Trace (B) + Via (F)

- **Interfacing layer (Sub-root)**
  - Derived layer from it's child nodes
  - No physical existence
  - Only created in the constraint graph
  - Maintains constraints among shared components of child nodes



I1



I2

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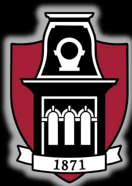


Layout Generation

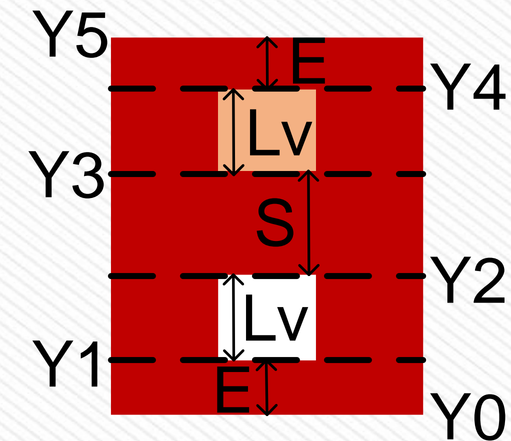
❑ High-level steps:

```
1    Read Input Script
2    Create a root node
3    Create group of layers connected with same via

4    For each via connected group
5      Create a sub-root (interfacing layer)
6      For each layer
7          Create HCS, VCS
8          Create and Evaluate HCG, VCG
9    For each ancestor from leaf to root
10     Perform bottom-up constraint propagation

11   Evaluate root node and compute available space

12   For each sub-tree from root to leaf
13     Perform top-down location propagation

14   Evaluate independent nodes
```

Imam Al Razi et. al., “Physical Design Automation for High-Density 3D Power Module Layout Synthesis and Optimization”, ECCE, pp. 1984–1991, 2020

Constraints Handling

- **Two types of edges:**
  - Rigid edge: Having fixed (constant) weight (•·····•)
  - Flexible edge: weight can be varied (⟶)
- **Two types of vertices:**
  - Independent: locations are randomized independently. (● blue)
  - Dependent: all incoming or outgoing edges are rigid edges. (● black)



HCS: Device with Vias

Initial VCG

Modified VCG

E: Min enclosure   Lv: Min via length   S: Min spacing

Imam Al Razi et. al., "Hierarchical Layout Synthesis and Optimization Framework for High-Density Power Module Design Automation", ICCAD, pp. 1-8, 2021

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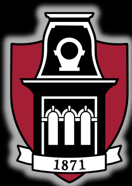
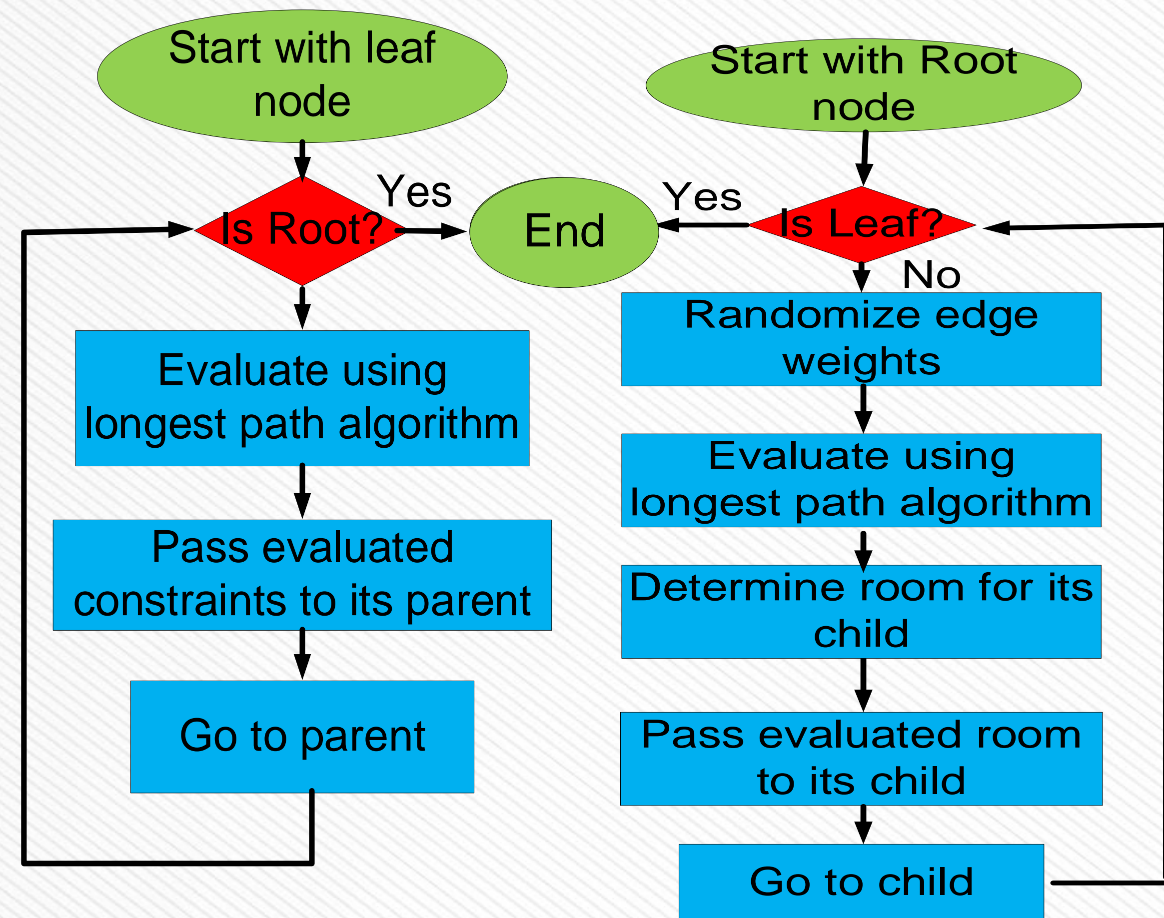


Constraint Propagation and Evaluation

- **Each constraint graph is evaluated using longest path algorithm.**
- **The evaluated constraints are propagated in a bidirectional manner.**
  - **Bottom-up constraint propagation**
    - Propagates from leaf towards root
    - Evaluated minimum constraints
    - Ensures room for child component
  - **Top-down location propagation**
    - Starts on arrival of all minimum constraint values in the root
    - Root node evaluation can generate three types of solutions:
      - Minimum-sized
      - Variable-sized
      - Fixed-sized
    - Propagates from root towards child
    - Shared vertices locations are propagated



Imam Al Razi et. al., "Hierarchical Layout Synthesis and Optimization Framework for High-Density Power Module Design Automation", ICCAD, pp. 1-8, 2021

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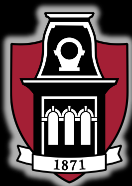
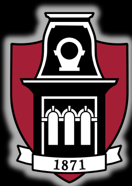


Genetic Algorithm Workflow

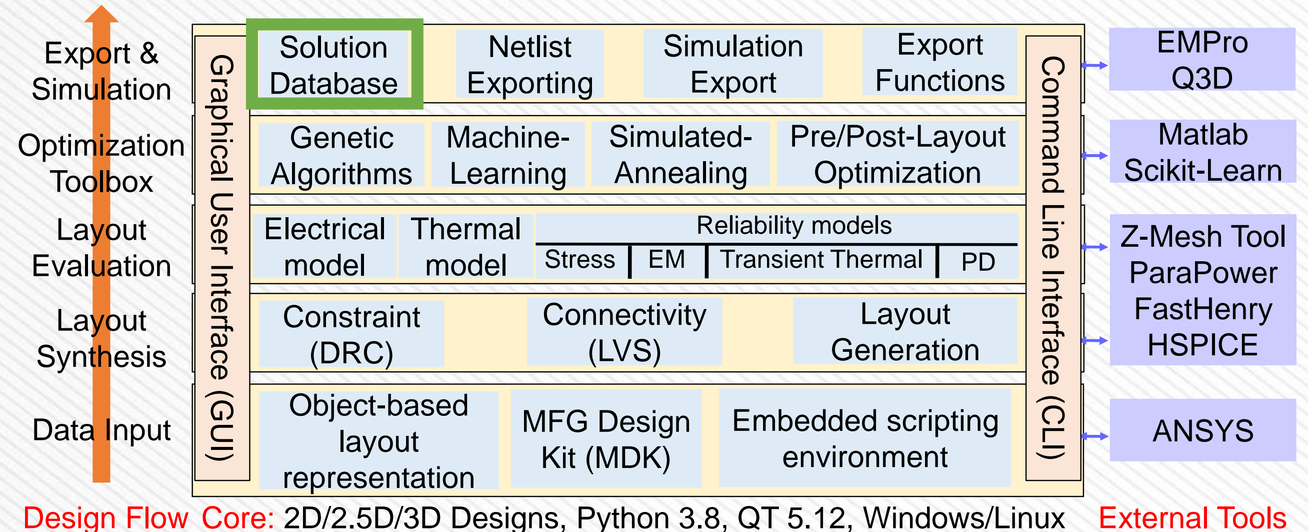
- **Non-dominated Sorting Genetic Algorithm II (NSGAII)**
  - **Customized flow for 2D/2.5D/3D MCPM layout optimization**

Imam Al Razi et. al., “Hierarchical Layout Synthesis and Optimization Framework for High-Density Power Module Design Automation”, ICCAD, pp. 1-8, 2021



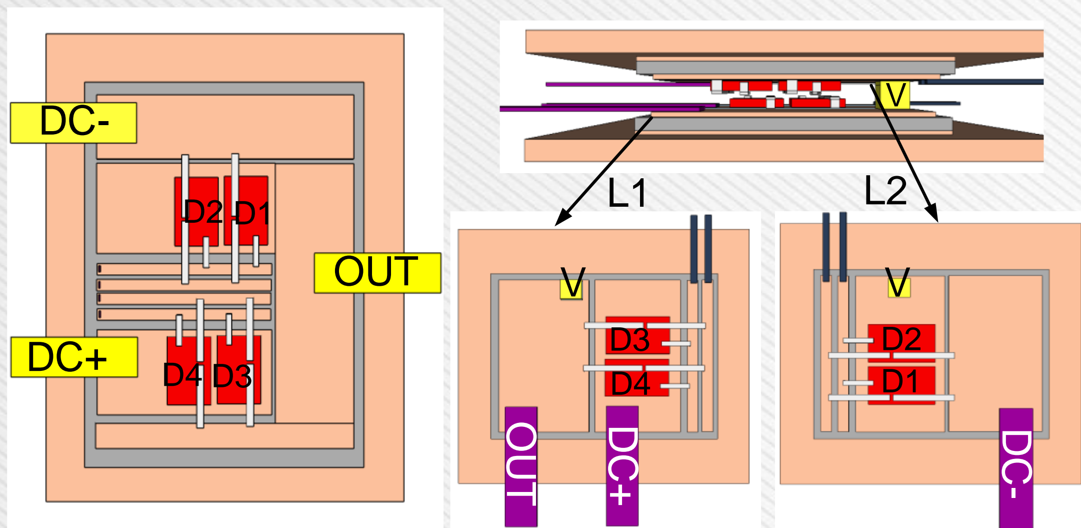
Outline

- ❑ Introduction
- ❑ Motivations & Contributions
- ❑ **Constraint-Aware Layout Engine**
  - Layout Representation
  - Methodology
  - **Results**
    - **Minimum-Sized Results**
    - 3D MCPM Layout Optimization & Hardware Validation
- ❑ Reliability Optimization
  - Thermal Cycling Impact Minimization
  - Electromigration (EM) Impact Minimization
- ❑ Conclusion & Future Work



2D vs. 3D Layout

❑ Initial Layout

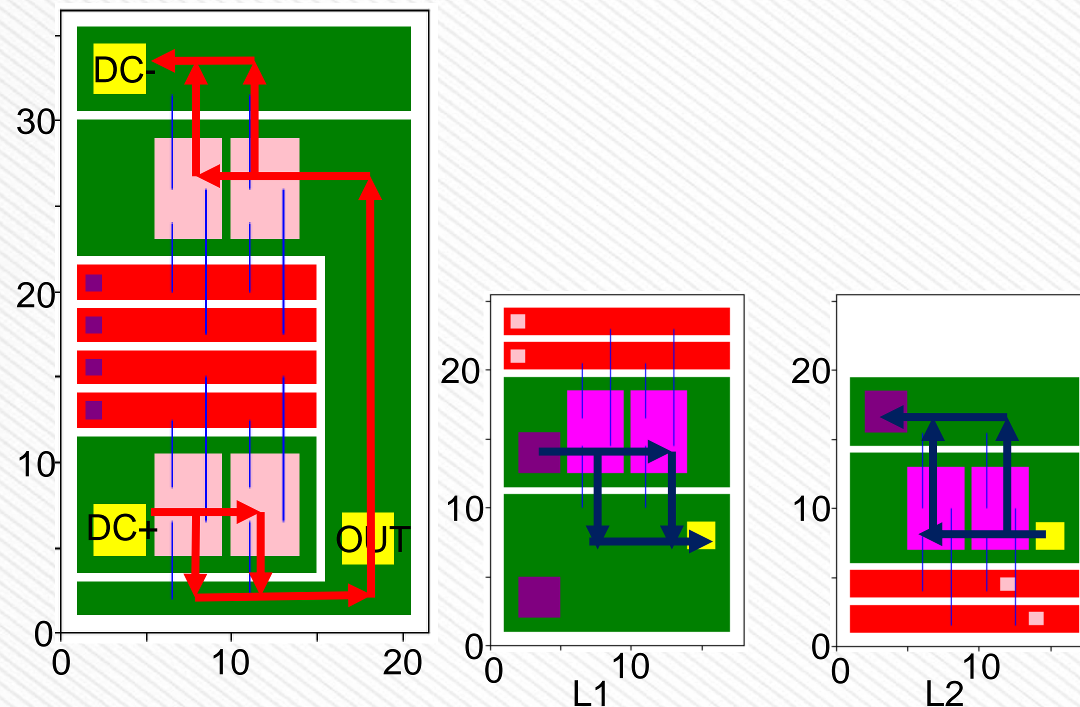


Half-bridge MCPM: 2D structure (left), 3D structure (right)

Performance comparison

Metric	2D	3D
Loop Inductance	15.93 nH	6.104 nH
Max Temperature	332.15 K	370.29 K (single-side cooling)
		328.38 K (dual-side cooling)

- **Min-Sized layout:**

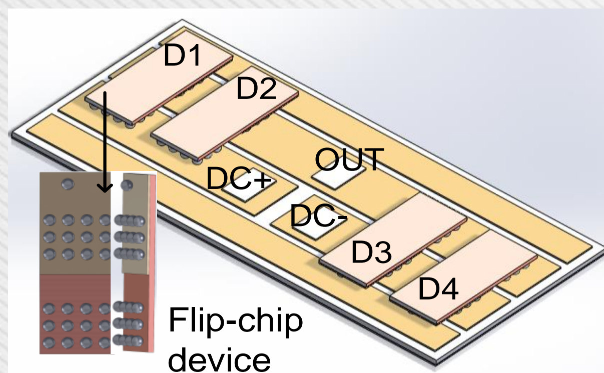


Imam Al Razi et.al, "Physical Design Automation for High-Density 3D Power Module Layout Synthesis and Optimization", in ECCE , pp. 1984–1991, Oct 2020

High-Density SOTA Packaging Layouts

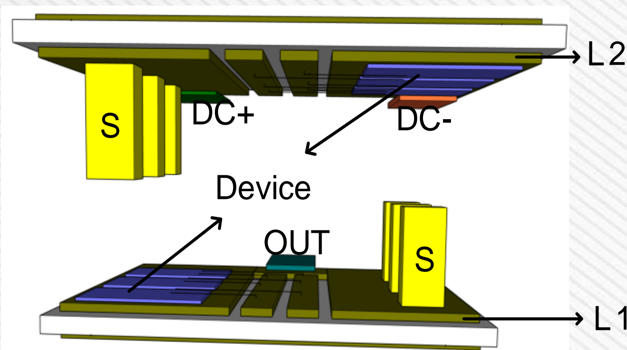
❑ Layout Types:

- 2D/2.5D/3D wire bonded, wire bondless, hybrid, Flip-chip
- Generic algorithm to generate all types of solutions



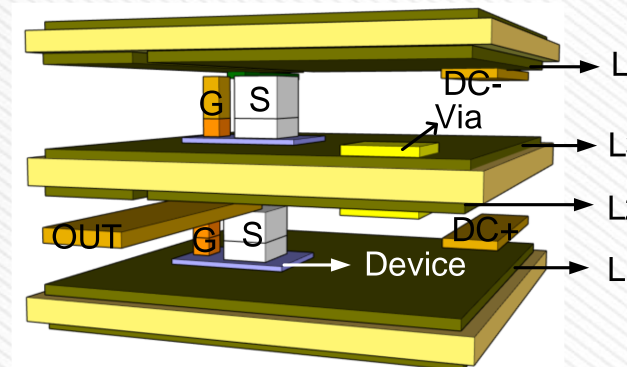
2D Flip-chip Half-bridge

- One device layer
- Solder ball array
- Extended drain connector
- Planar power loop
- Double-sided cooling



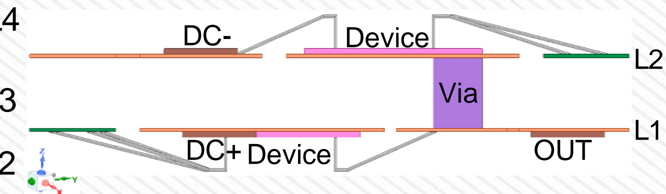
3D Hybrid Half-bridge

- Two device layers
- Wire bond (gate loop)
- Metallic post (power loop)
- Hybrid power loop
- Double-sided cooling



3D Wire-bondless Half-bridge

- Two device layers
- Metallic post (power & gate loop)
- Vertical power loop
- Double-sided cooling

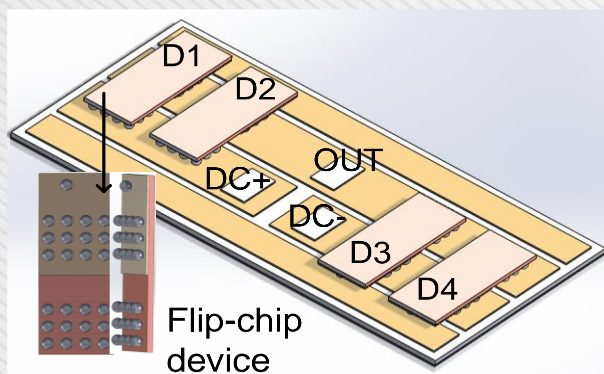


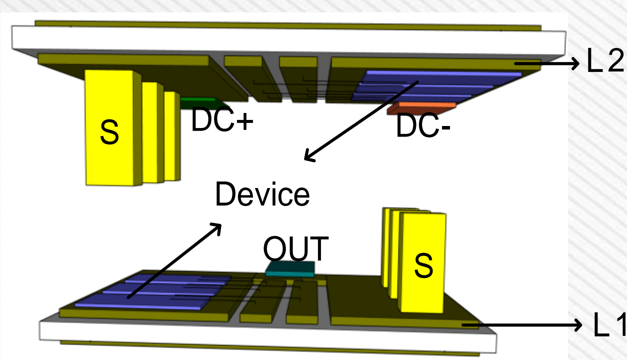
3D Wire-bonded Half-bridge

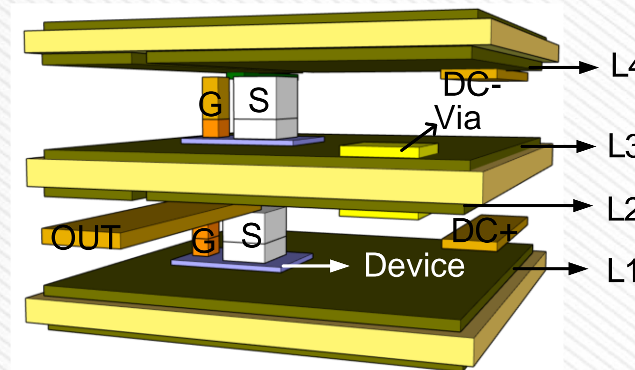
- Two device layers
- Wire-bond (power & gate loop)
- Vertical power loop
- Embedded cooling

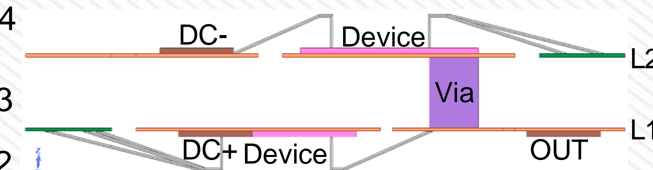
❑ Minimum-sized Solutions

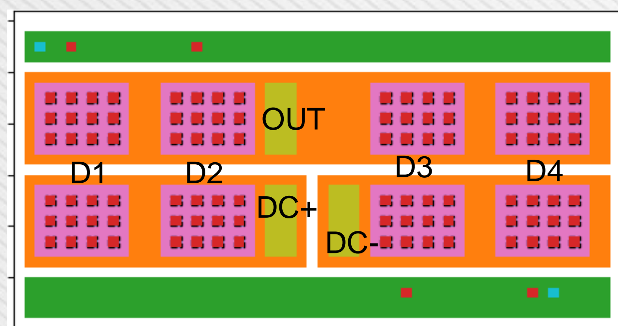
- Demonstrates the layout handling capability
- Maximum power-density of each type
- Further optimization required
- Fabrication complexity is key for prototyping





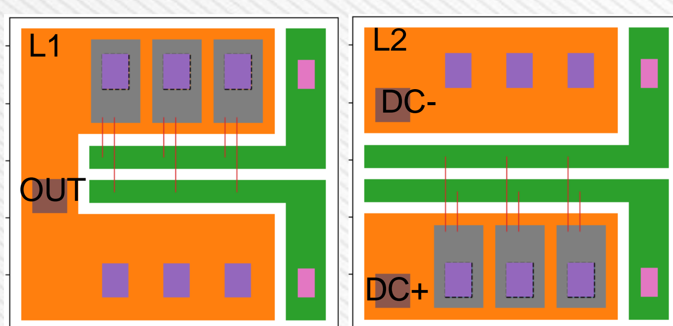






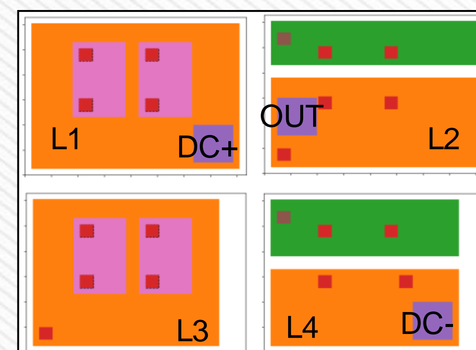
(58 mm × 31 mm)

Flip-Chip Module



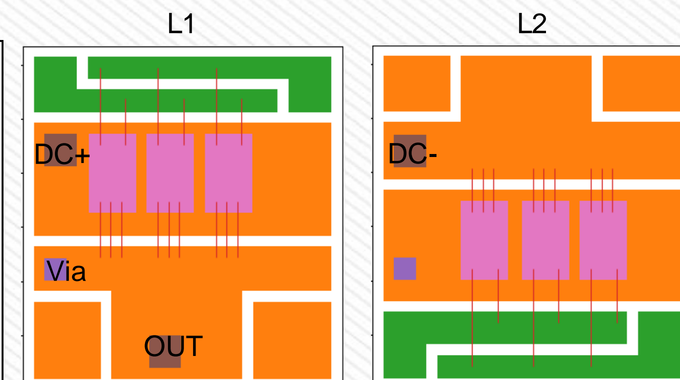
(28.68 mm × 27.52 mm)

Hybrid Module



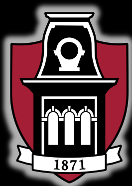
(16.7 mm × 12.6 mm)

Wire-bondless Module



(29.54 mm × 31.72 mm)

Wire-bonded Module



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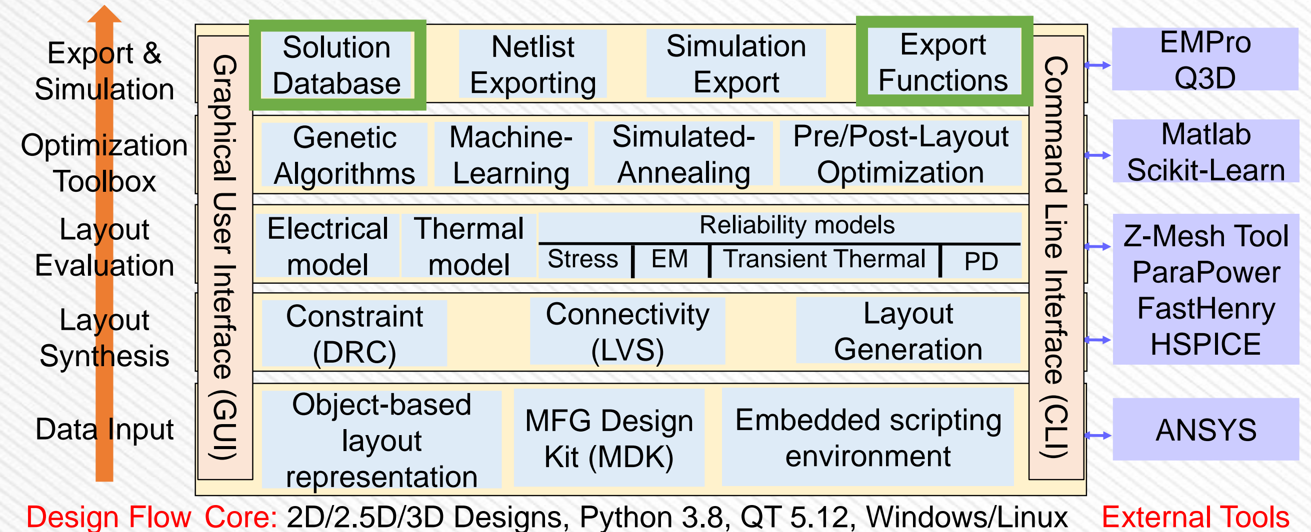

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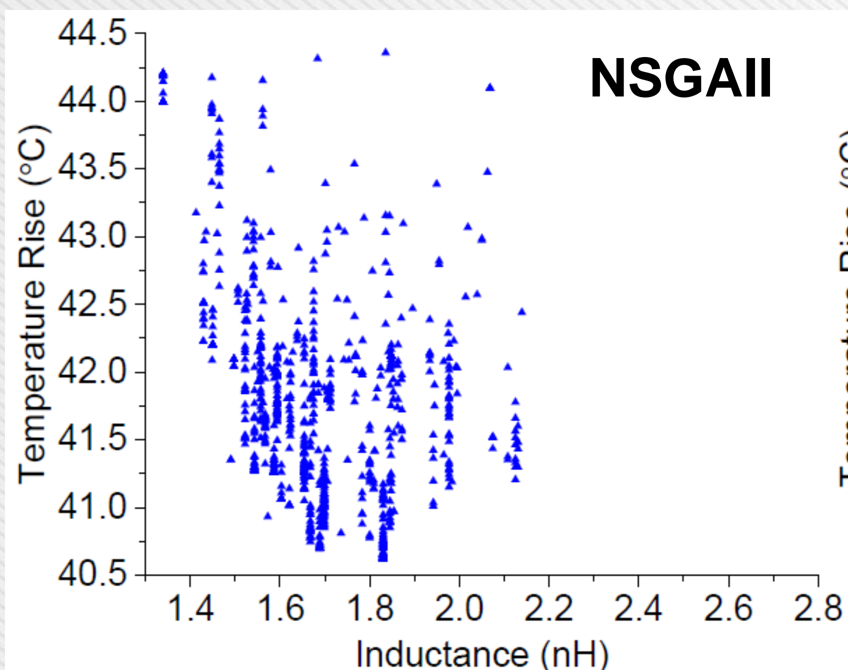
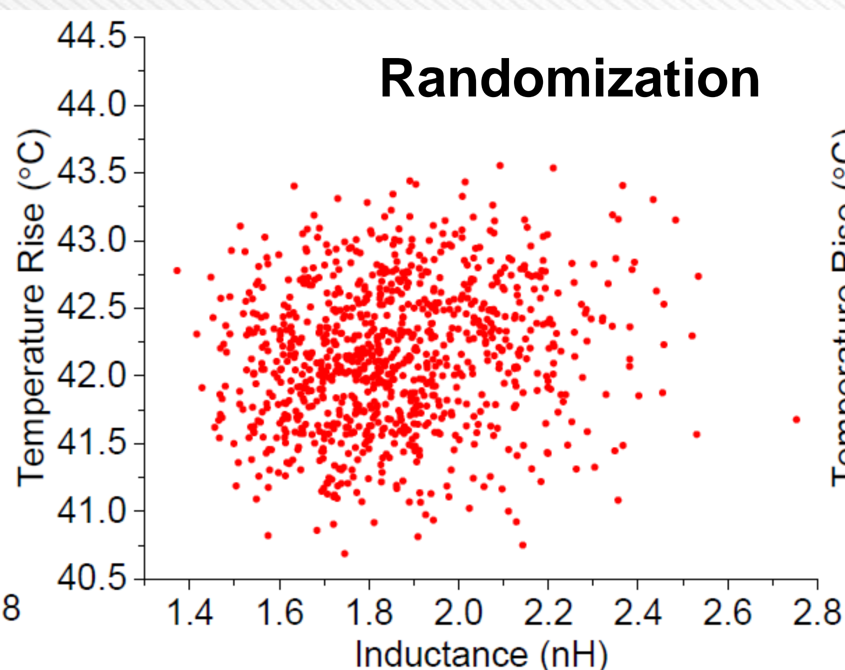
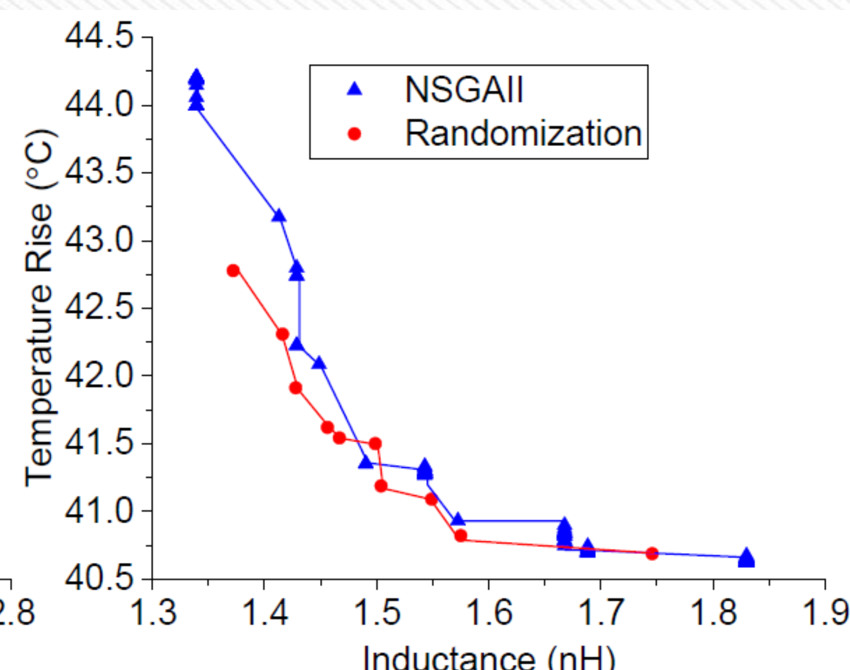
NSGAII vs. Randomization

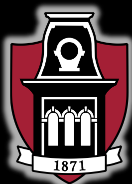
- Comparison for wire-bond less 3D module

Algorithm	Total Layouts	Approximate runtime(min)		On Pareto-front
		Generation	Evaluation	
NSGAII	937	25	206	148
Randomization	937	1	212	10





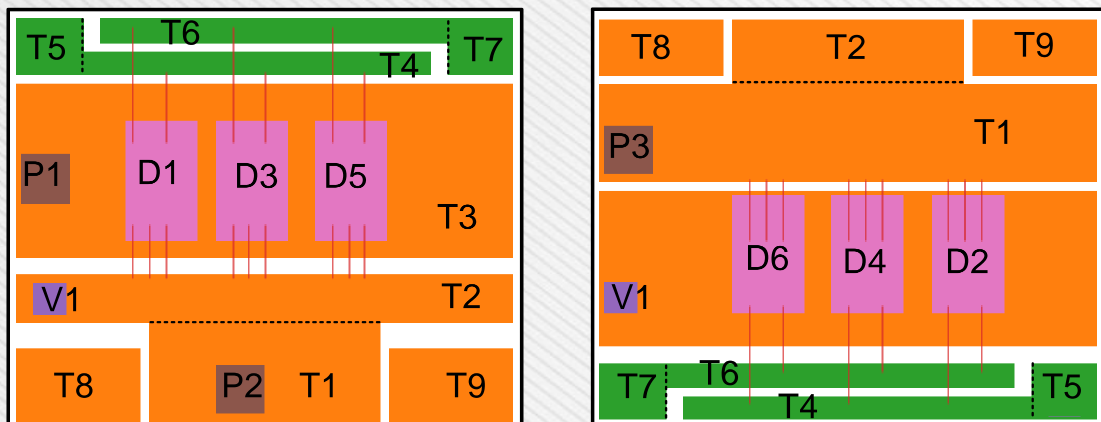




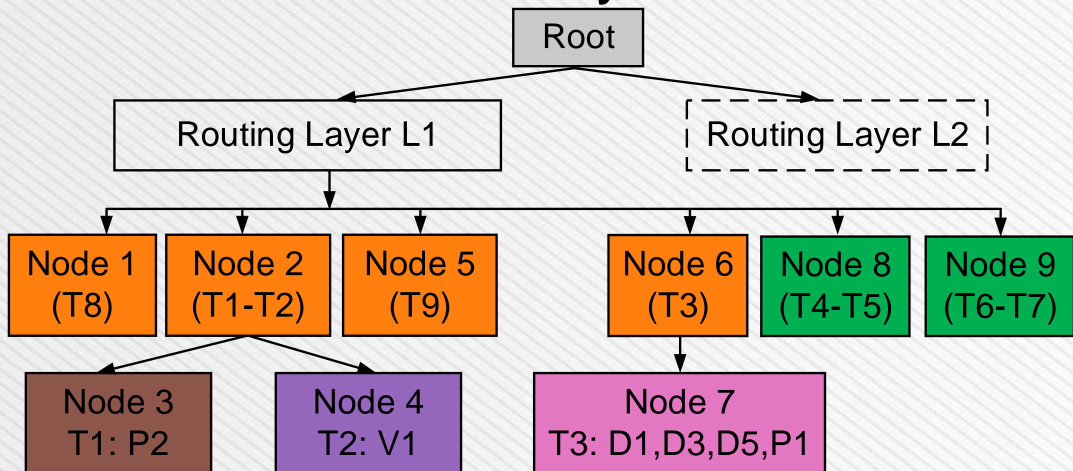
3D MCPM Layout Optimization

❑ 3D Wire-Bonded half-bridge MCPM layout

Signal Trace　Power Trace　Device



L1　**Initial layout**　L2



Hierarchical tree

```
# Via Connectivity Information
L1 L2: V1  Through

# Layout Geometry
L1 Z-
+ T8 power 7 7 7.5 4.5
+ T9 power 29.5 7 7.5 4.5
+ T1 power 15 7 14 6
- T2 power 7 13 30 3
    + B11 power 14 15.75
    + B28 power 20 15.75
    + B36 power 26 15.75
    + P2 power_lead 19 7.5
    + V1 Via 8 13.5
+ T4 signal 11 28 21 1.5
- T5 signal 7 28 4 3.5
    + B7 signal 16 28.25
    + B27 signal 22 28.25
    + B40 signal 28 28.25
+ T6 signal 12 30 21 1.5
- T7 signal 33 28 4 3.5
    + B8 signal 14 31
    + B29 signal 20 31
    + B41 signal 26 31
+ T3 power 7 17 30 10.5
    + P1 power_lead 7.5 21
    + D1 MOS 13.5 18
        + B1 signal 16 24
        + B2 power 14 19
        + B3 power 14 24
    + D3 MOS 19 18
        + B24 signal 22 24
        + B25 power 20 19
        + B26 power 20 24
    + D5 MOS 25 18
        + B37 signal 28 24
        + B38 power 26 24
        + B39 power 26 19
```

Developer mode

```
# Via Connectivity Information
L1 L2: V1 Through

# Layout Geometry
L1 Z-
+ T8 power 7 7 7.5 4.5
+ T9 power 29.5 7 7.5 4.5
+ T1 power 15 7 14 6
- T2 power 7 13 30 3 BW3 BW6 BW9
    + P2 power_lead 19 7.5
    + V1 Via 8 13.5
+ T4 signal 11 28 21 1.5 BW1 BW4 BW7
- T5 signal 7 28 4 3.5
+ T6 signal 12 30 21 1.5 BW2 BW5 BW8
- T7 signal 33 28 4 3.5
+ T3 power 7 17 30 10.5
    + P1 power_lead 7.5 21
    + D1 MOS 13.5 18 BW1 BW2 BW3
    + D3 MOS 19 18 BW4 BW5 BW6
    + D5 MOS 25 18 BW7 BW8 BW9
```

User mode

Input geometry script for L1

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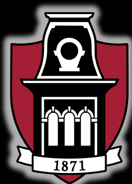


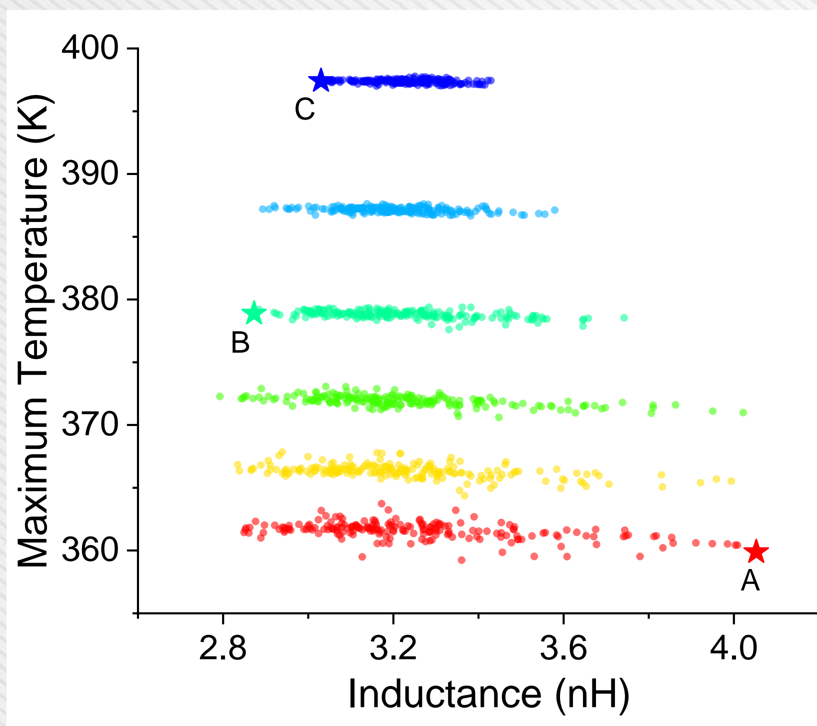
3D Layout Optimization Results

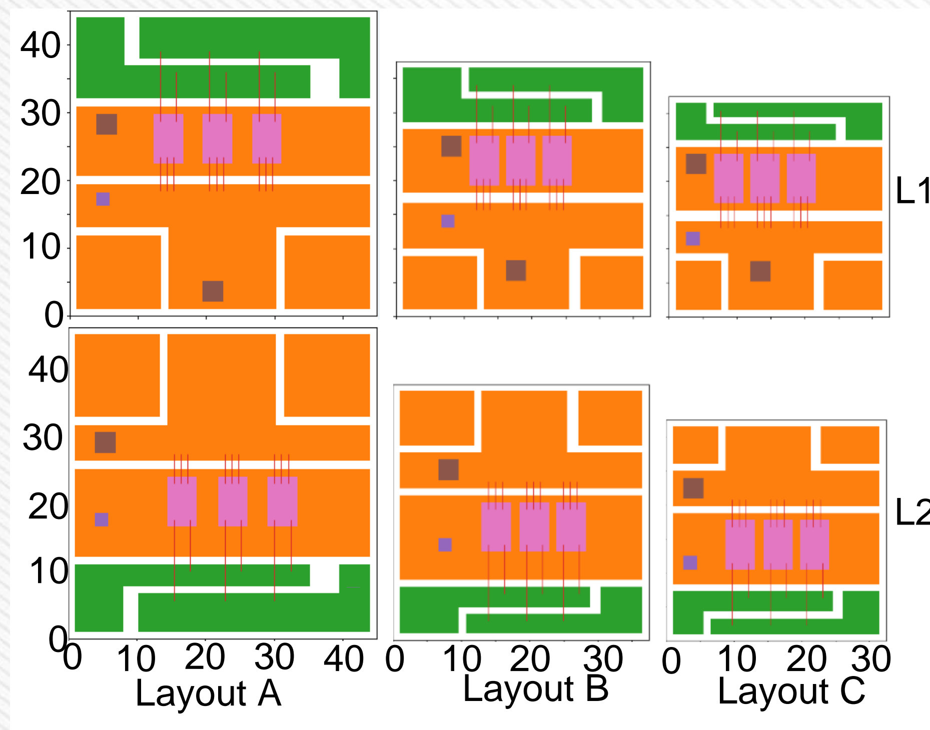
3D Wire-Bonded Layout Case

- Electro-thermal optimization
  - Six floorplan sizes
  - 1200 solutions
  - 2600 s runtime

Performance Values

ID	L (nH)	Max T (K)	Size (mm^2)
A	4.05	359.87	45 × 45
B	2.87	378.88	37.5 × 37.5
C	2.54	397.41	32.5 × 32.5





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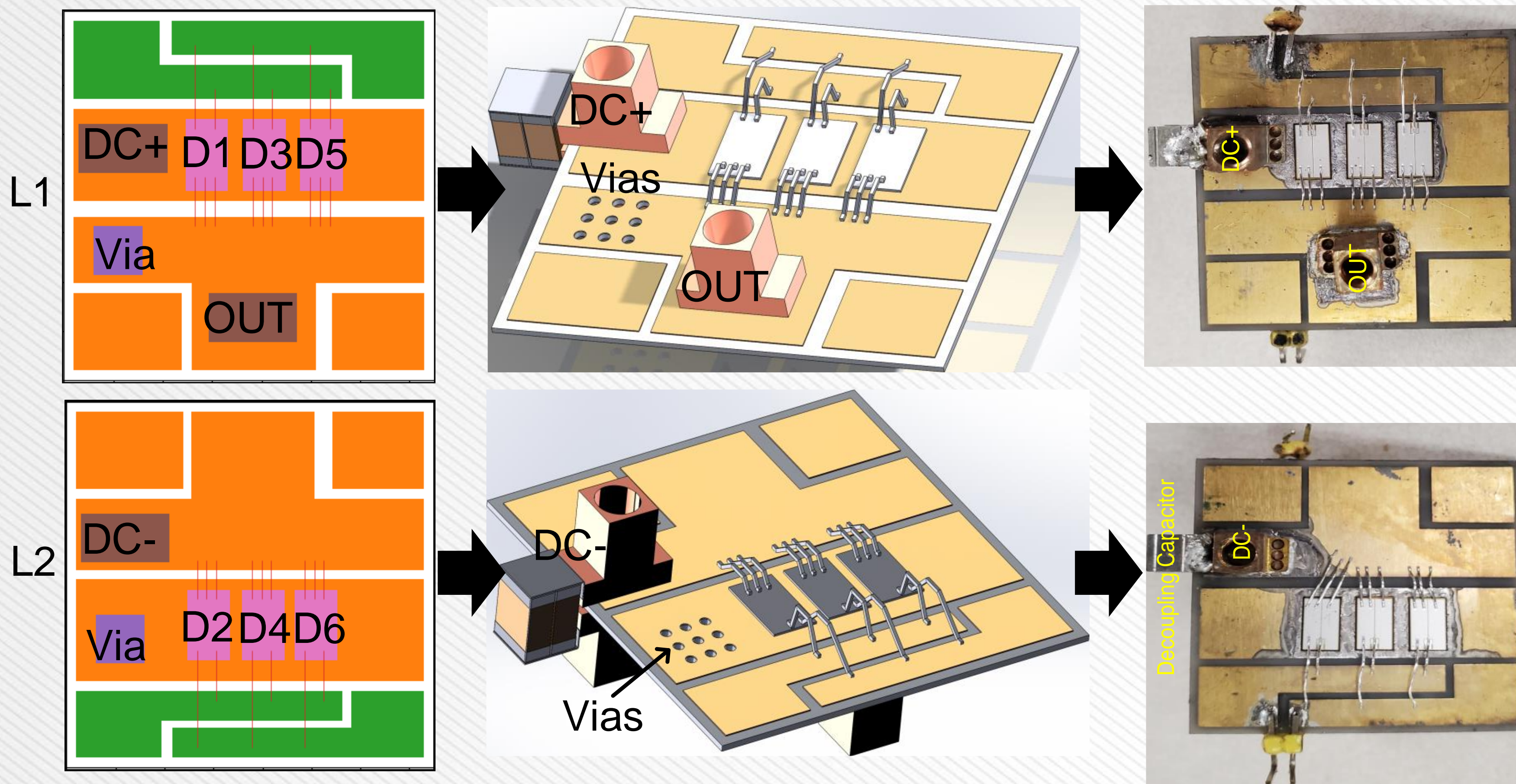
Layout Finishing & Fabrication

❑ Post-Layout Optimization

- Solution layout B has been tuned for gate loop optimization
- Modified solution is exported to SoliDWorks and taped out for fabrication



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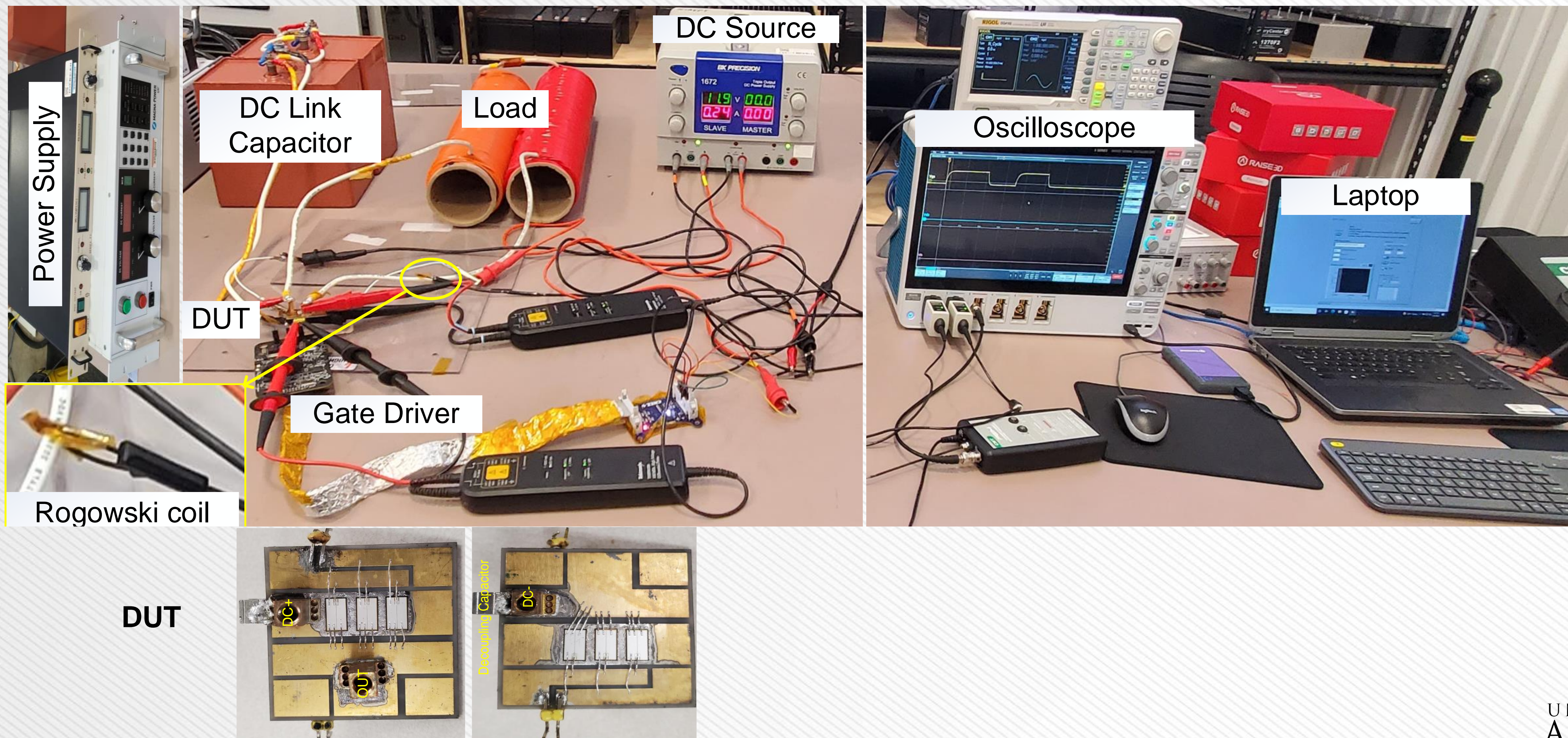
Module Functionality Validation (1/2)

❑ Double Pulse Test (Experimental Setup)



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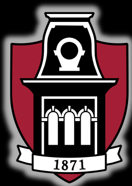
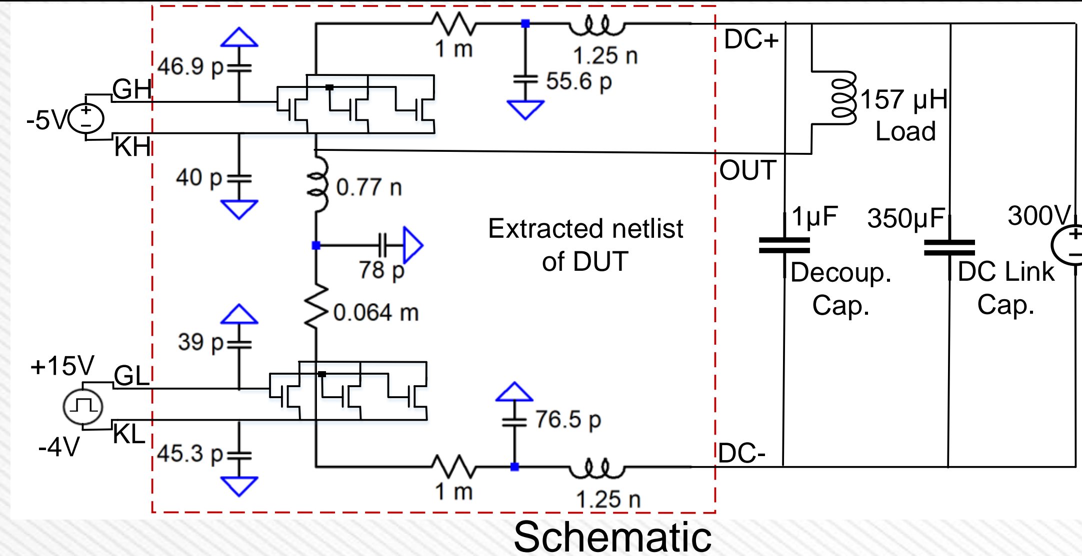
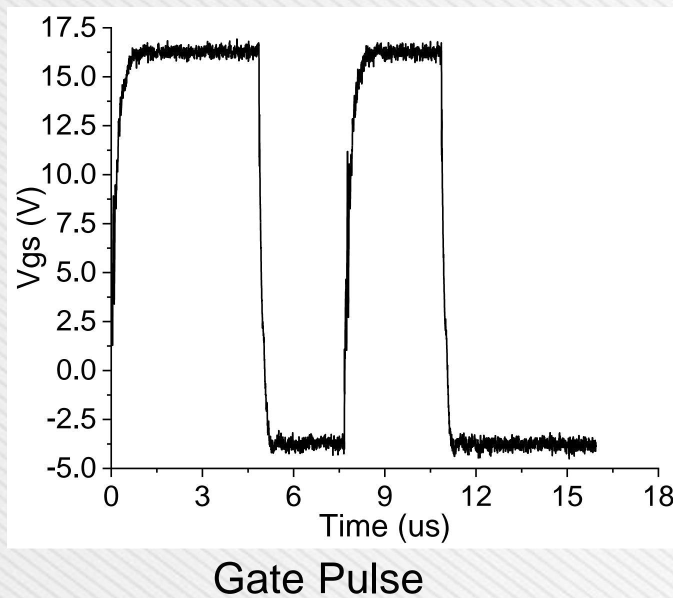


Module Functionality Validation (2/2)

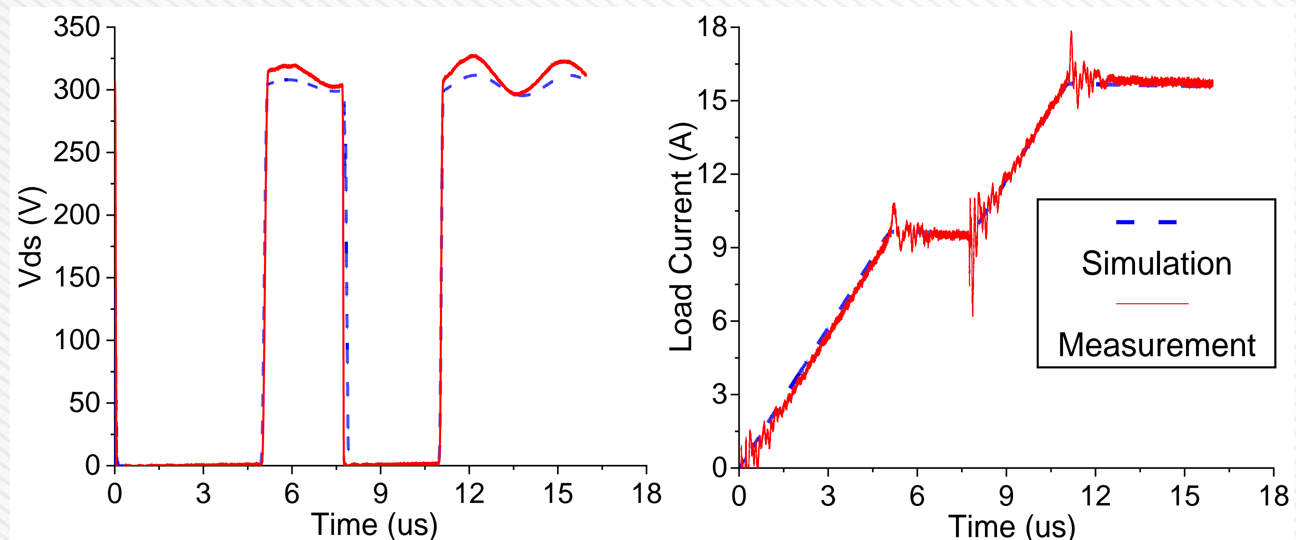
❑ Double Pulse Test Results



Schematic



Gate Pulse



DPT Results

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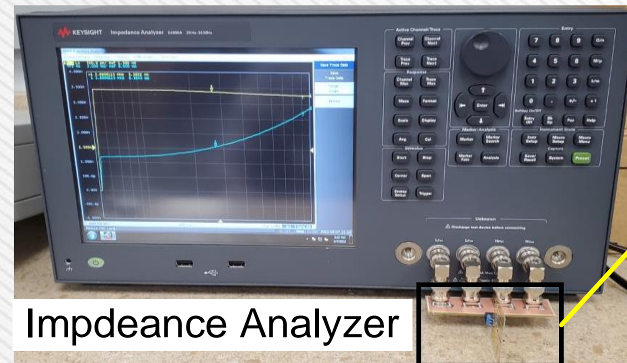
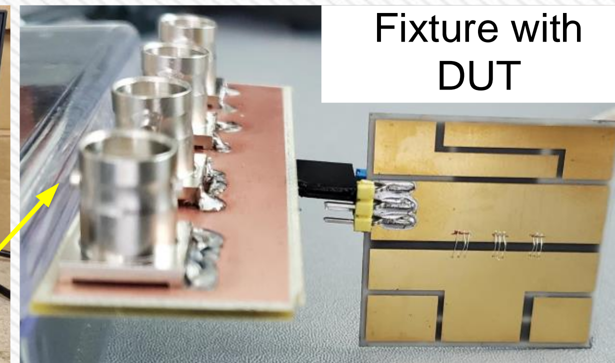
Electrical Validation

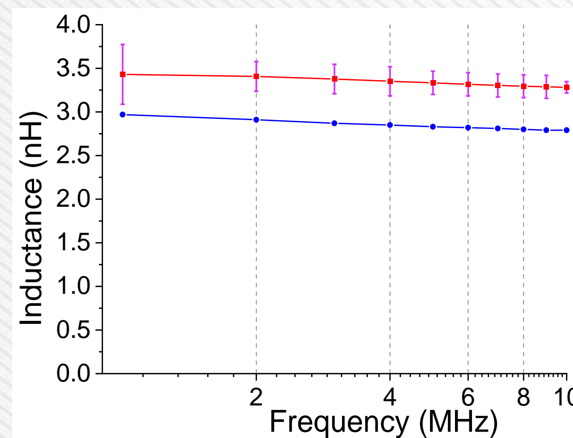
❑ Impedance Measurement

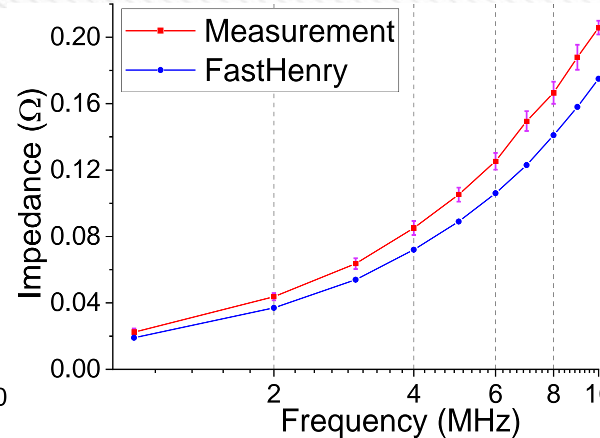
- Setup





- Results





Metric	Frequency	FastHenry	Measurement	Mismatch%
L (nH)	1 MHz	2.97	3.43	13.4%
Z (Ω)	10 MHz	0.175	0.20	12.5%

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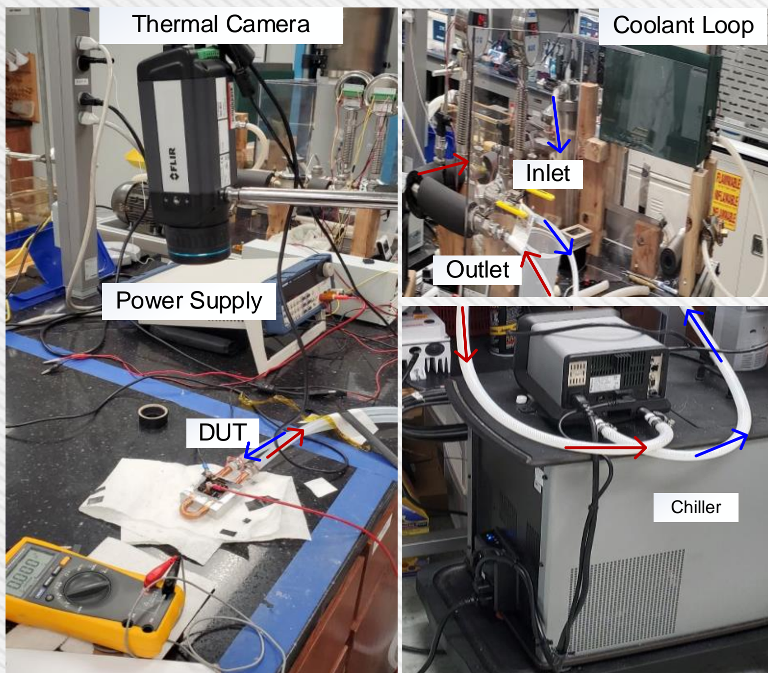
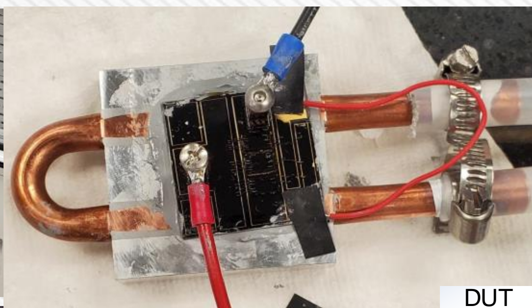
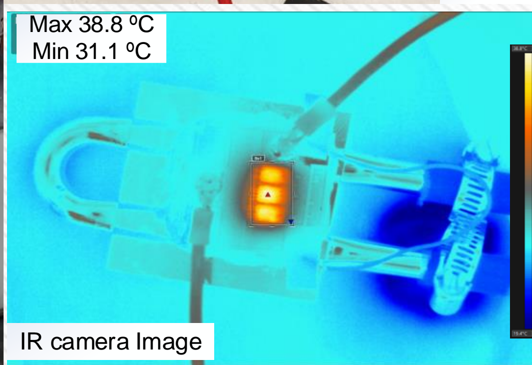
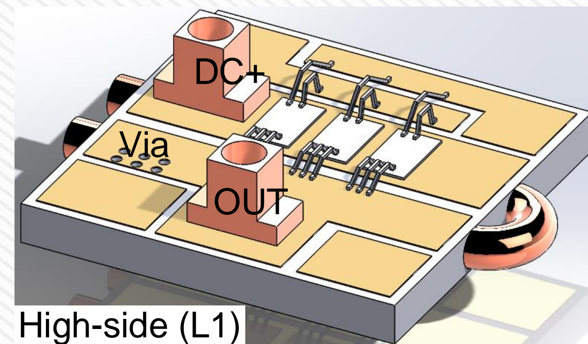
Thermal Validation

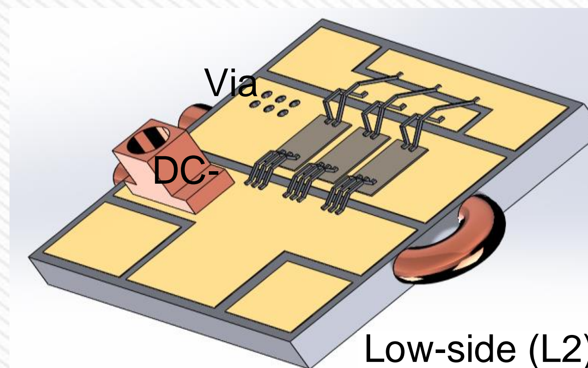
❑ Embedded Cooling Concept







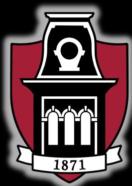




Boundary Conditions:

- Heat dissipation/die: 10.2 W
- Effective h: 7394 W/m²K
- Ambient T: 297 K

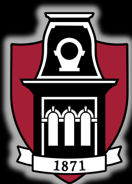
Case	Maximum Temperature (ºC)			% of Mismatch
	D1	D3	D5	
Measurement	37.00	38.80	37.90	-
ParaPower	40.75	42.30	40.78	9.02%



Comparison Against Manual Designs

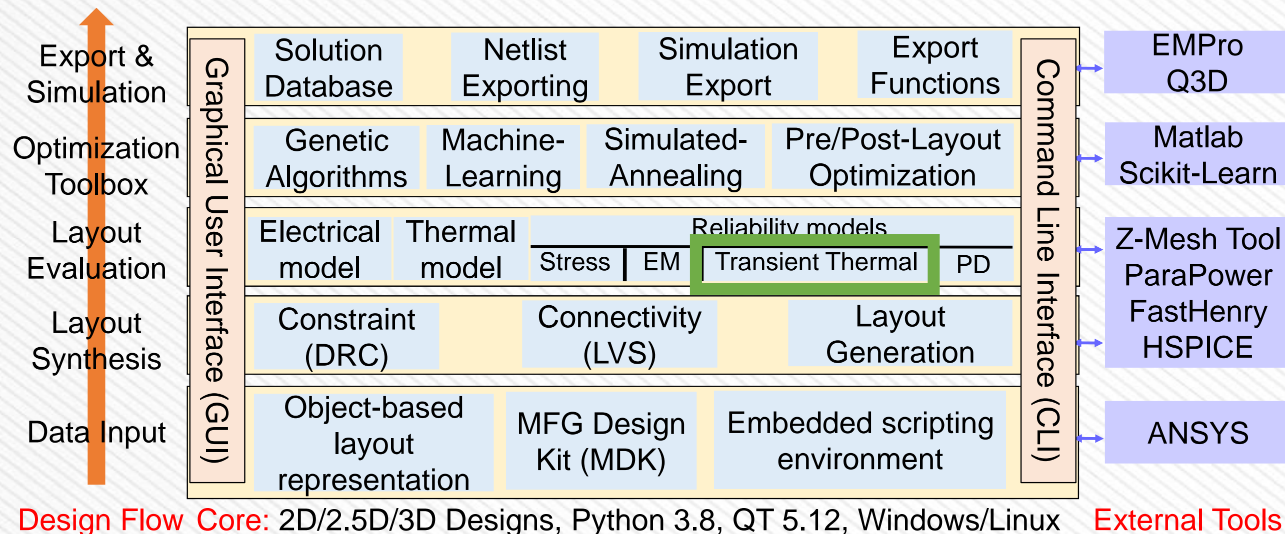
Source	Architecture	Packaging	Power Loop Inductance (nH)	Cooling	Device Rating	Devices/ Sw. Position	Area ($mm \times mm$)
[84]	2D Phase-leg	Wire-Bonded	9.7 (Planar loop)	Single	1200 V/ 100 A	5 SiC MOS	88.1 × 50.1
[85]	2D Half-bridge	Wire-Bonded	7.5 (Vertical loop)	Dual	650 V/ 200 A	3 SiC MOS	60 × 80
[86]	2.5D Half-bridge	Hybrid	2.60 (Vertical loop)	Dual	1200 V/ 90 A	1 SiC MOS	40 × 37
[87]	2.5D Half-bridge	Hybrid	3.38 (Vertical loop)	Single	1200 V/ 24 A	1 SiC MOS	21 × 11.5
[88]	2.5D Half-bridge	Hybrid	4.3 (Vertical loop)	Single	1200 V/ 40 A	2 SiC MOS	23.7 × 14.2
[89]	2.5D H-bridge	Wire Bondless	4.5 (Vertical loop)	Dual	1200V/ 50A	4 SiC MOS	76.9 × 74.9
PS v1.9	2D Half-bridge/ 2.5D Full-bridge	Wire-Bonded	7.58 (Planar loop)	Single	1200 V/ 40 A	2 SiC MOS	40 × 40
[90]	3D Half-bridge	Wire-Bondless	0.93 (Vertical loop)	Dual	650 V/ 60 A	2 GaN HEMT	45 × 35
[91]	3D Half-bridge	Wire Bondless	4 (Vertical loop)	Dual	1200 V/ 50A	2 Si IGBT	42.5 × 40.1
[92]	3D Half-bridge	Flip-chip	4.5 (Vertical loop)	Dual	900 V/ 194 A	2 SiC MOS	28 × 50.5
[92]	3D Half-bridge	Wire Bondless	5.1 (Vertical loop)	Dual	3300 V/ 50 A	2 SiC MOS	27 × 46.4
PS v2.0	3D Half-bridge	Wire-Bonded	3.43 (Vertical loop)	Embedded	900 V/ 194 A	3 SiC MOS	37.5 × 37.5

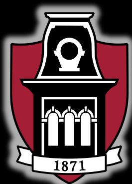
Imam Al Razi, “Constraint-Aware, Scalable, and Efficient Algorithms for Multi-Chip Power Module Layout Optimization”, Ph.D. Dissertation, July 2022.



Outline

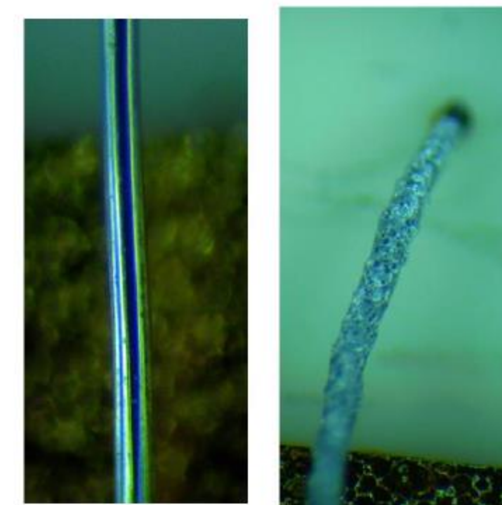
- ❑ Introduction
- ❑ Motivations & Contributions
- ❑ Constraint-Aware Layout Engine
  - Layout Representation
  - Methodology
  - Results
    - Minimum-Sized Results
    - 3D MCPM Layout Optimization & Hardware Validation
- ❑ **Reliability Optimization**
  - **Thermal Cycling Impact Minimization**
  - Electromigration (EM) Impact Minimization
- ❑ Conclusion & Future Work



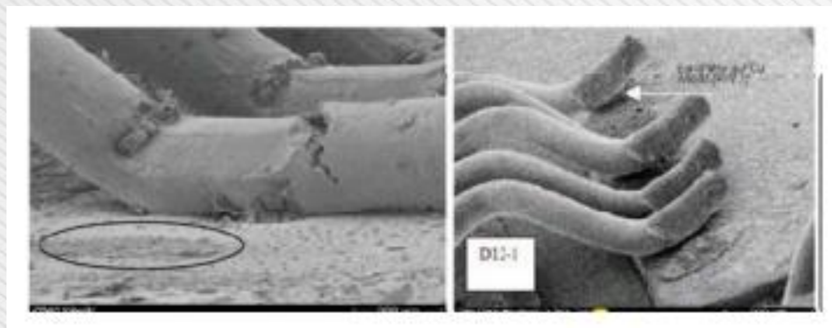


Reliability Optimization

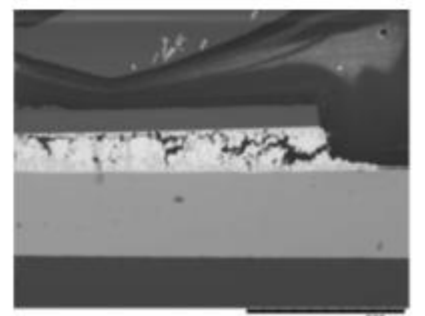
- **To perform reliable operation:**
  - **Electro-thermal optimization is critical but not enough**
  - **At high power density, a few dominating threats for lifetime**
    - Thermal/Power cycling
    - Electromigration (EM)
    - Mechanical stress
    - Partial discharge (PD)



Before **After**

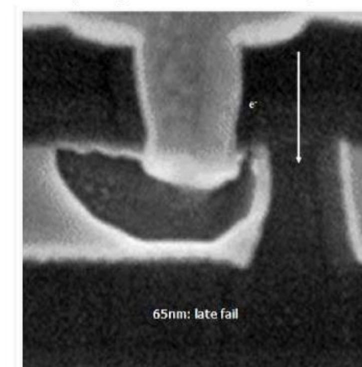


Wire bond failure

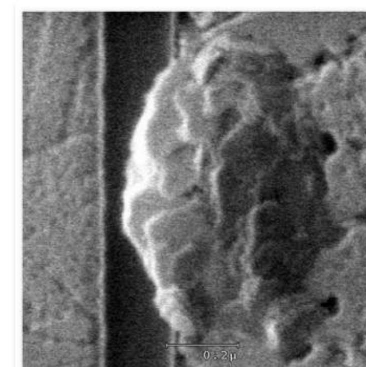


Solder fatigue and void formation

Thermal cycling impact



void formation

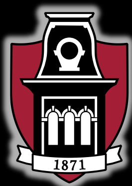


Short ckt formation

EM impact on interconnect

Li-Ling Liao et. al., "Power Cycling Test and Failure Mode Analysis of High-Power Module," *ICEP*, 2016

Whit Vinson, "Development of an Accelerated Life Testing Method for Reliability Assessment of Wire Bonded Interconnects Subjected to Mechanical and Electromigratory Stresses," Master's thesis, Dept. of Mechanical Engineering, University of Arkansas, 2022.



Reliability Optimization Using PowerSynth

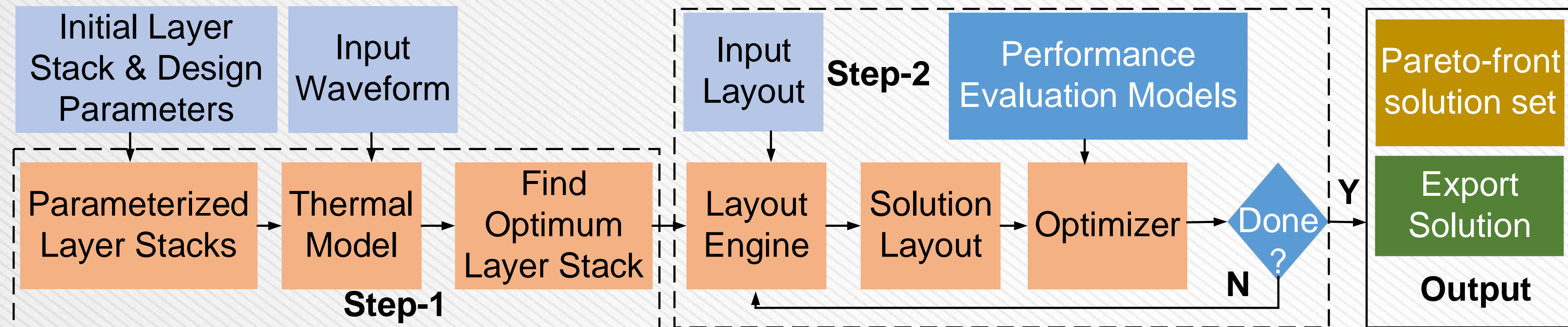
- **PowerSynth 2 allows:**
  - **Integration external modeling efforts/tools through APIs**
    - ParaPower: Army Research Lab (ARL) developed thermal and stress evaluation tool
  - **Handling both types of interconnects (i.e., wire bonds and solder joints)**
  - **Considering arbitrary layer stack**
  - **Material library modification**
- **To perform reliability optimization, it requires efficient, and accurate models**
- **In this work, MCPM layouts are optimized for two major reliability threats:**
  - **Thermal cycling impact minimization**
    - Transient thermal model for 2D MCPM layouts
    - Phase change material (PCM) consideration
  - **Electromigration associated risk assessment**
    - Current density modeling through Z-Mesh tool

ARL ParaPower, "https://github.com/USArmyResearchLab/ParaPower".

Thermal Cycling Impact Optimization

❑ **Two-step optimization flow:**

- **Step-1: Layer stack optimization**
  - Material, thickness variation
- **Step-2: Layout optimization**
  - Placement of devices & routing of traces
  - Variable floorplan sizes



- **Newly developed transient thermal model:**
  - Max, average, peak-to-peak temperature evaluation
  - Both static and transient thermal evaluation
  - Interaction among three tools

HSPICE

Imam Al Razi et. al., “PowerSynth-Guided Reliability Optimization of Multi-Chip Power Module”, APEC, pp. 1516-1523, 2021

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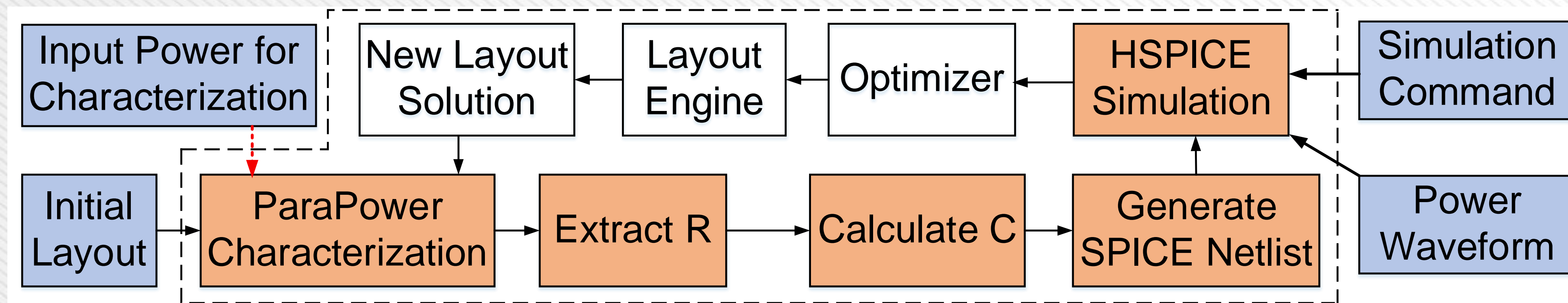
Transient Thermal Model

❑ Transient Thermal Model for 2D Layouts:

- Generic layer stack handling with the latest layout engine of PowerSynth.
- Represents MCPM structure as a cauer thermal RC network
- Thermal resistance (R) extraction through ParaPower characterization
- Thermal capacitance (C) value calculation using material properties.
- PCM is modeled as voltage (temperature) dependent variable R and C.
- HSPICE engine: solves RC-network to produce temperature metrics result

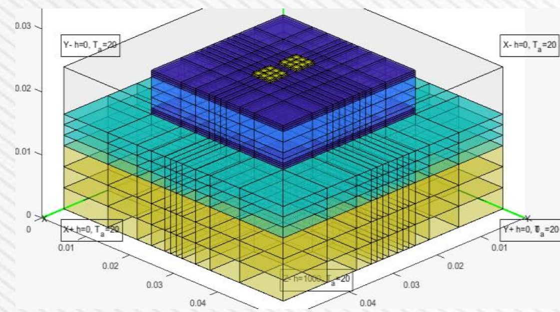
- **More capabilities:**
  - Performance evaluation under input waveform parameters sweep
  - Find the optimum operating waveform for a given layer stack.



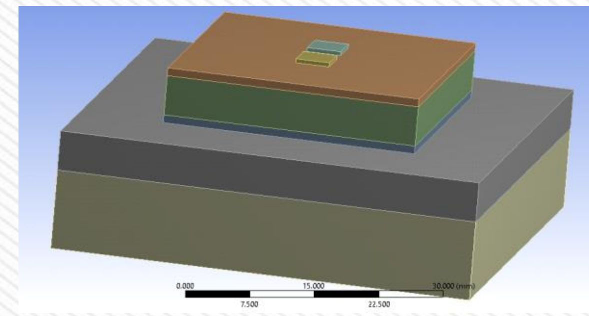
Model Validation

❑ An example layer stack and corresponding validation structure

Layer stack

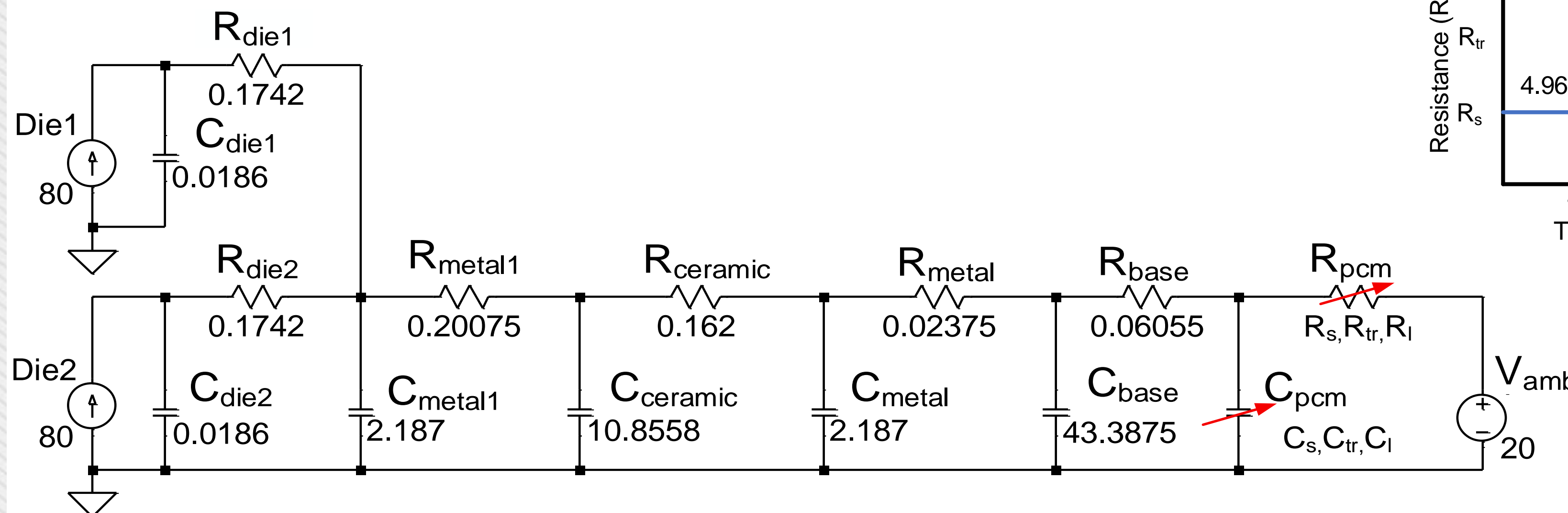


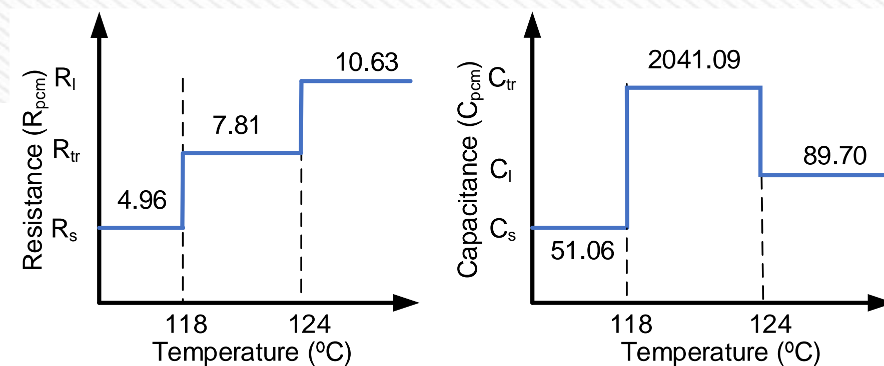
ParaPower structure



ANSYS structure

❑ Corresponding Cauer thermal network:





Variable R,C values for PCM

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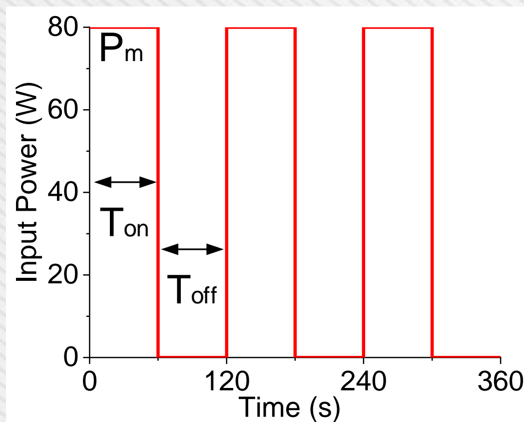
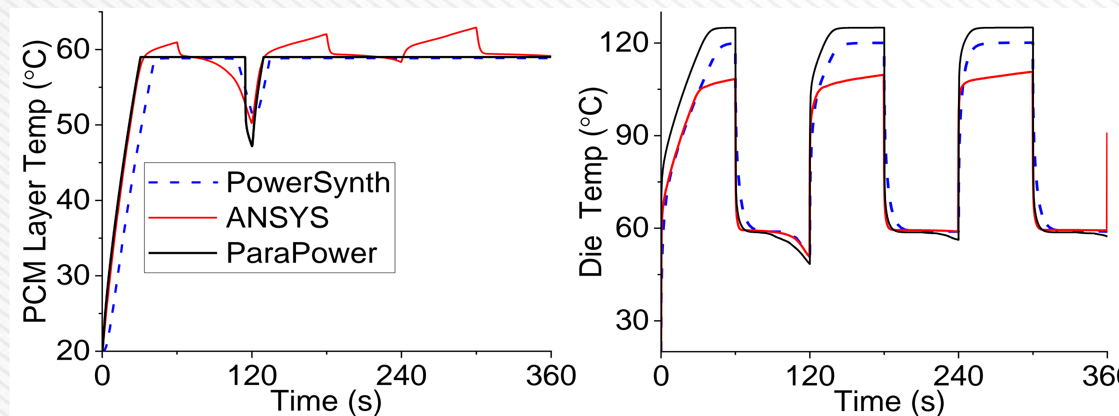
Validation Results

❑ Input waveform and Resultant PCM, die layer temperature:



Input Waveform



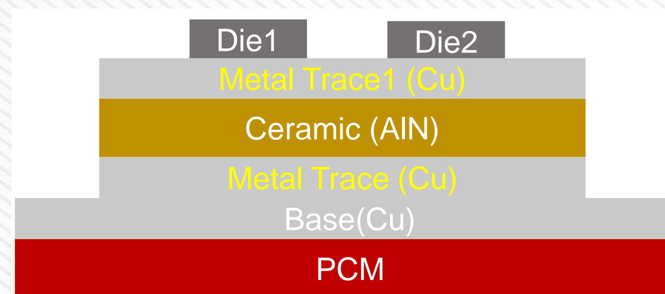
Resultant Waveform

❑ Performance comparison result:

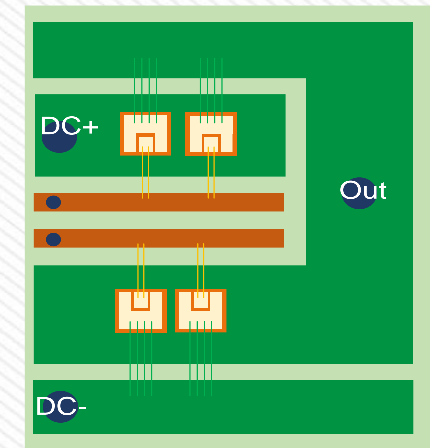
Approach	Max Temp. (ºC)	Avg. Temp. (ºC)	P-to-P Temp. (ºC)	Runtime (s)	Speedup	Memory (MB)
ANSYS	110.7	84.87	51.73	11165	1×	3373
ParaPower	125.0	90.64	68.67	35.27	316×	2361
PowerSynth	120.1	89.57	61.14	3.2	3489×	315

Reliability Optimization Case Study

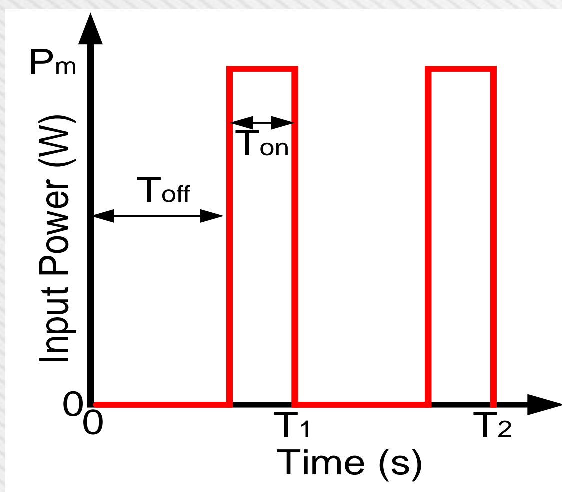
- **MCPM layer stack and layout for case study:**
  - 2D half-bridge power module
  - PCM layer is considered
- **Choosing thermal cycling waveform:**
  - Energy sweep: Varying Ton & Pm
  - Optimum waveform (Ton= 60 s, Pm= 40 W) is chosen based on the thermal metrics.



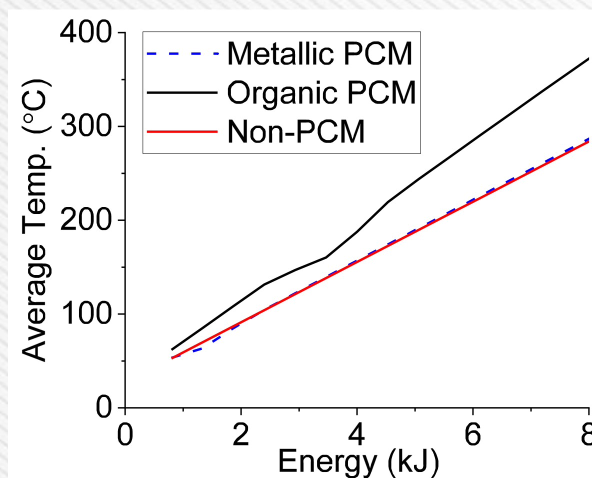
Layer stack

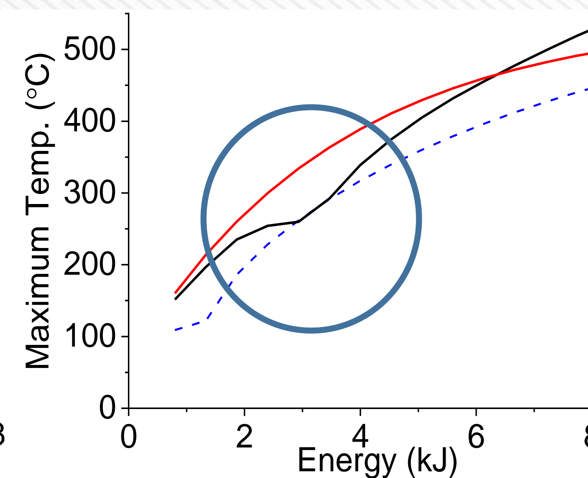


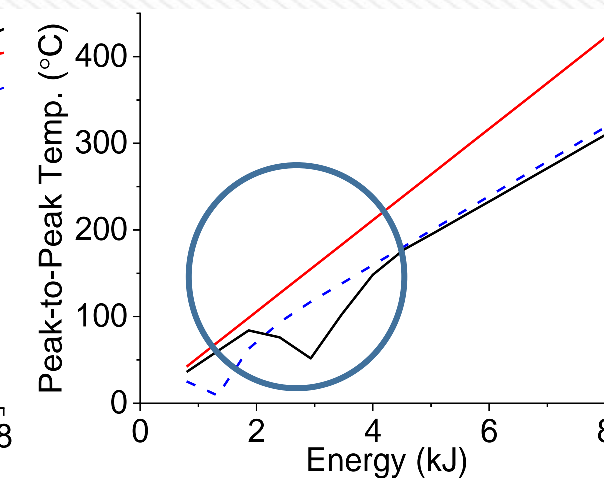
Half-Bridge MCPM Layout



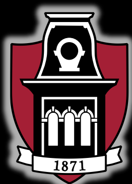
Sample Input Waveform







Energy sweep result



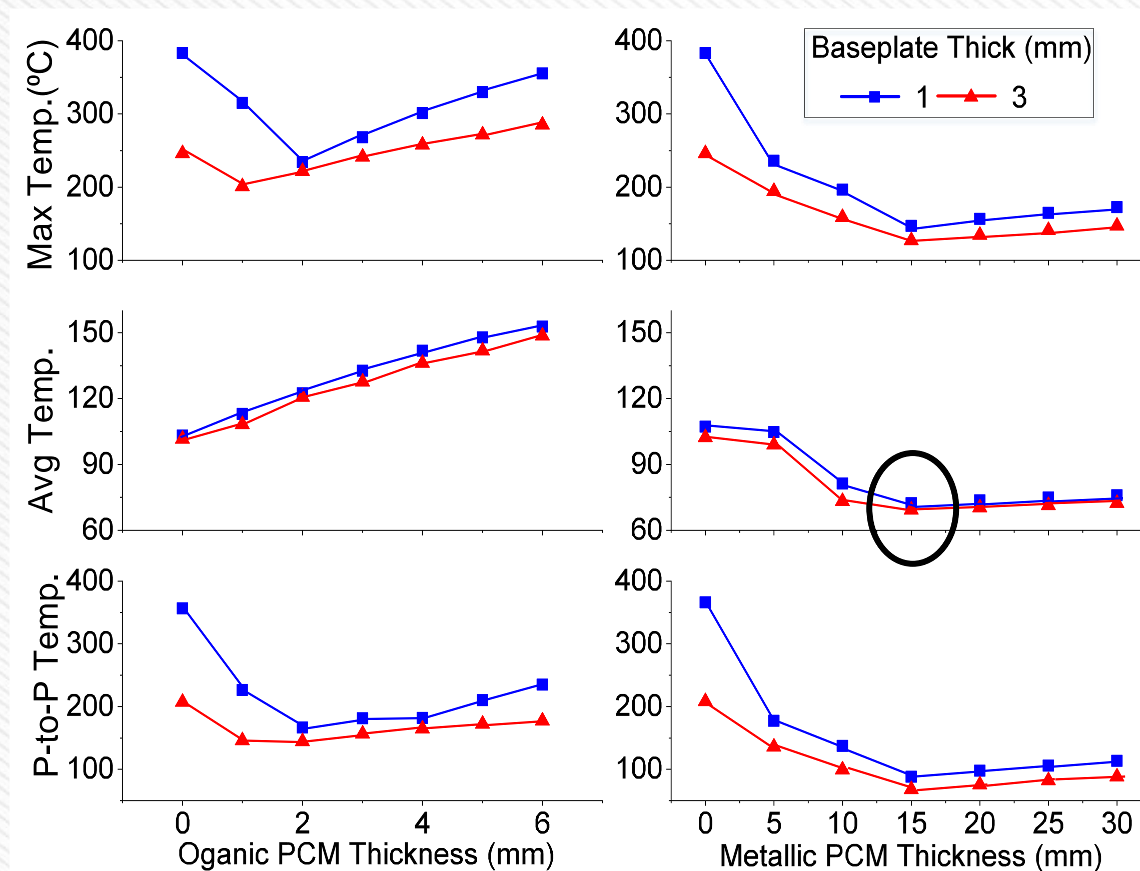
Layer Stack Optimization

❑ Step-1

- **Layer stack optimization**

Layer	Material	Thickness (mm)
Baseplate	Copper	1, 3
PCM	Fields' Metal (Metallic)	0, 5, 10, … 30
	Erythritol (Organic)	0, 1, 2, … 6

- **Optimum layer stack:**
  - 3 mm Copper baseplate
  - 15 mm Metallic PCM



Temperature metrics vs. thickness variation

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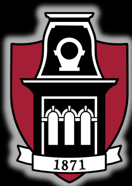
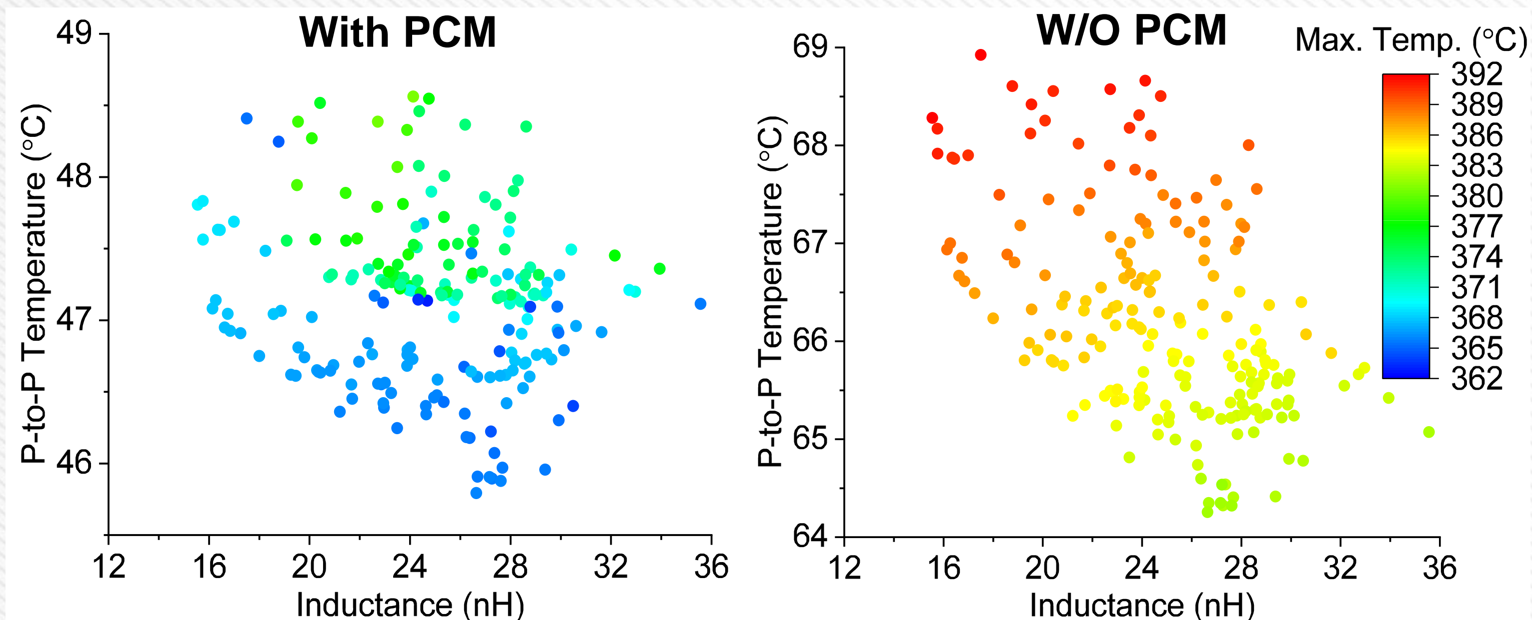


PCM vs Non-PCM Comparison

❑ Optimum layer stack vs. Non-PCM case

- **Layer stack choice:**
  - 3 mm Copper baseplate with no-PCM
  - 3 mm Copper baseplate with 15 mm metallic PCM (optimum layer stack)
- **Electro-thermal optimization**
  - 200 solutions for each
- **Input waveform:**
  - between 0 W to 40 W
  - 15% duty cycle
- **Total runtime:**
  - PCM→ ~815 s
  - Non-PCM→ ~147 s
- **PCM provides better thermal capacity over non-PCM**



Fixed-floorplan size (46 mm × 36 mm) solution space

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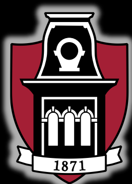
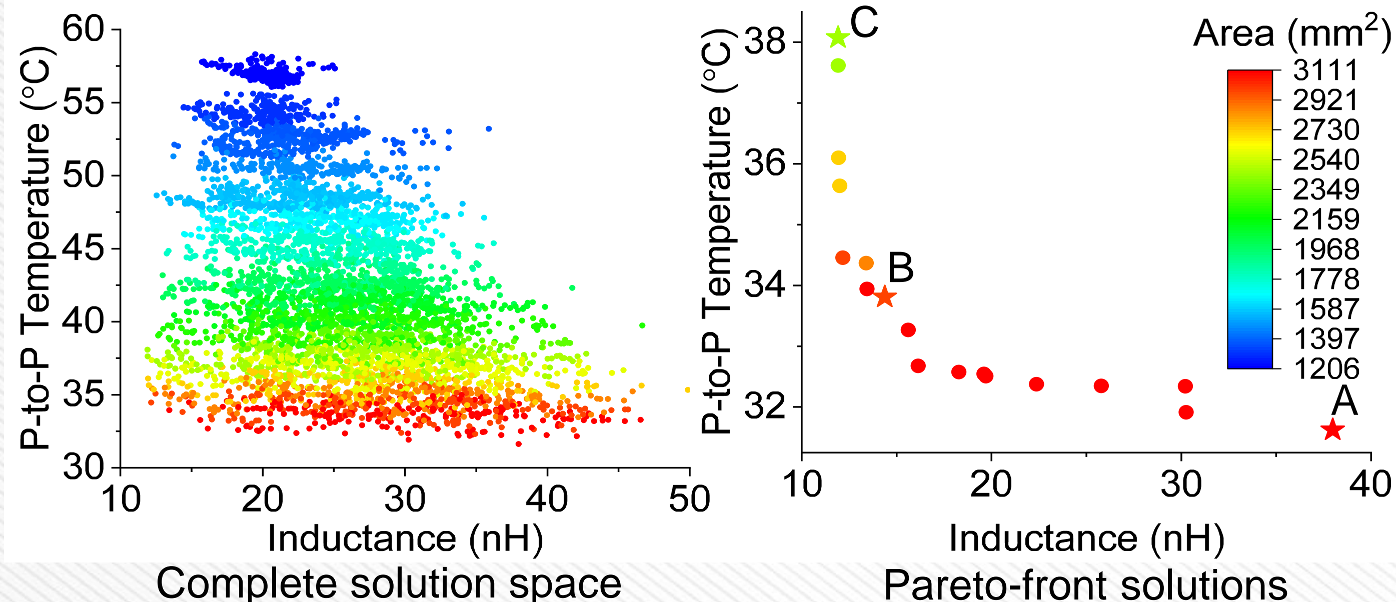


PowerSynth-Guided Layout Optimization

Step-2

- **Layout optimization**
  - Optimum layer stack is considered.
  - 6400 solutions with 32 different floorplan sizes.
  - For each size, 200 solutions are generated and evaluated (total runtime ~815 s)

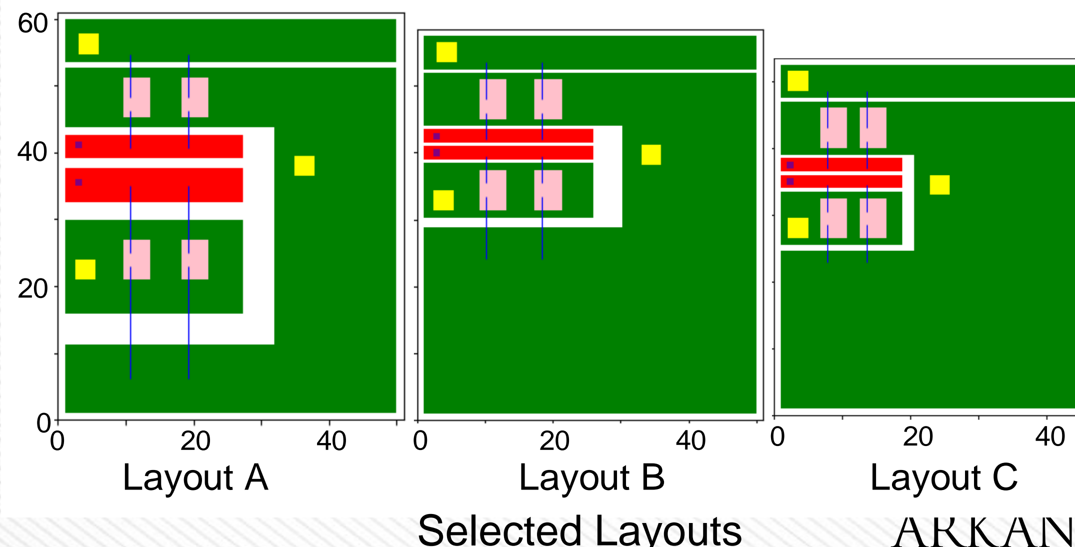


Complete solution space

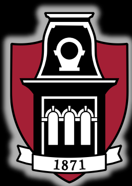
Pareto-front solutions

Performance Table

ID	Floorplan Size (mm × mm)	Loop Inductance (nH)	P-to-P Temperature (°C)
A	51 × 61	37.98	31.62
B	51 × 58.5	14.38	33.81
C	46 × 53.5	11.91	38.07



Selected Layouts



Outline

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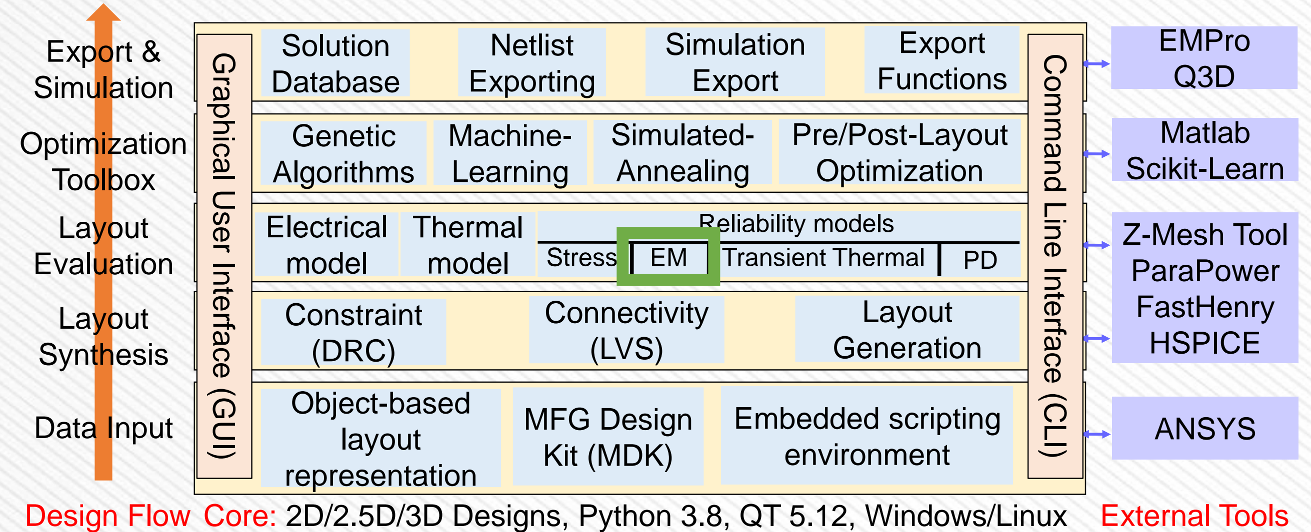

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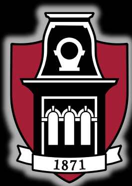
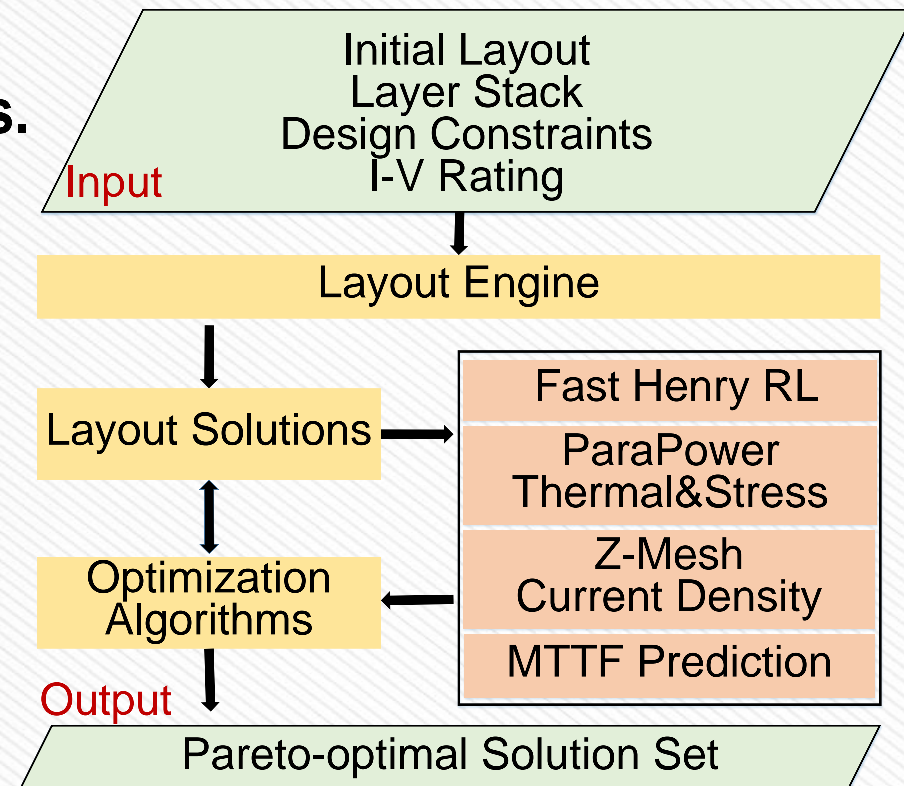


EM-Aware Reliability Optimization

Objectives:

- Quick assessment of risks associated with electro migration (EM) and mechanical failure of interconnects.
- Optimize power module layout to reduce the risk of failure of interconnect.

Methodology



Optimization workflow

- **Features to be considered:**
  - Layout generation capability with different interconnects
  - Fast and accurate model for current density estimation through interconnects.
  - Fast and accurate model for temperature and stress distribution

Imam Al Razi et. al., "Electromigration-Aware Reliability Optimization of MCPM Layouts Using PowerSynth", (accepted) in ECCE, 2022

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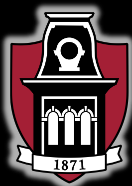

EM-Aware Reliability Optimization

❑ Implementation using PowerSynth 2 APIs:

❑ Mean Time To Failure (MTTF) Calculation :

- **Closed-formula approach (Black's Equation for Electromigration)**

  $MTTF = A\, j^{-2} \exp(E_a/kT)$,

  where, A = constant, j = current density, E_a = Activation energy, k = Boltzman constant, T= Temperature

- **Data-Driven Model**
  - Look-up table from experimental results
  - Parameter tuning on analytical models from experimental results

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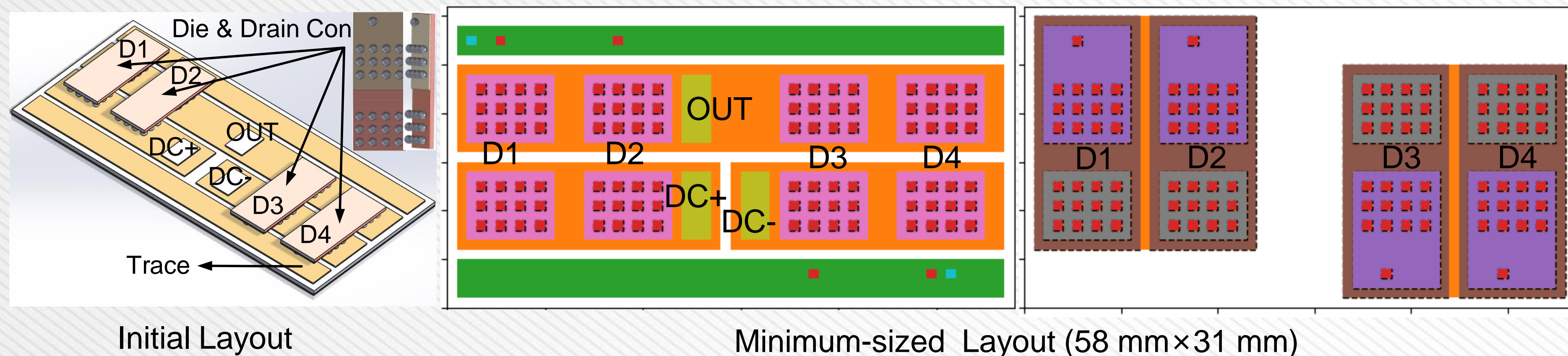
Case Study I

❑ Layout Solution Generation

- **Flip-Chip Design:**
  - Half-bridge module: 2 SiC devices/switching position
  - Source side is directly bonded
  - Drain side is extended through metallic connector and bonded with traces through solder balls.



Initial Layout

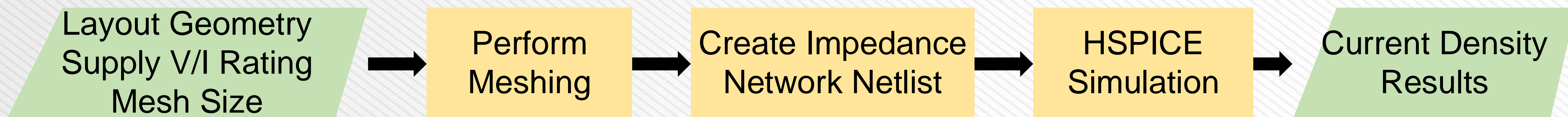
Minimum-sized Layout (58 mm×31 mm)

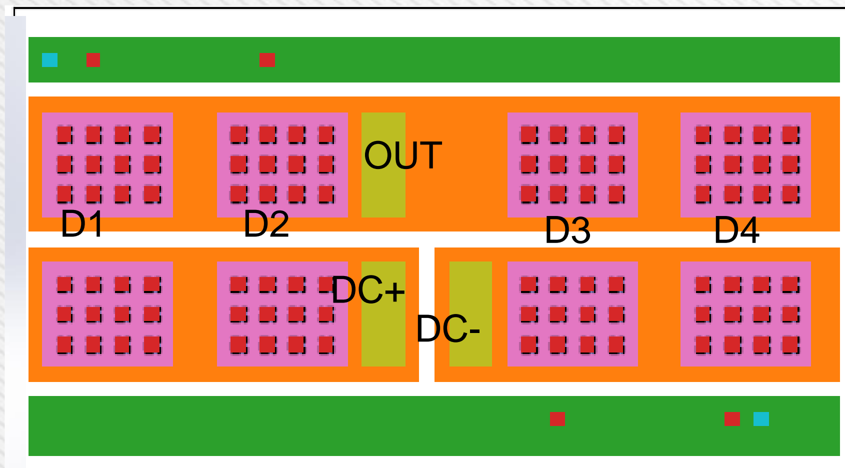
❑ Current Density: Z-Mesh tool

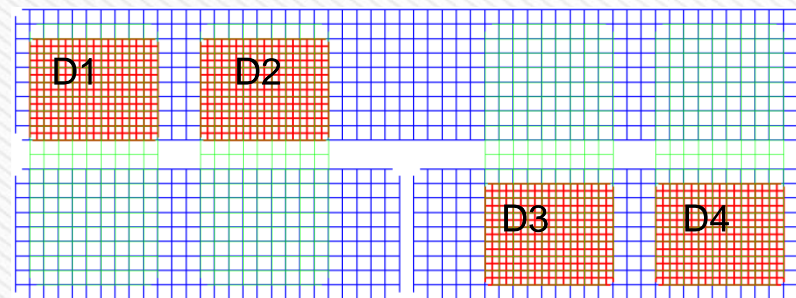
❑ Temperature Distribution: ParaPower

Z-Mesh Modeling

❑ Workflow







Z-mesh (power loop only)

❑ Performance Comparison

Model	Runtime (s)	Speedup	Memory (MB)	Memory Reduction
ANSYS	310	×1	10329	×1
Z-Mesh	0.28	×1107	513	×20

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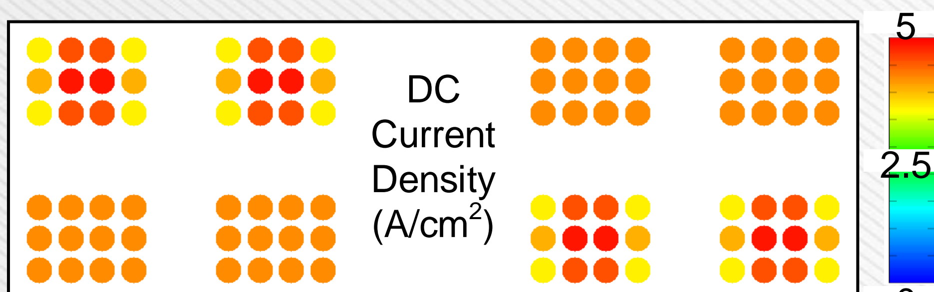
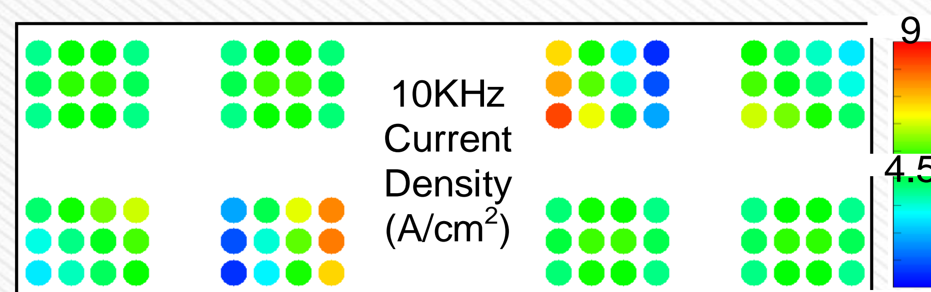
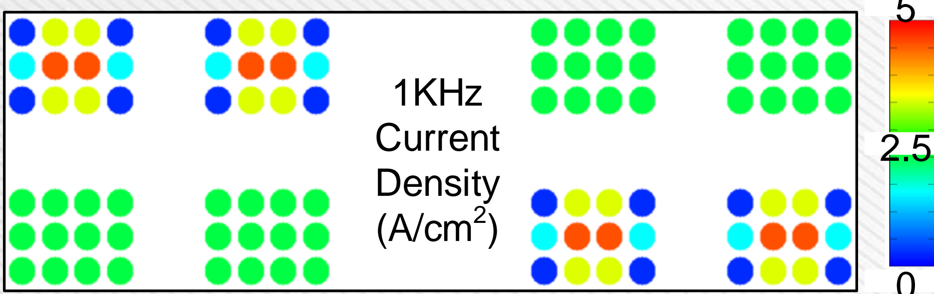
Current Density Results

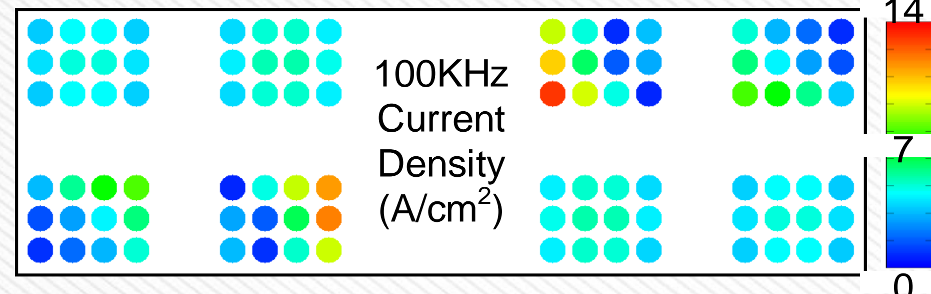
❑ Frequency Dependent Current Density

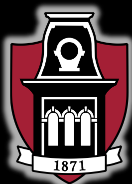
- At DC, intra-die current density variation is observed
- Frequency increases → loop impedance increases → inter-die current density variation increases
  - Solder joints close to the DC+ and DC- : Higher current density
  - Solder joints away from the DC+ and DC- : Lower current density





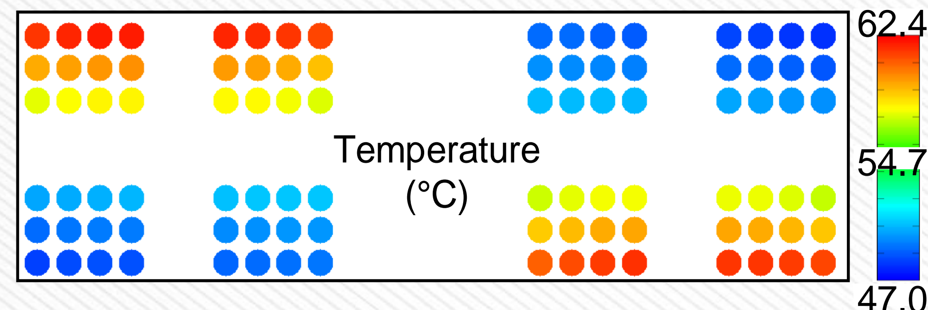


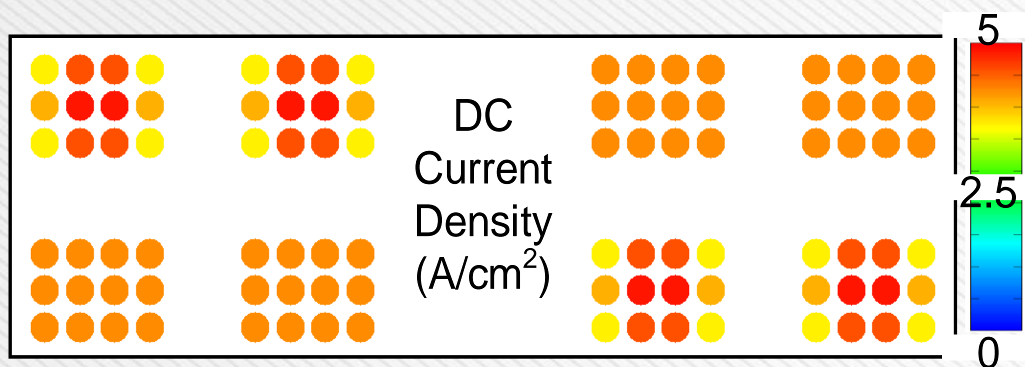


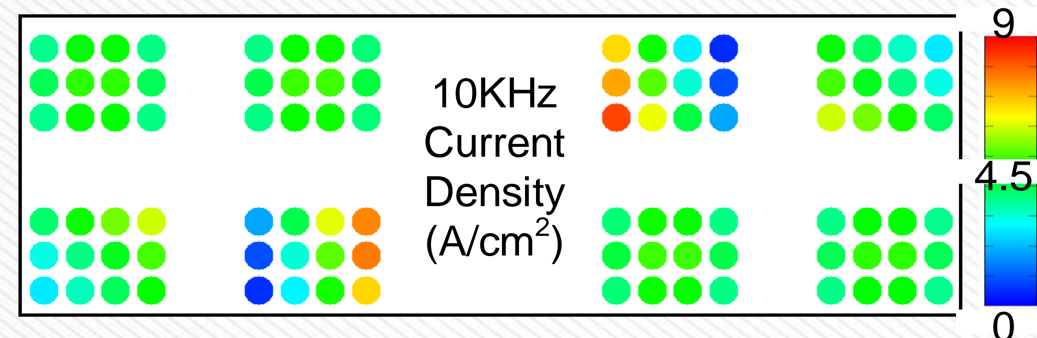


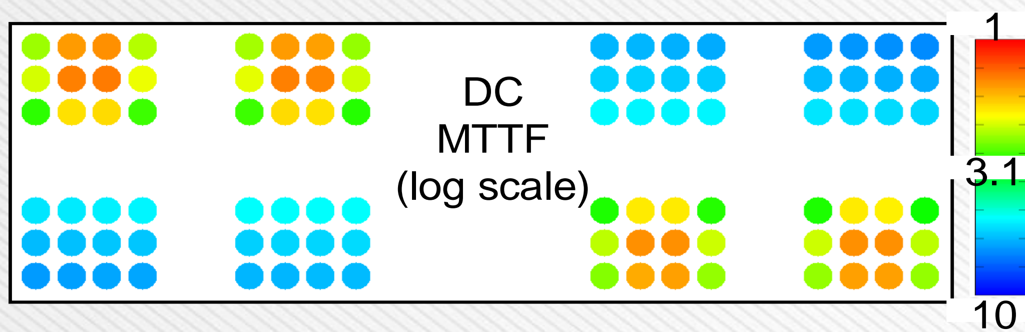
MTTF Results

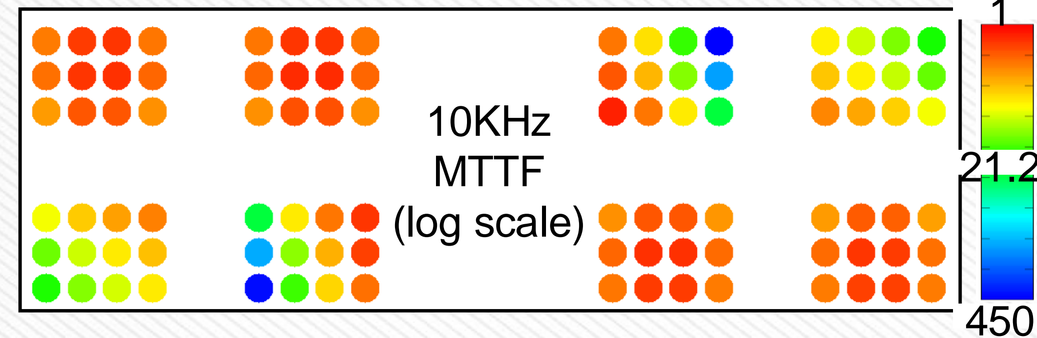
- **MTTF: DC vs AC**
  - At DC: Temperature is dominant
  - At AC: Temperature and current density both are critical











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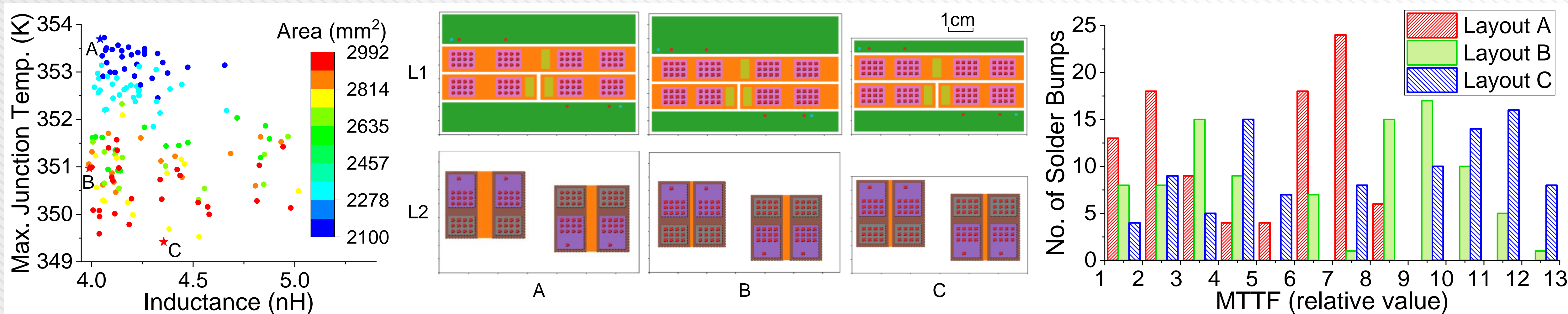
Optimization Results

❑ Approach 1: Floorplan area variation

- 10 floorplan sizes : 15 solutions/size (135 s/ layout solution)
- L: FastHensry, T: ParaPower, J: Z-Mesh tool.



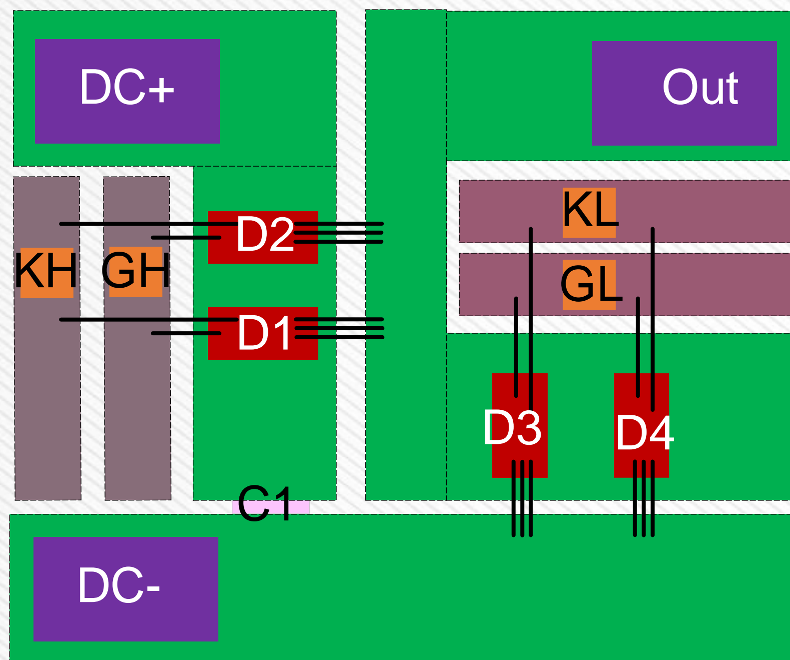
❑ Approach 2: Fixed floorplan # of solder ball variation

Solder Array	Max J (A/cm²)	Max Temp. (ºC)	MTTF	Improvement
4 × 3	4.86	62.43	1.19	×1
5 × 4	3.13	62.34	2.89	×2.4

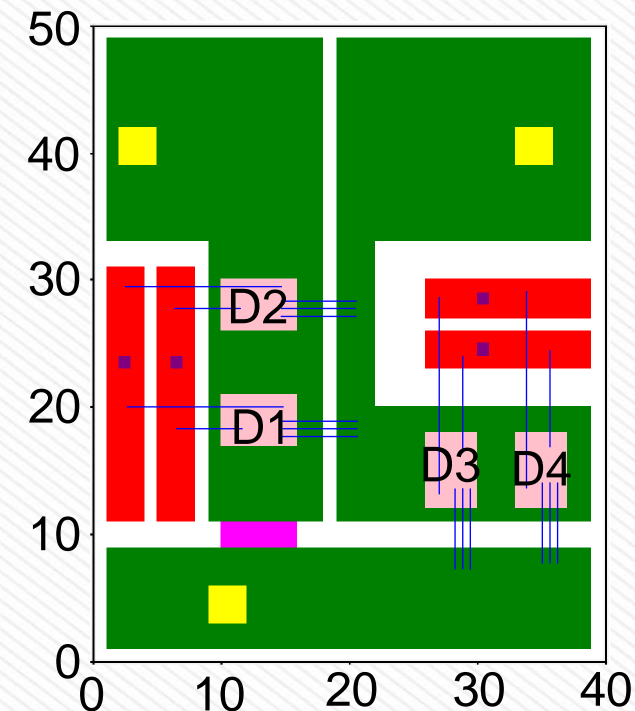
Case Study II

❑ Layout Solution Generation

- **Wire bonded 2D module:**
  - Half-bridge module: 2 SiC devices/switching position
  - Three 5 mil Aluminum wire bonds per device
  - Embedded decoupling capacitor (C)
  - Hardware validated parasitic extraction result
  - Temperature distribution result from ParaPower

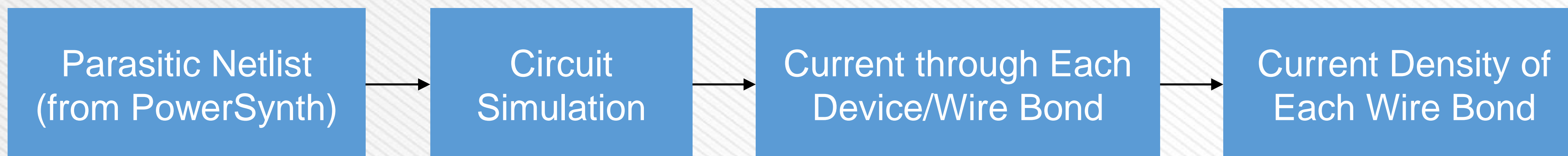


Initial Layout



Optimized Solution (40 mm × 50 mm)

❑ Current density extraction steps:

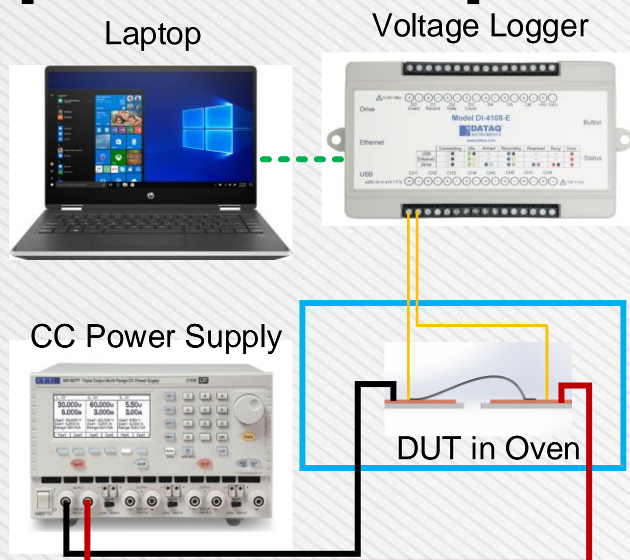


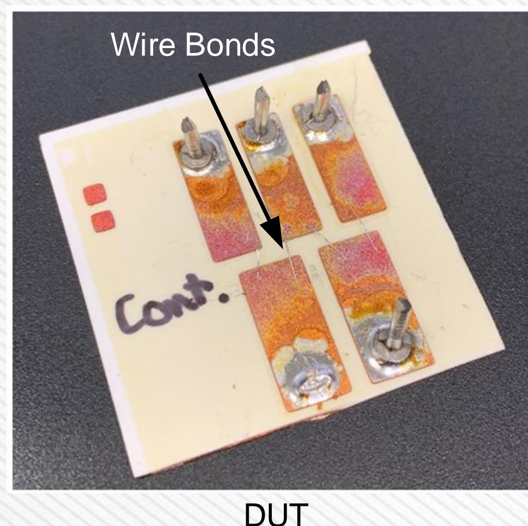
MTTF Results

- **Current Density Extraction**
  - Supply current ~ 23 A
- **Reliability Metric:**
  - 10% increase in R of the wire bond

Device	Current (A)	Temperature (K)	Wire Bond Current Density (A/cm2)	10% R Increment Time (Hrs)
D1	11.53	416.8	3.03×10^4	217.4
D2	11.26	416.5	2.95×10^4	229.6
D3	11.55	427.0	3.03×10^4	210.8
D4	11.24	427.7	2.95×10^4	221.9

- **Experimental Setup & Results**





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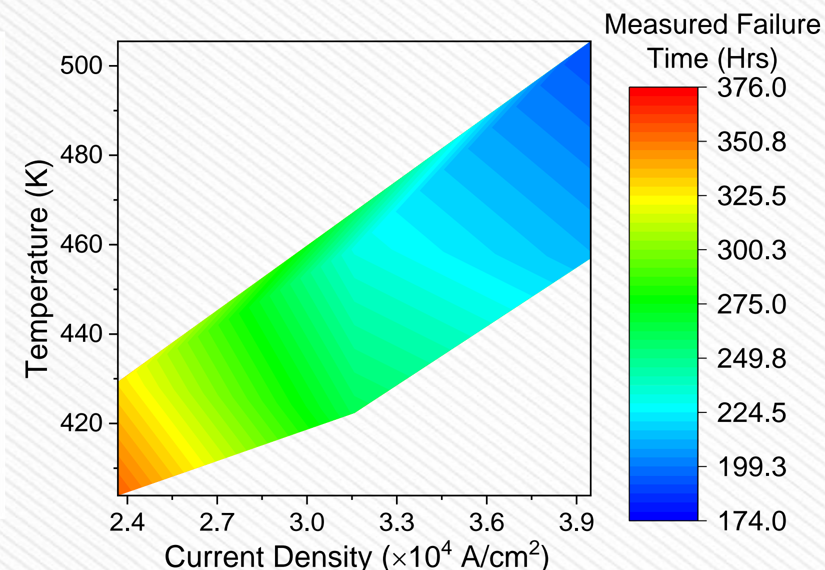
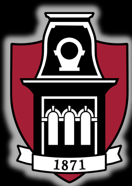


V. Whit, "Development of an Accelerated Life Testing Method for Reliability Assessment of Wire Bonded Interconnects Subjected to Mechanical and Electromigratory Stresses," Master's thesis, Dept. of Mechanical Engineering, University of Arkansas, 2022.



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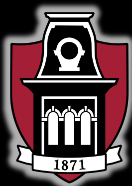
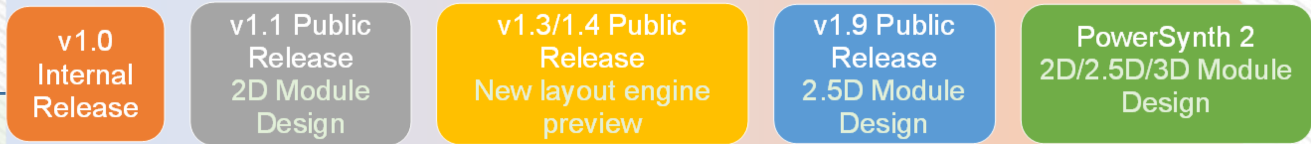


PowerSynth Progression

PowerSynth Development Summary

Release Webpage: https://e3da.csce.uark.edu/release/PowerSynth/

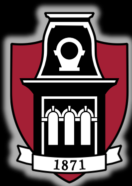


- **Features**

PS v1.3/1.4
  - 2D layouts with complex geometry
  - Constraint-aware, flat-level layout engine
  - Heterogeneous components
  - Multiple optimization techniques

PS v1.9
  - All 2D/2.5D Manhattan geometries
  - Hierarchical layout representation & optimization
  - Larger solution space
  - Hardware-validated optimization result

PS v2.0
  - All 2D/2.5D/3D Manhattan layouts
  - Both GUI and CLI for users
  - Randomization and NSGAII
  - Electro-thermal and reliability optimization
  - Hardware-validated CAD flow



Conclusions

- **PowerSynth is the first power module layout synthesis and optimization framework promising for design automation in the power electronics industry.**
  - **Generic and hierarchical representation technique → All 2D/2.5D/3D Manhattan Layouts**
  - **Design and reliability constraints → 100% DRC-clean and reliable solutions**
  - **Scalable, and efficient layout engine → All SOTA 2D/2.5D/3D power modules optimization**
  - **Both 2D/2.5D and 3D CAD flow have been hardware-validated**
  - **PowerSynth flow vs. traditional approach → Order of magnitude productivity improvement**
    - Accuracy: 10-15%, Speedup: X1000, Memory reduction: X100
  - **First tool to consider electro-thermo-mechanical and reliability co-optimization.**
  - **Both GUI and command-line interfaces for users**
  - **PowerSynth v2.0 release package with test cases and user manual.**
  - **Limitations:**
    - Initial layout dependency
    - Lacking of 3D visualization feature in GUI
    - Reliability models are not hardware-validated
    - Unable to handle non-Manhattan routing

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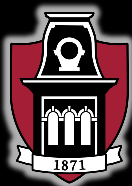
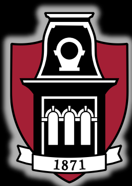


Future Work

- **Potential Improvements:**
  - **Develop a generic layout description language**
  - **Reduce the correlation among components to generate more variations in the layout solutions**
  - **Two-folded optimization can be performed to improve the optimization result quality:**
    - Implement template selection procedure to choose the initial layout
    - Perform optimization on the best initial layout
  - **Implement layout synthesis engine for generic 2D/2.5D/3D layouts**
  - **Add performance improvement tolerance as another stop criteria for genetic algorithm.**
  - **Implement machine learning/ deep learning-based optimization approach.**
  - **Update the transient thermal model to handle 3D layouts.**
  - **Stress impact needs to be added to EM modeling effort.**
  - **Hardware validation of more 3D layouts with complicated structures.**



Publications(1/2)

❑ Journals

[1] Imam Al Razi, Quang Le, Tristan Evans, H. Alan Mantooth, and Yarui Peng, "PowerSynth 2: Physical Design Automation for High-Density 3D Multi-Chip Power Modules," (Major revision) in in IEEE Transactions of Power Electronics.

[2] Quang Le, **Imam Al Razi**, Tristan Evans, Shilpi Mukherjee, Yarui Peng, and H. Alan Mantooth, "Fast and Accurate Parasitic Extraction in Multichip Power Module Design Automation Considering Eddy-Current Losses", (accepted) in IEEE Journal of Emerging and Selected Topics in Power Electronics, 2022.

[3] Imam Al Razi, Quang Le, Tristan Evans, Shilpi Mukherjee**,** H. Alan Mantooth, and Yarui Peng**,** "PowerSynth Design Automation Flow for Hierarchical and Heterogeneous 2.5D Multi-Chip Power Modules", IEEE Transactions on Power Electronics, vol. 36, no. 8, pp. 8919-8933, 2021.

[4] Yarui Peng, Quang Le, **Imam Al Razi**, Shilpi Mukherjee, Tristan Evans, and H. Alan Mantooth, "PowerSynth Progression on Layout Optimization for Reliability and Signal Integrity", IEICE Nonlinear Theory and Its Applications, vol. 11, no. 2, pp. 124–144, Apr 2020, Invited Paper.

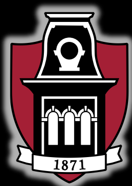
[5] Tristan Evans, Quang Le, Shilpi Mukherjee, **Imam Al Razi**, Tom Vrotsos, Yarui Peng, and H. Alan Mantooth, "Powersynth: A Power Module Layout Generation Tool", IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5063–5078, Jun 2019, Highlighted Paper.

❑ Conferences

[6] David Huitink, Whit Vinson, Collin Ruby, **Imam Al Razi**, and Yarui Peng, "Factoring Interacting Stress Mechanisms in Design for Reliability of Extreme Environment Power Modules", (under review) in Proc. IEEE Workshop on Wide Bandgap Power Devices and Applications, 2022.

[7] Imam Al Razi, Whit Vinson, David Huitink, and Yarui Peng, "Electromigration-Aware Reliability Optimization of MCPM Layouts Using PowerSynth", (accepted) in Proc. IEEE Energy Conversion Congress and Exposition, 2022.

[8] Imam Al Razi, Quang Le, H. Alan Mantooth, and Yarui Peng, "Hierarchical Layout Synthesis and Optimization Framework for High-Density Power Module Design Automation", in Proc. International Conference on Computer-Aided Design, pp. 1-8, Nov 2021.



Publications (2/2)

Conferences

[9] Joshua Mitchener, **Imam Al Razi**, and Yarui Peng, "Designing a Graphical User Interface for the Power Module Optimization Tool PowerSynth", in Proc. ASEE Midwest Section Conference, pp. 1-12, Sep 2021.

[10] Quang Le, **Imam Al Razi**, Yarui Peng, and H. Alan Mantooth, "PowerSynth Integrated CAD Flow for High Density Power Modules", in Proc. IEEE Design Methodologies Conference, pp. 1-6, Jul 2021.

[11] Quang Le, **Imam Al Razi**, Yarui Peng, and H. Alan Mantooth, "Fast and Accurate Inductance Extraction For Power Module Layout Optimization Using Loop-Based Method", in Proc. IEEE Energy Conversion Congress and Exposition, pp. 1358-1365, Oct 2021.

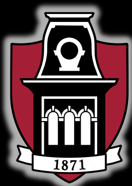
[12] Imam Al Razi, David Huitink, and Yarui Peng, "PowerSynth-Guided Reliability Optimization of Multi-Chip Power Module", in Proc. IEEE Applied Power Electronics Conference, pp. 1516-1523, Jun 2021.,.

[13] Imam Al Razi, Quang Le, H. Alan Mantooth, and Yarui Peng, "Physical Design Automation for High-Density 3D Power Module Layout Synthesis and Optimization", in Proc. IEEE Energy Conversion Congress and Exposition, pp. 1984–1991, Oct 2020.

[14] Bakhtiyar Md Nafis, Ange Iradukunda, **Imam Al Razi**, David Huitink, and Yarui Peng, "System-level Thermal Management and Reliability of Automotive Electronics: Goals and Opportunities in the Next Generation of Electric and Hybrid Electric Vehicles", in Proc. ASME International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems, pp. 1–8, Oct 2019.

[15] Imam Al Razi, Quang Le, H. Alan Mantooth, and Yarui Peng, "Hierarchical Layout Synthesis and Design Automation for 2.5D Heterogeneous Multi-Chip Power Modules", in Proc. IEEE Energy Conversion Congress and Exposition, pp. 2257–2263, Sep 2019.

[16] Imam Al Razi, Quang Le, H. Alan Mantooth, and Yarui Peng, "Constraint-Aware Algorithms for Heterogeneous Power Module Layout Synthesis and Optimization in PowerSynth", in Proc. IEEE Workshop on Wide Bandgap Power Devices and Applications, pp. 323–330, Oct 2018.



Thank You

Questions?

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