Electromigration-Aware Reliability Optimization of MCPM Layouts Using PowerSynth

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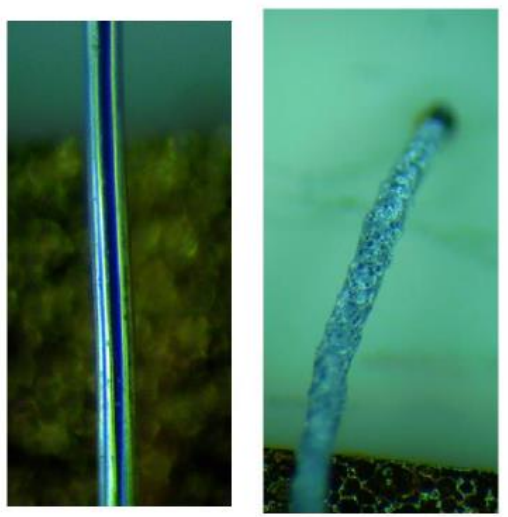
Introduction

What is Electromigration (EM) ?

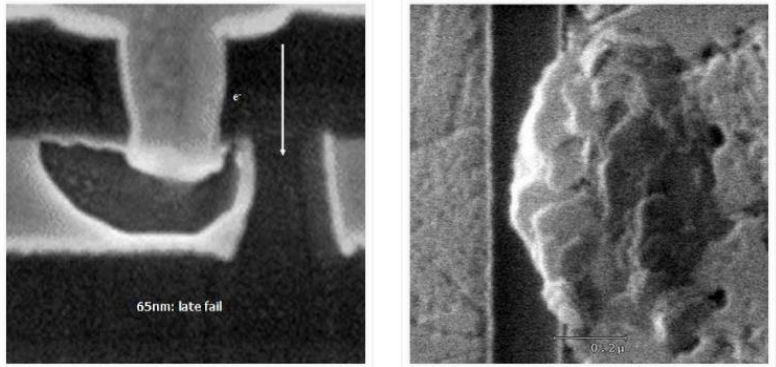
- A material migration based on the flow of current through it
- A diffusion-controlled process.
- Accelerated by:
  - High current density
  - High temperature

Why EM is a concern in Power Modules ?

- Recent trend toward high power density
  - Increasing current density and temperature
- Reliability of the interconnects: Wire bonds, solder bumps
  - Void formation: Open circuit
  - Hillock formation: Short circuit



Before After



void formation Short ckt formation

EM impact on interconnects

EM Risk Assessment Modeling Approaches

❑ Analytical & Experimental

- combined effect of high current and high temperature on Ag, Cu, and Au wire bonds [1]
- An electrical-thermal-mechanical coupled EM analysis in a bonding wire of a power module [2]
- Current density variation impact on wire bond resistance and die attach solder [3]
- Optimizing solder bump structure through solder bump parametric variation in [4]
  - Solder material
  - Solder bump diameter/pitch
  - Geometry
- Solder bump distribution orientation variation for optimization [5]

All efforts are based on manual parameterization and experimental studies

[1] P. Lall et. al., "Study of Electromigration in Cu and Ag Wirebonds Operating at High Current in Extreme Environments," in IEEE iTherm, 2017
[2] M. Kato et al., "Electromigration Analysis of Power Modules by Electrical-Thermal-Mechanical Coupled Model," in ASME IMECE, Nov. 2019.
[3] H. Luo et al., "Study of Current Density Influence on Bond Wire Degradation Rate in SiC MOSFET Modules," IEEE JESTPE, 2020.
[4] M. Montazeri et al., "Vertically Stacked, Flip-Chip Wide Bandgap MOSFET Co-Optimized for Reliability and Switching Performance," IEEE JESTPE, 2021.
[5] C. Hau-Riege and Y. Yau, "Electromigration Reliability of Solder Balls," in IEEE IPFA, 2018

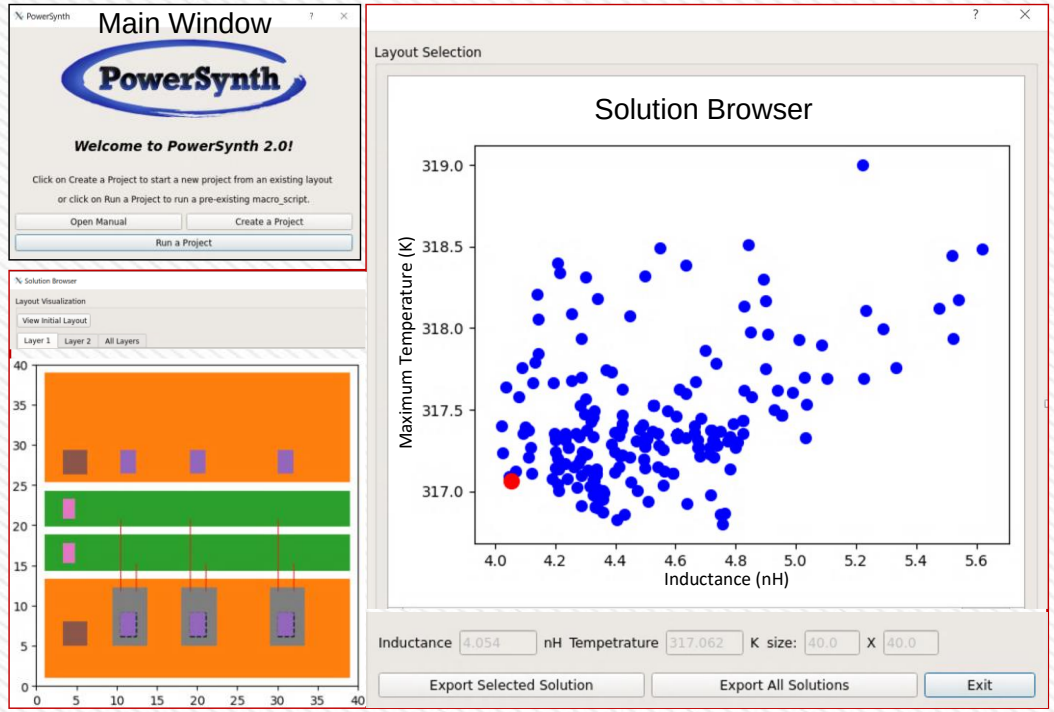
Motivations & Contributions

❑ Motivations

- No design automation effort for EM assessment
- High density power module optimization requires EM-aware reliability optimization
- Need EDA tools for EM-aware layout optimization
- Our solution: EM-Aware PowerSynth 2 [1]

❑ Contributions

- Current density distribution for DC and AC
- A generic EM-aware risk assessment workflow
  - Analytical
  - Data-Driven



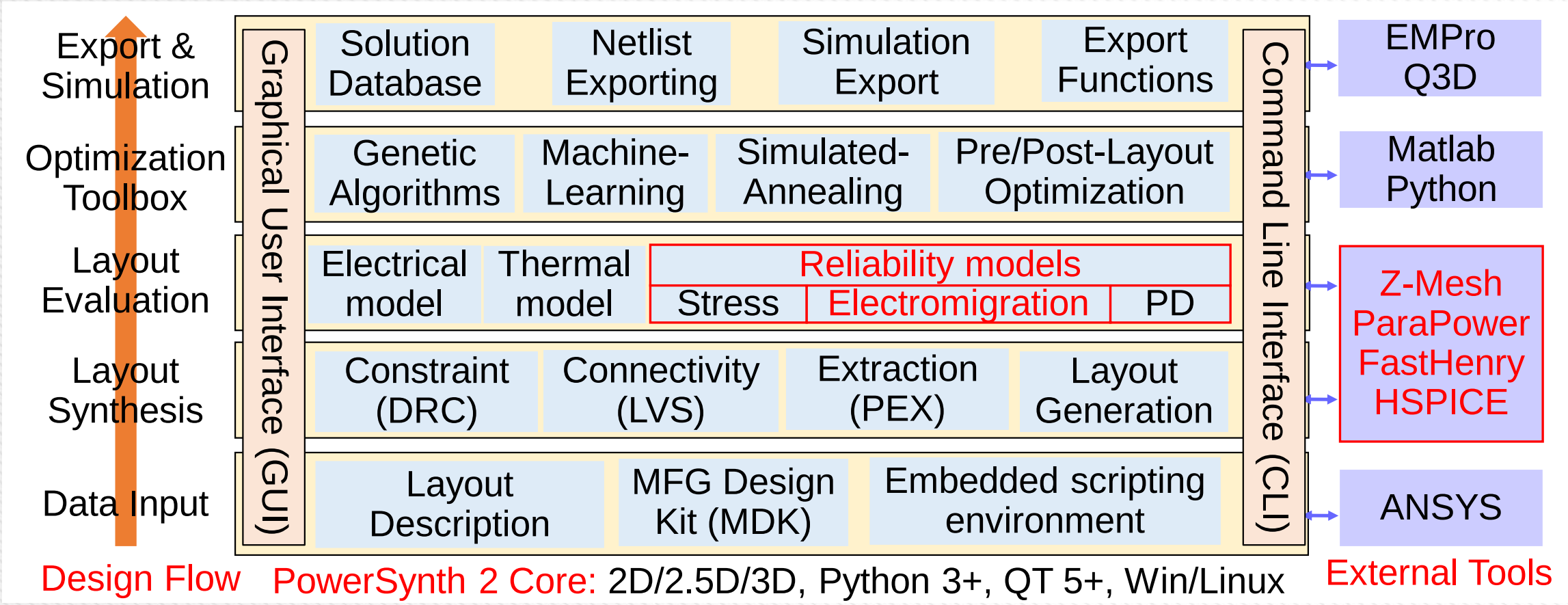
PowerSynth 2 GUI

- Case studies demonstration: Power module with solder bumps and wire bonds
- EM-aware electro-thermal optimization using PowerSynth 2

[1] I. Al Razi et. al., "Hierarchical Layout Synthesis and Optimization Framework for High-Density Power Module Design Automation," ICCAD, 2021.

PowerSynth 2

❑ Architecture



[1] PowerSynth Release Website: https://e3da.csce.uark.edu/release/PowerSynth/

Reliability Optimization Using PowerSynth

- **PowerSynth 2 allows:**
  - **Integration external modeling efforts/tools through APIs**
    - ParaPower: Army Research Lab (ARL) developed thermal and stress evaluation tool
  - **Handling both types of interconnects (i.e., wire bonds and solder joints)**
  - **Considering arbitrary layer stack**
  - **Material library modification**
- **To perform reliability optimization, it requires efficient, and accurate models**
- **Currently, MCPM layouts can be optimized for two major reliability threats:**
  - **Thermal cycling impact minimization [1]**
    - Transient thermal model for 2D MCPM layouts
    - Phase change material (PCM) consideration
  - **Electromigration associated risk assessment**
    - Current density modeling through Z-Mesh tool

[1] Imam Al Razi, David Huitink, and Yarui Peng, "PowerSynth-Guided Reliability Optimization of Multi-Chip Power Module", APEC, 2021.
[2] ARL ParaPower, "https://github.com/USArmyResearchLab/ParaPower".

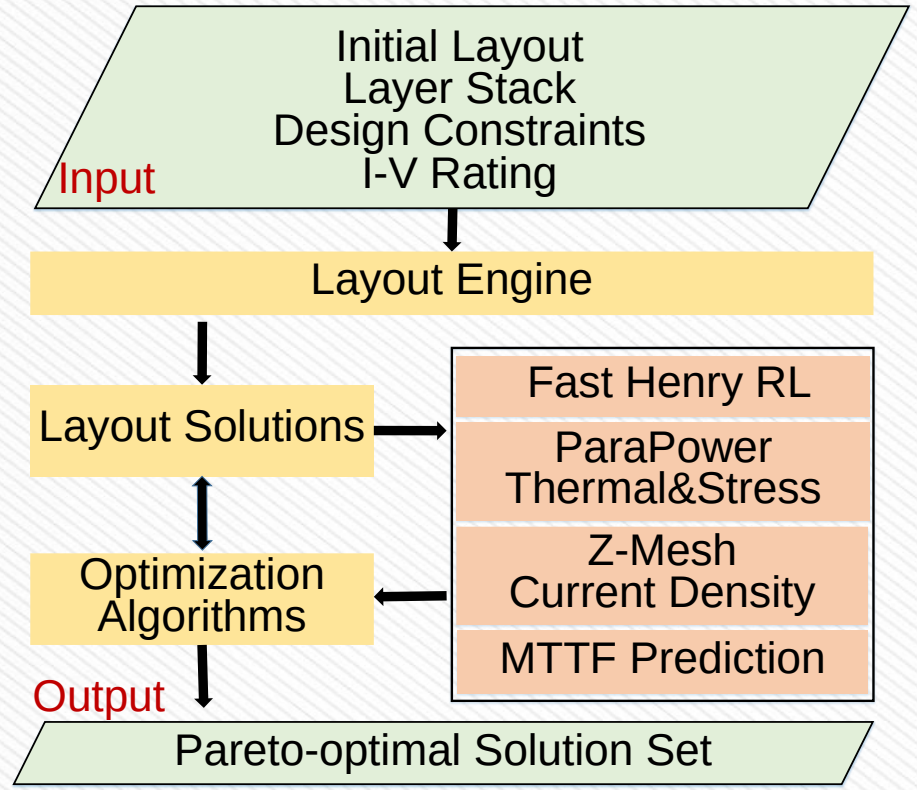
EM-Aware Reliability Optimization

Objectives:

- Quick assessment of risks associated with electro migration (EM) and mechanical failure of interconnects.
- Optimize power module layout to reduce the risk of failure of interconnect.

Methodology

- Features to be considered:
  - Layout generation capability with different interconnects
  - Fast and accurate model for current density estimation through interconnects.
  - Fast and accurate model for temperature and stress distribution



Optimization workflow

Implementation Using PowerSynth 2

❑ Implementation using PowerSynth 2 APIs:

❑ Mean Time To Failure (MTTF) Calculation :

- **Closed-formula approach (Black's Equation for Electromigration)**

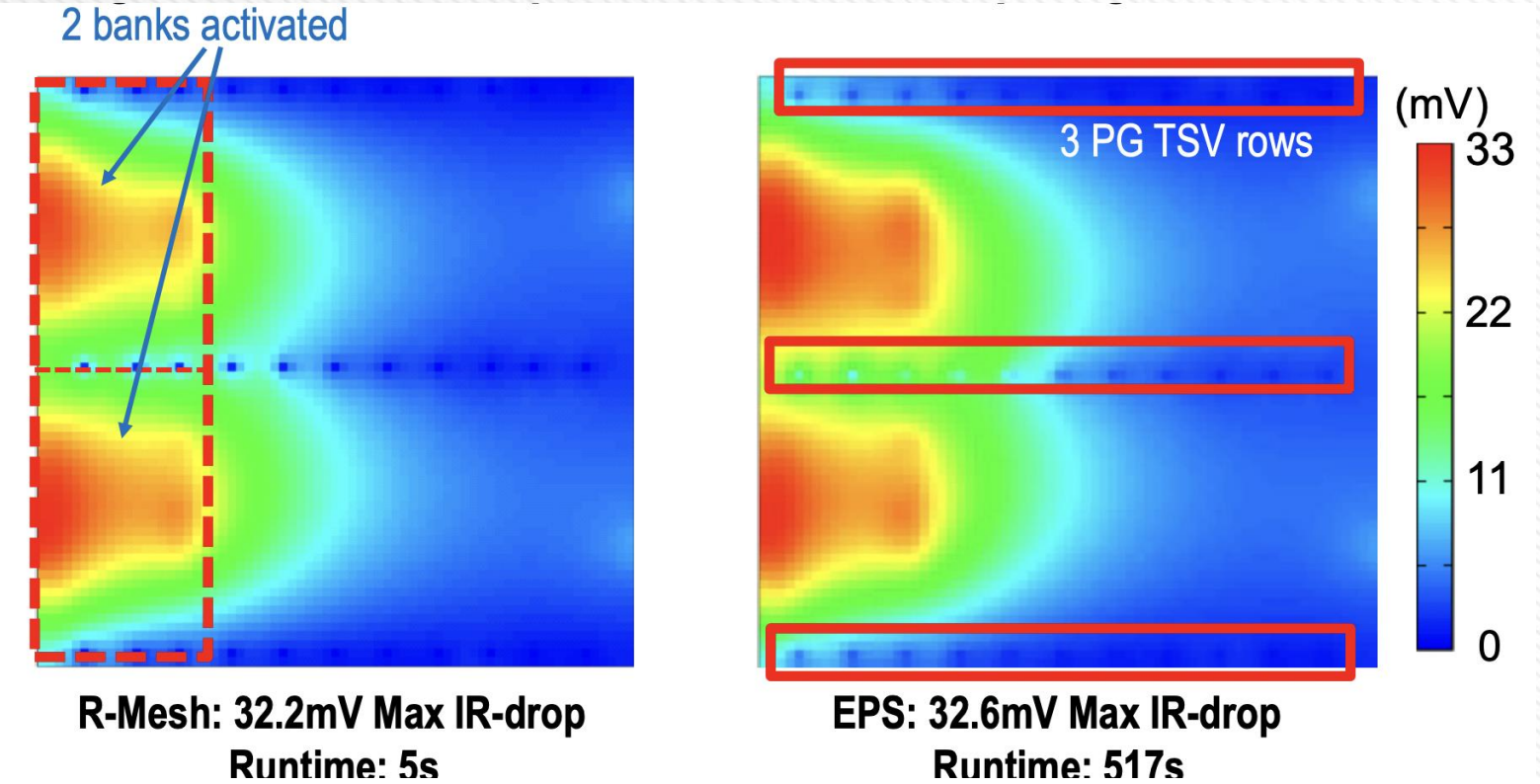
$$MTTF = \frac{A}{j^2} e^{\frac{E_a}{kT}}$$

  - where, A = constant, j = current density, E_a = Activation energy, T= Temperature

- **Data-Driven Model**
  - Look-up table from experimental results
  - Parameter tuning on analytical models from experimental results

Zmesh Current Density Model

- **Zmesh model is derived based on a fast-and-accurate resistive mesh network modeling Rmesh tool, first developed to model IR-drop in 3D DRAM**
  - Validated against Cadence EPS with 103x runtime speed up using a DDR3 layout
  - Extended to cover both DC and AC frequency for power electronics useage

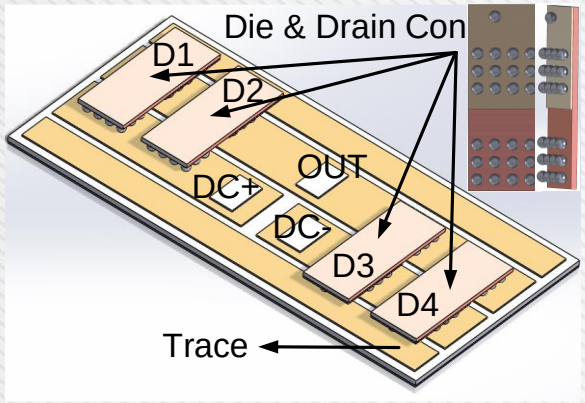


[1] Yarui Peng et al., "Design, Packaging, and Architectural Policy Co-Optimization for DC Power Integrity in 3D DRAM", in Proc. Design Automation Conference, pp. 1–6, Jun 2015.

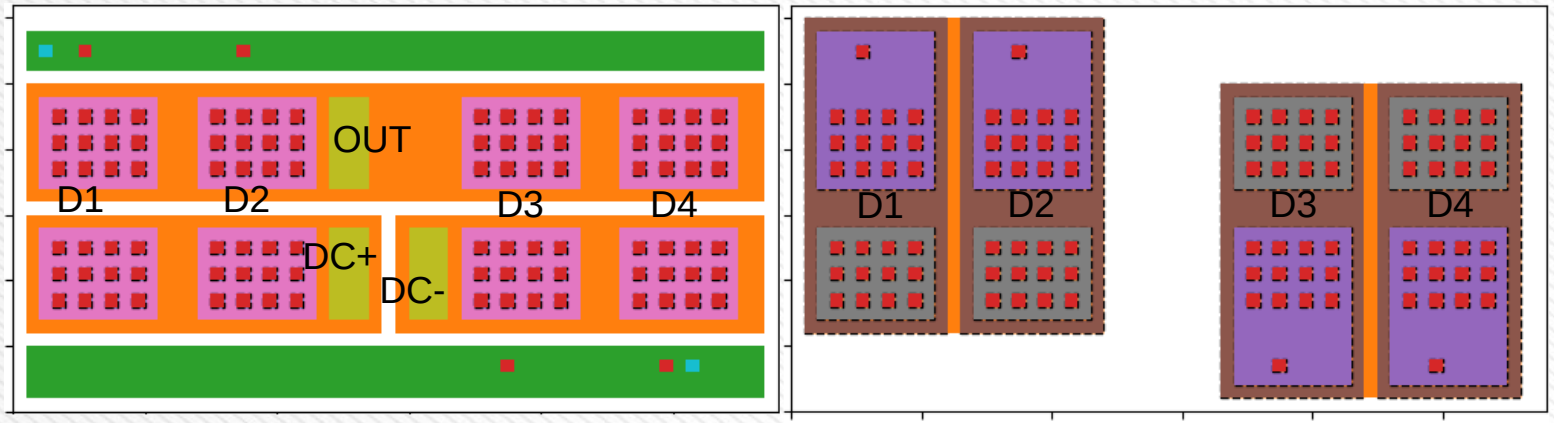
Case Study I

❑ Layout Solution Generation

- **Flip-Chip Design:**
  - Half-bridge module: Two SiC devices/switching position
  - Source side is directly bonded
  - Drain side is extended through metallic connector and bonded with solder balls.



Initial Layout



Minimum-sized Layout (58 mm×31 mm)

❑ Current Density: Z-Mesh tool

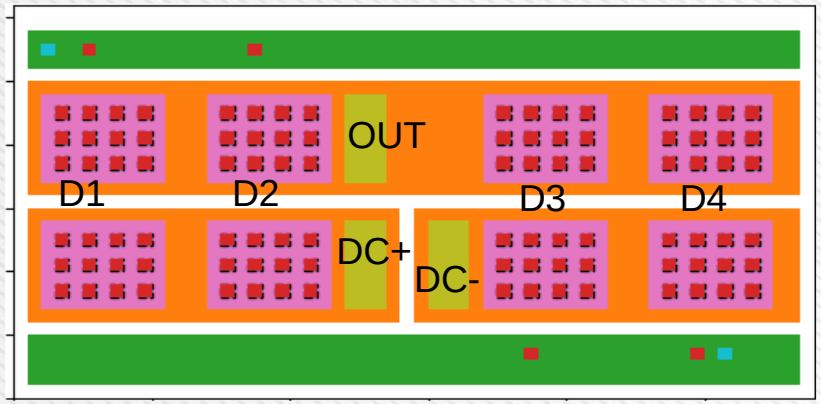
❑ Temperature Distribution: ParaPower

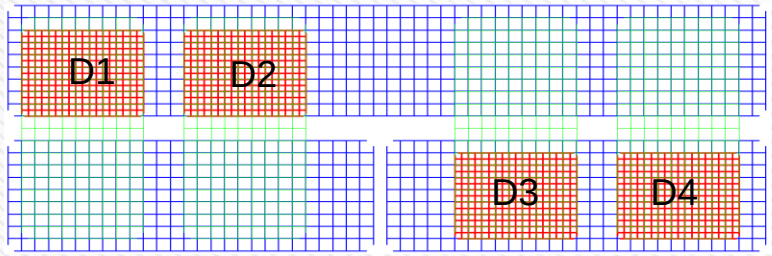
Z-Mesh Modeling

❑ Workflow

Layout Geometry
Supply V/I Rating
Mesh Size

→ Perform Meshing → Create Impedance Network Netlist → HSPICE Simulation → Current Density Results





Z-mesh (power loop only)

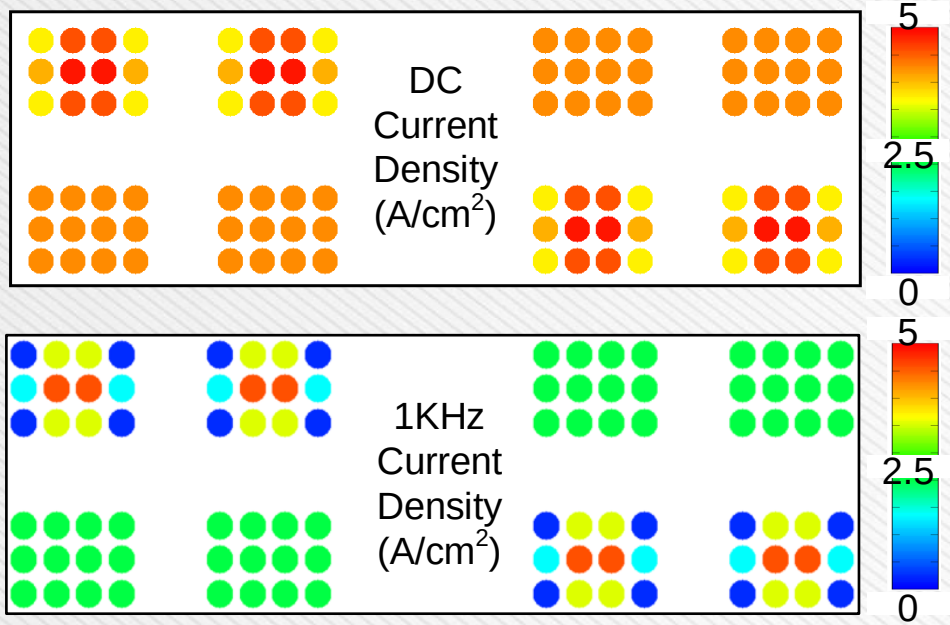
❑ Performance Comparison

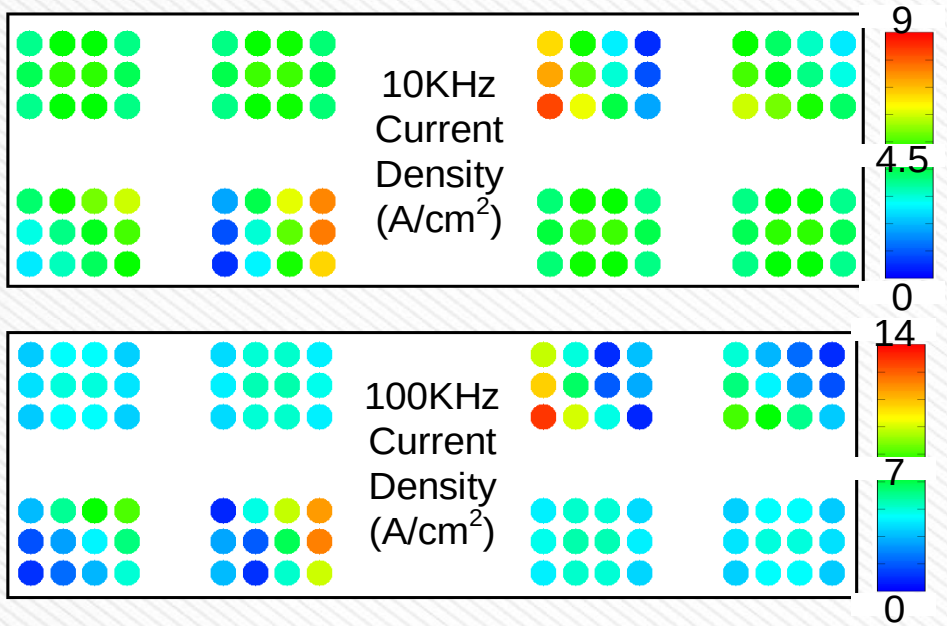
Model	Runtime (s)	Speedup	Memory (MB)	Memory Reduction
ANSYS	310	×1	10329	×1
Z-Mesh	0.28	×1107	513	×20

Current Density Results

❑ Frequency Dependent Current Density

- At DC, intra-die current density variation is observed
- Frequency increases → loop impedance increases → inter-die current density variation increases
  - Solder joints close to the DC+ and DC- : Higher current density
  - Solder joints away from the DC+ and DC- : Lower current density





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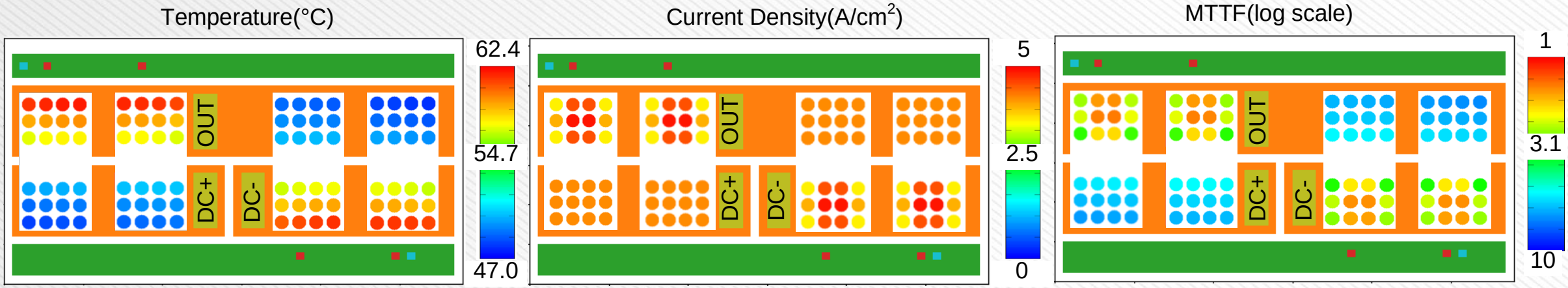
MTTF Results

❑ MTTF Evaluation: DC

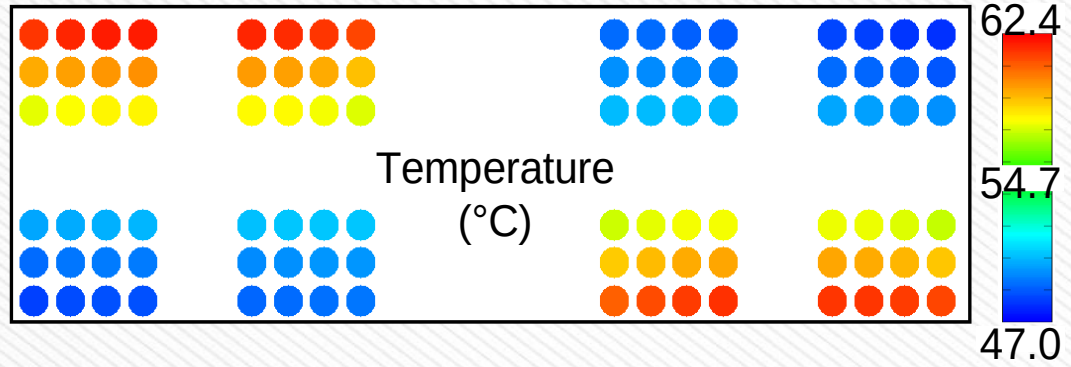
- **Inter-die current density negligible**
- **Temperature is dominant**
  - Hot spots: source-side solder bumps
- **MTTF:**
  - Lower: source-side solder bumps



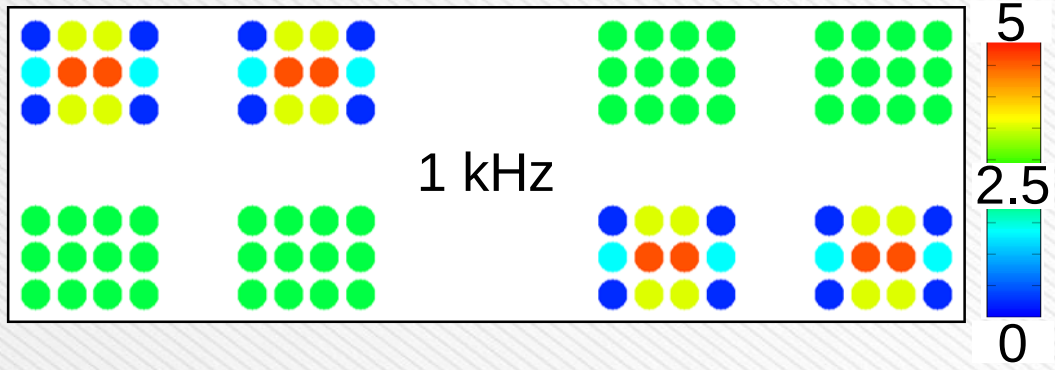
MTTF Results

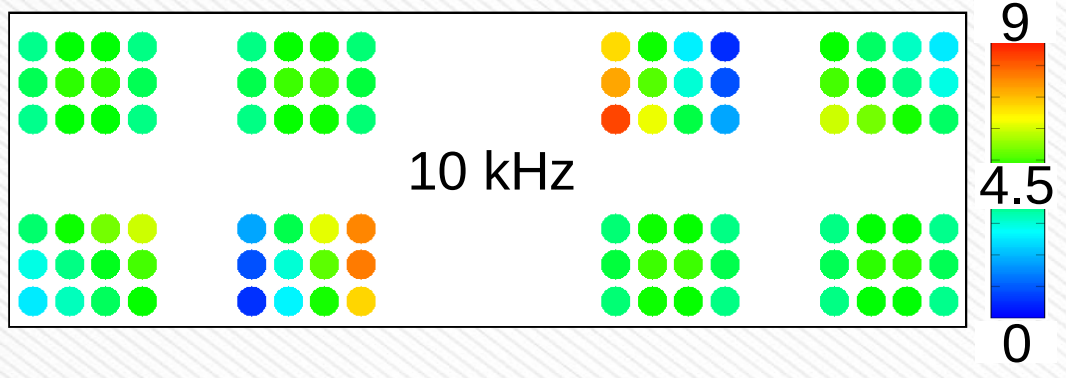
❑ MTTF Evaluation: AC

- Critical: current density and temperature
- Frequency increases→ current density impact increases

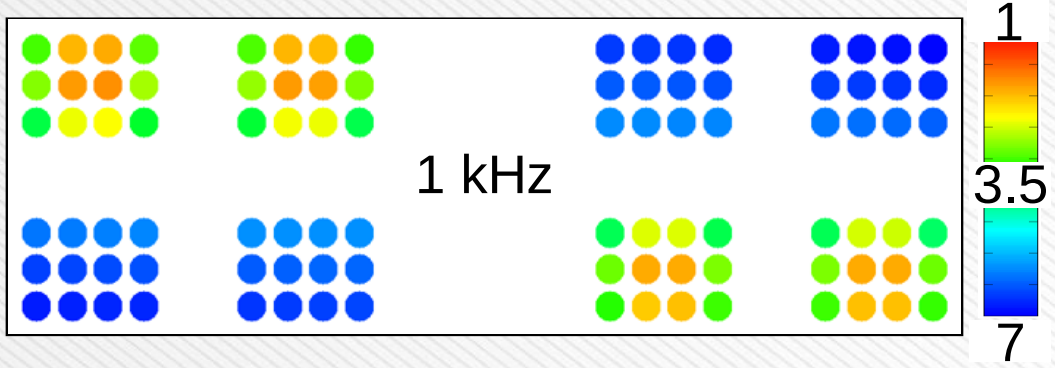


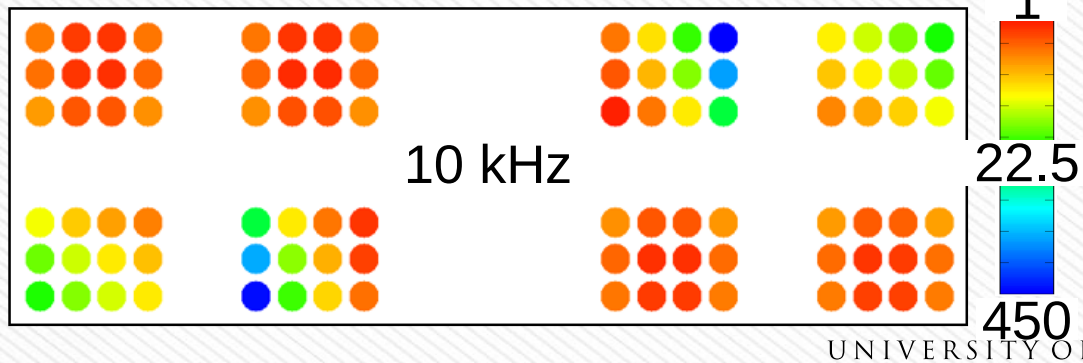
Current Density
(A/cm²)





MTTF
(log scale)





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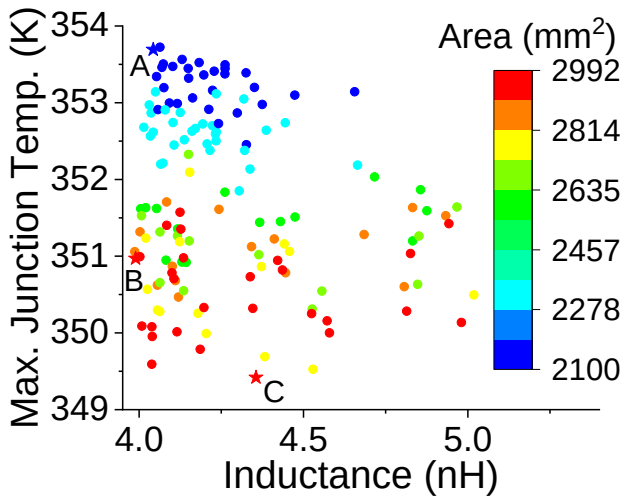
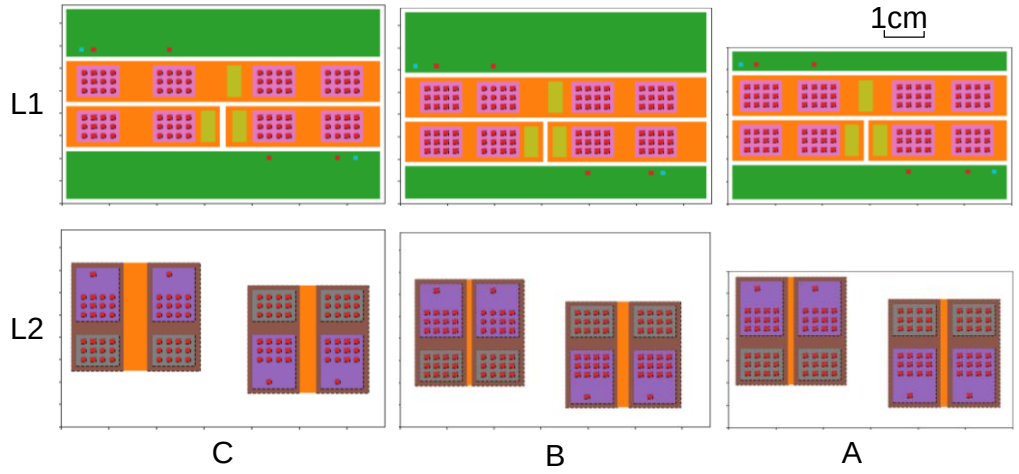
Optimization Results

❑ Approach 1: Floorplan area variation

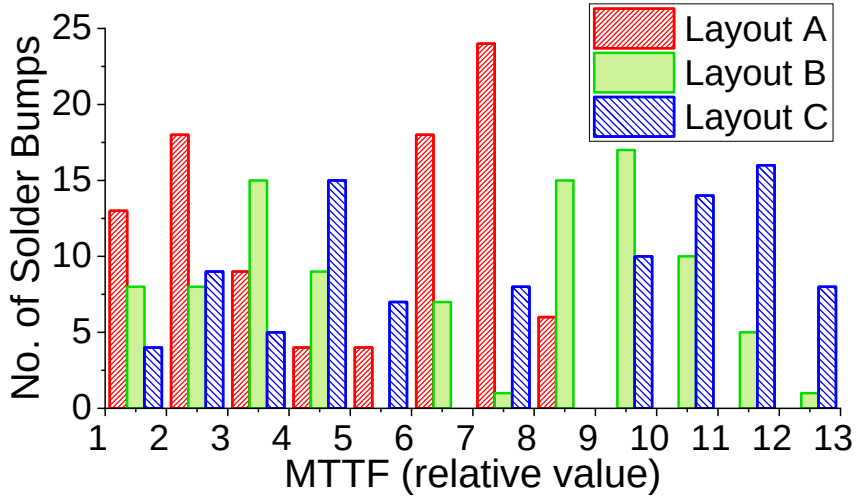
- 10 floorplan sizes : 15 solutions/size (135 s/ layout solution)
- L: FastHenry, T: ParaPower, J: Z-Mesh tool.
- MTTF evaluation at DC
  - Layout A: Highest temperature rise → lower MTTF
  - Layout C: Lowest temperature rise → Higher MTTF
  - Layout B: Balanced solution



Solution space



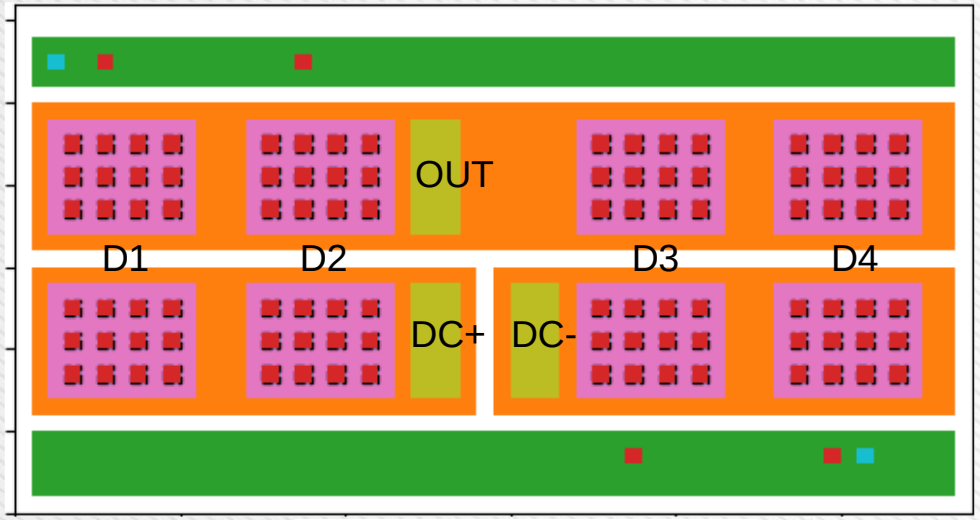
Three layouts



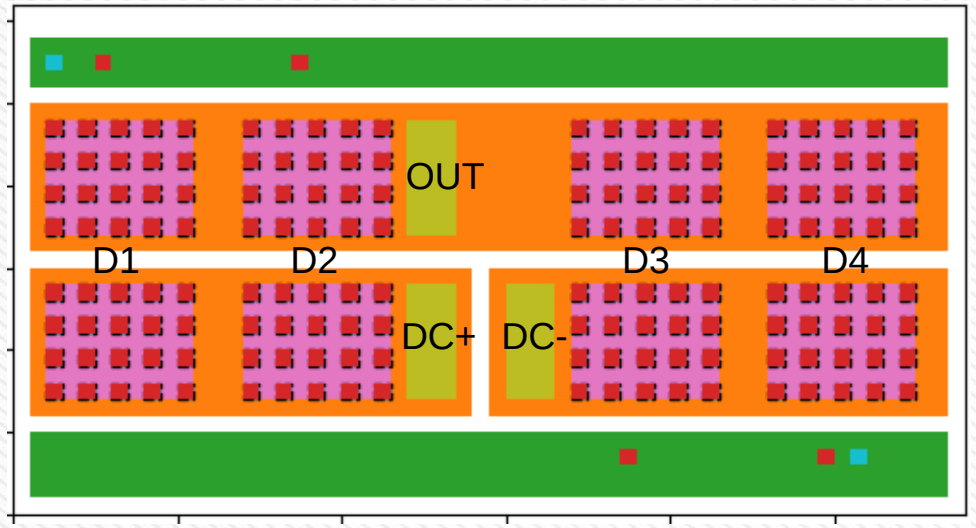
MTTF distribution of three layouts

Optimization Results

- **Approach 2: Fixed floorplan # of solder ball variation**
  - Minimum-sized solution: 58 mm × 31 mm
  - Larger array size → more even current distribution → less density



Case 1: 4 × 3 Array

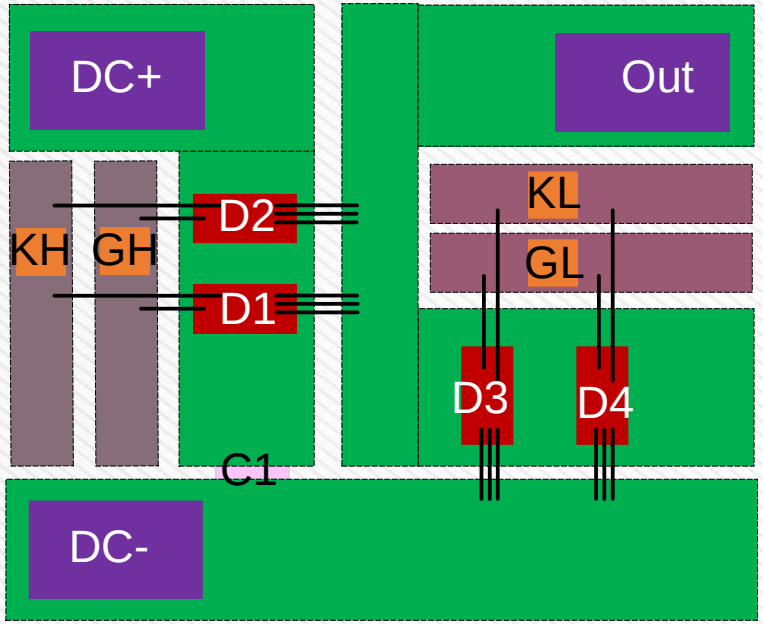


Case 2: 5 × 4 Array

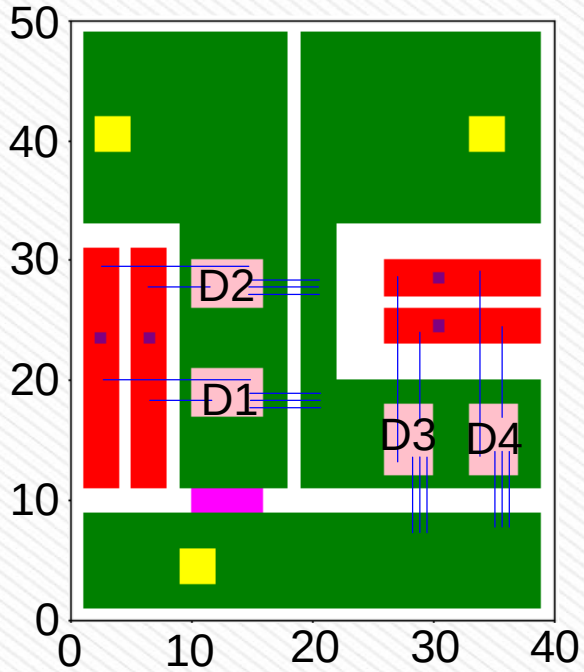
Case	Solder Array	Max J (A/cm^2)	Max Temp. (ºC)	MTTF	Improvement
1	4 × 3	4.86	62.43	1.19	×1
2	5 × 4	3.13	62.34	2.89	×2.4

Case Study II

- **Layout Solution Generation**
- **Wire-bonded 2D module:**
  - Half-bridge module: Two SiC devices/switching position
  - Three 5-mil Al wirebonds/device
  - Embedded decoupling capacitor (C)
  - Hardware validated parasitic extraction result
  - Temperature distribution result from ParaPower
- **Current density extraction steps:**



Initial Layout



Optimized Solution (40 mm × 50 mm) [1]

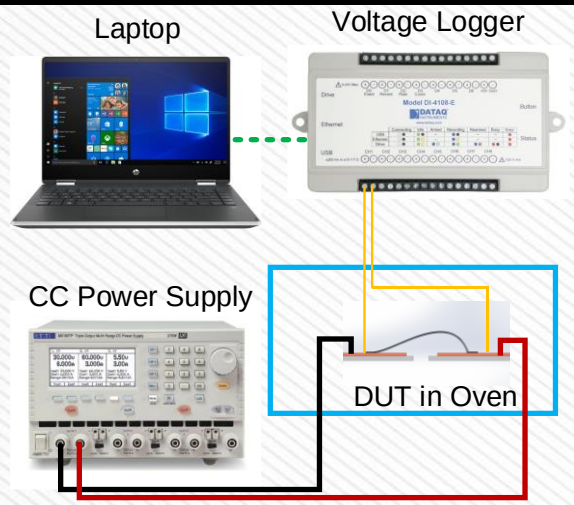
Parasitic Netlist (from PowerSynth) → Circuit Simulation → Current through Each Device/Wire Bond → Current Density of Each Wire Bond

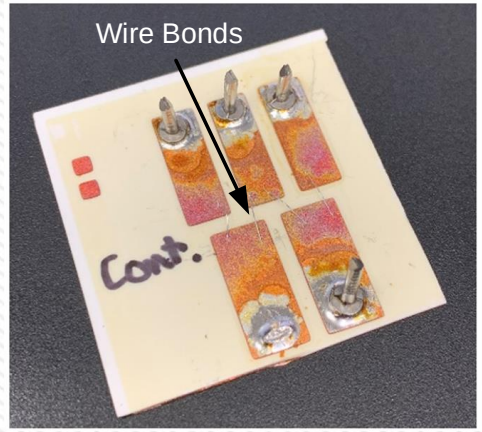
[1] Imam Al Razi et. al., "PowerSynth Design Automation Flow for Hierarchical and Heterogeneous 2.5D Multi-Chip Power Modules", IEEE Transactions on Power Electronics, vol. 36, no. 8, pp. 8919–8933, 2021.

Failure Time Measurement Experiment

❑ Wire Bonds EM Failure Experimental Setup

- Two DBC with four 5-mil Al wirebonds
- Accelerated test setup
  - Elevated ambient temperature using oven
  - Variable current densities
  - DATAQ voltage module
    - Resistance (R) change monitoring
  - Failure criteria: 10% increase in R

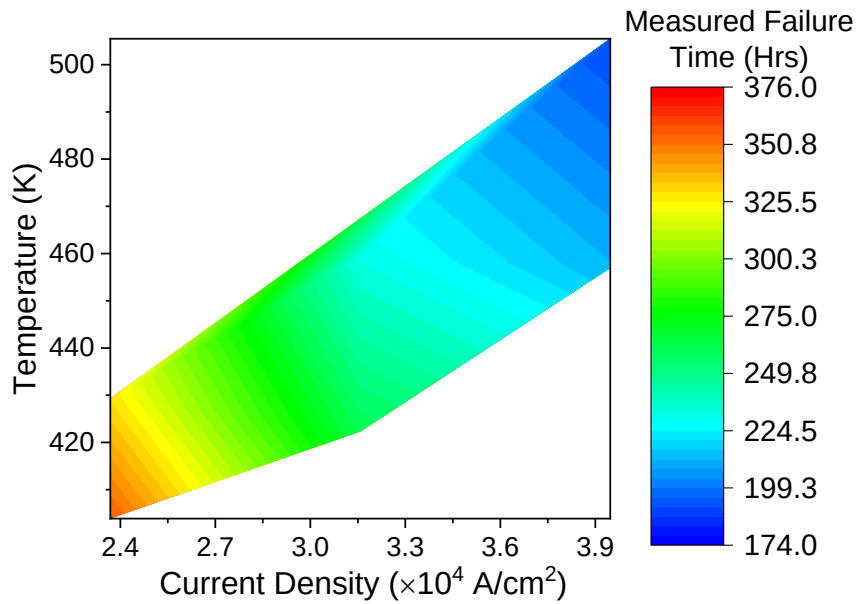




DUT

❑ Results

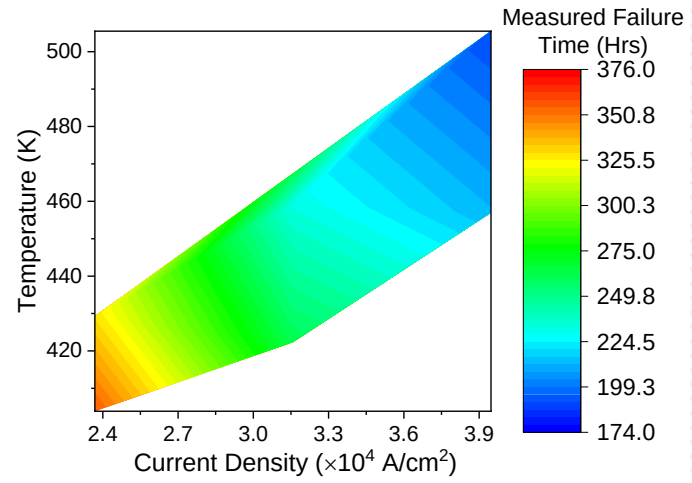
- Contour plot to represent aggregation of
  - the current density through the wire bonds,
  - the temperature of the wire bonds at that current density,
  - the corresponding failure time (color bar)



MTTF Results

Wire-bonded Module

- **Current Density Extraction**
  - Supply current ~ 23 A
- **Temperature**
  - Measurement data from [1]
- **Reliability Metric:**
  - 10% increase in R of the wire bond (from contour plot based on the experimental data)



Device	Current (A)	Temperature (K)	Wire Bond Current Density (A/cm²)	EM Failure Time (Hr)
D1	11.53	416.8	3.03×10^4	217.4
D2	11.26	416.5	2.95×10^4	229.6
D3	11.55	427.0	3.03×10^4	210.8
D4	11.24	427.7	2.95×10^4	221.9

[1] Imam Al Razi et. al., “PowerSynth Design Automation Flow for Hierarchical and Heterogeneous 2.5D Multi-Chip Power Modules”, IEEE Transactions on Power Electronics, vol. 36, no. 8, pp. 8919–8933, 2021.

Conclusions and Future Work

❑ Conclusions:

- EM needs to be considered with multi-physics models and detailed layout
- Integrated fast and accurate models in PowerSynth2 for
  - Current density distribution
  - Temperature distribution
  - EM-aware MTTF estimation
- Both closed-form models and data-driven models are highly accurate with significant runtime improvement over FEM.
- Our EM-aware design automation flow can optimize both flip-chip and wire-bonded MCPM layouts with high accuracy and efficiency

❑ Future Work:

- More accurate current and temperature distribution across the wire bonds
- Incorporating stress impact in the electromigration risk assessment model
- Validate the optimization results through experiments

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