DESIGN METHODOLOGIES FOR POWER ELECTRONICS

UNIVERSITY OF ARKANSAS | College of Engineering | Mixed-Signal Computer Aided Design Research Lab

Paper No: S3P1

# Placement and Routing for Power Module Layout

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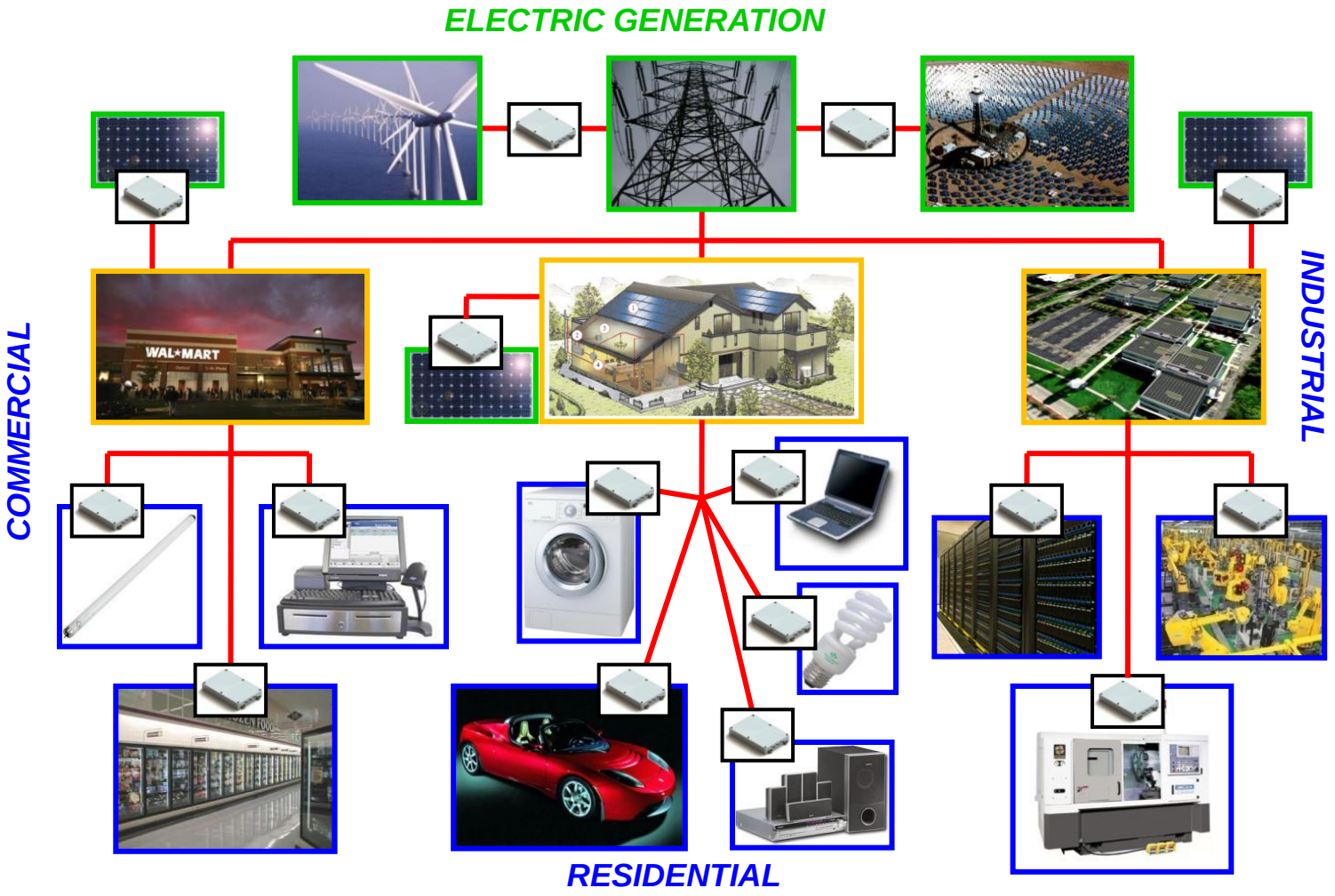
# Outline

- Motivation
- PowerSynth Introduction
  - Overview
  - Improvement
- Placement & Routing for Power Electronics
  - VLSI Inspiration
  - Force-Directed Placement
  - Grid-Based Routing
- Initial Results
- Conclusions and Future Work

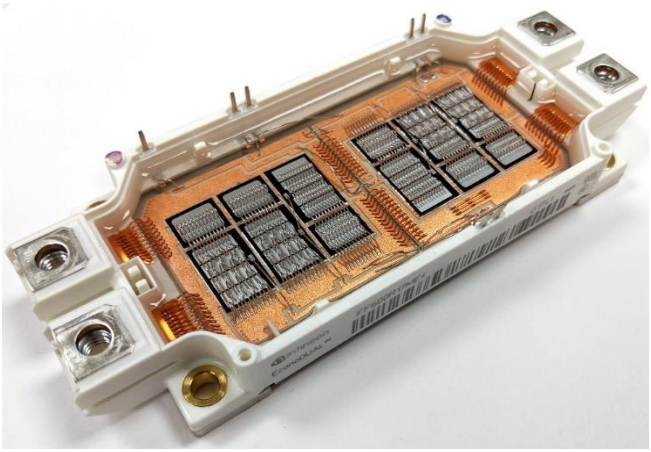
# Power Electronics is Everywhere



# MCPM Co-Design Challenges

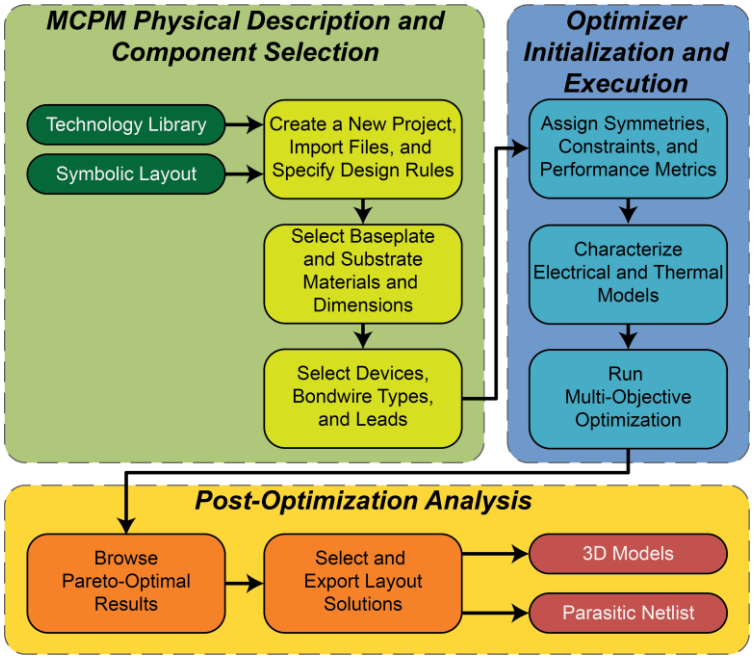
**Physical design of multi-chip power modules (MCPM) is time consuming and poses several challenges:**

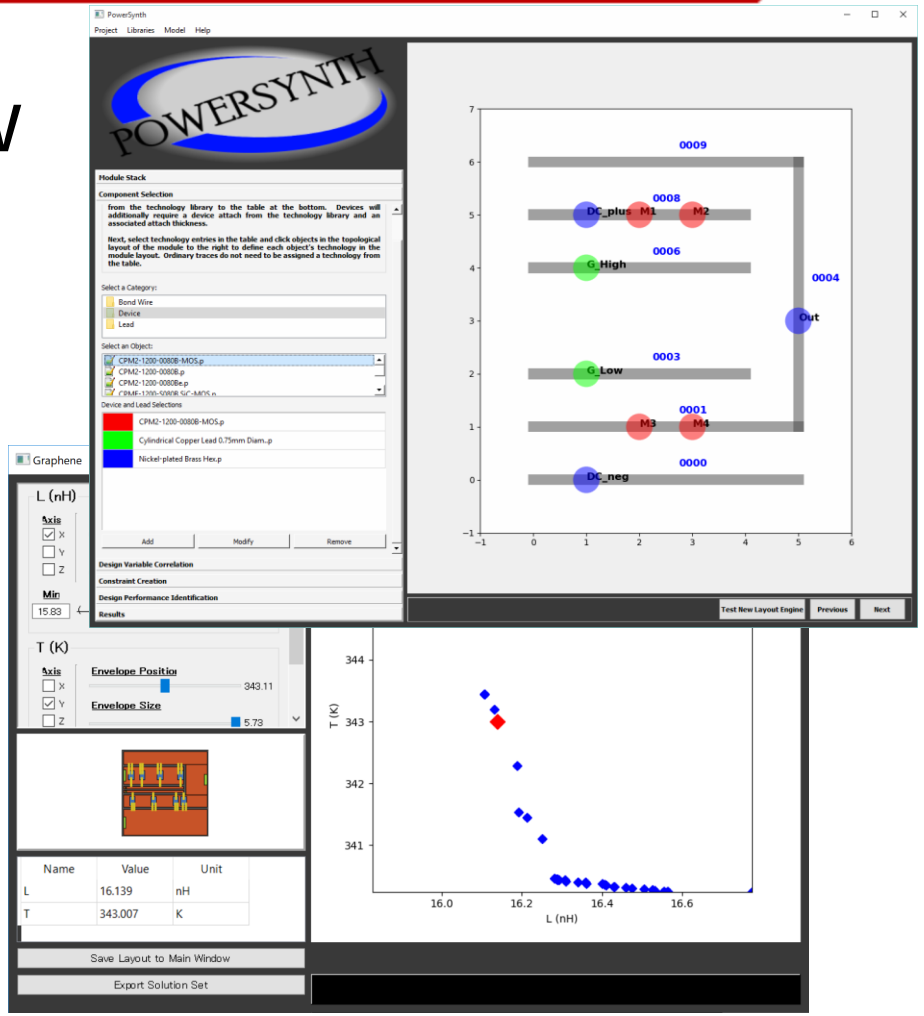
- Multi-domain nature of power electronic packaging necessitates consideration of materials and designs towards reduced:
  - Electrical parasitics for high performance devices
  - Temperature and mechanical stress for higher reliability
- Traditional design flows are iterative and require extensive use of computationally expensive finite element analysis (FEA)



# PowerSynth Overview

- EDA tool for multi-chip power modules (MCPM)
- Multi-objective layout optimization
- Reduced order models
- Pareto-front of tradeoffs
- Design export




Tristan M. Evans, Quang Le, Shilpi Mukherjee, Imam Al Razi, Tom Vrotsos, Yarui Peng, H. Alan Mantooth , "PowerSynth: A Power Module Layout Generation Tool," in *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5063-5078, June 2019. doi: 10.1109/TPEL.2018.2870346 **Highlighted Paper**

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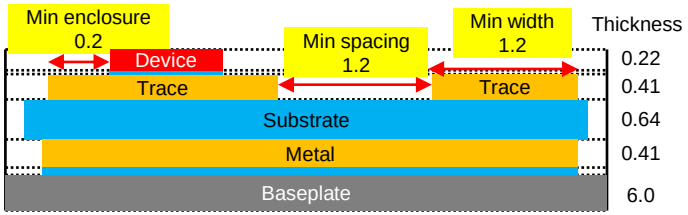
# PowerSynth Manufacturer Design Kit (MDK) and Technology Library

## Layer Stack

- Input file describing layers and technologies
- Holds information pertaining to
  - Layer width, length, and thickness
  - Layer material properties




**MCPM layer stack**

## MDK and Design Rules and Checker (DRC)

- Input file containing technology-dependent design and processing rules
- Ensures feature sizing and component placement are within processing tolerance

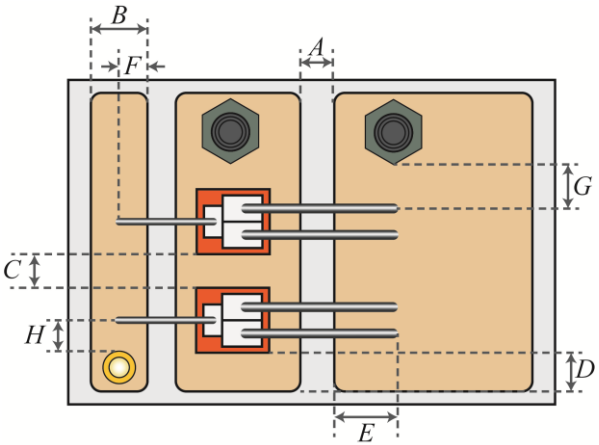
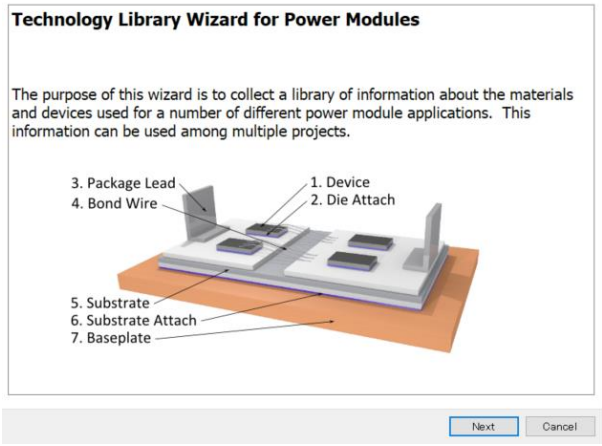


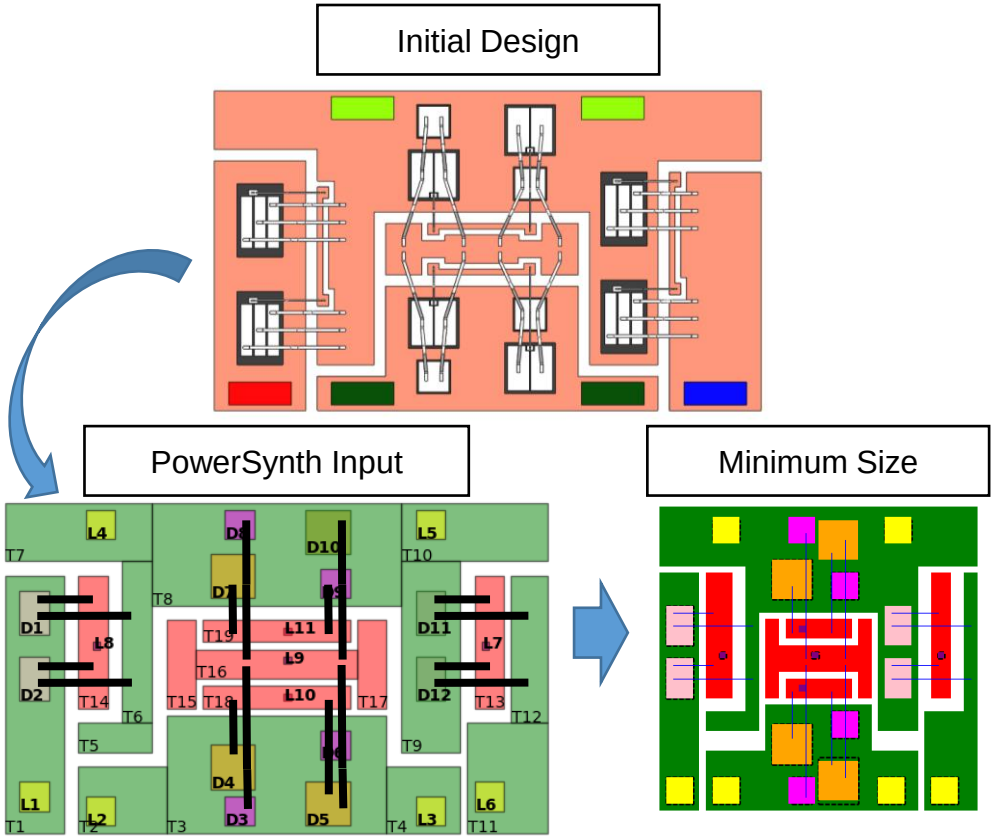

**Illustration of design rules pertaining to feature placement and minimum spacing**




**PowerSynth technology library wizard**

# PowerSynth Layout Engine

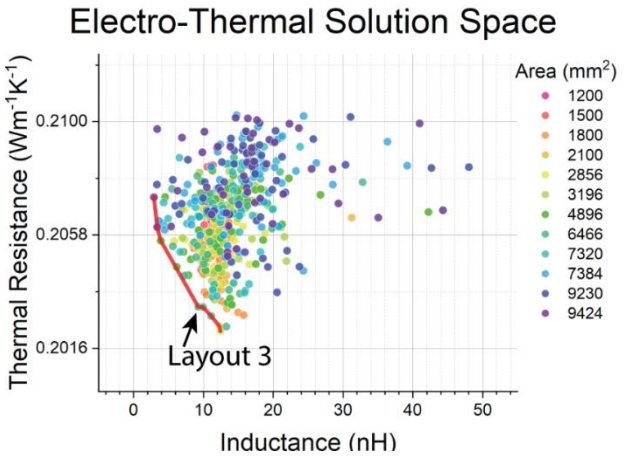
- Constraint aware, hierarchical layout engine
- Minimum trace gaps set by trace-to-trace potential difference
- Heterogeneous component support
- Fixed or minimum layout size capabilities



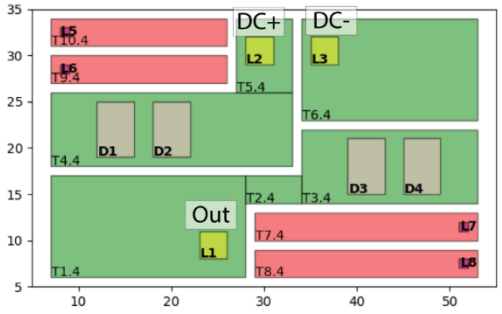

I. Al Razi, Q. Le, H. A. Mantooth, and Y. Peng, "Constraint-Aware Algorithms for Heterogeneous Power Module Layout Synthesis and Reliability Optimization." in *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2018, pp. 323-330.

# Co-Design Example (1/2)

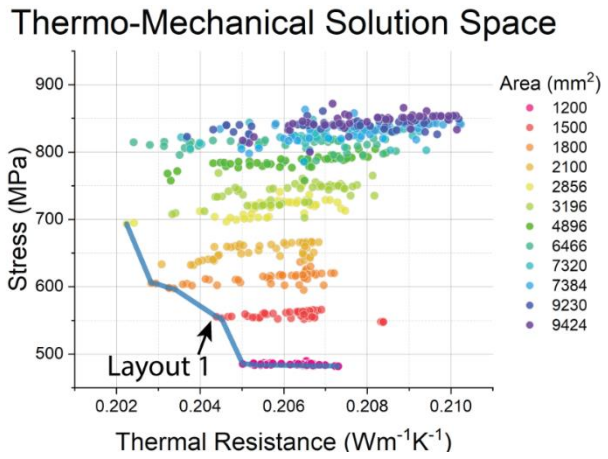
- Half bridge layout
- Loop inductance from DC+ to DC-
- 10 W power dissipation/die, 25℃ backside temperature
- 230℃ process temperature,
- -40℃ minimum ambient temperature

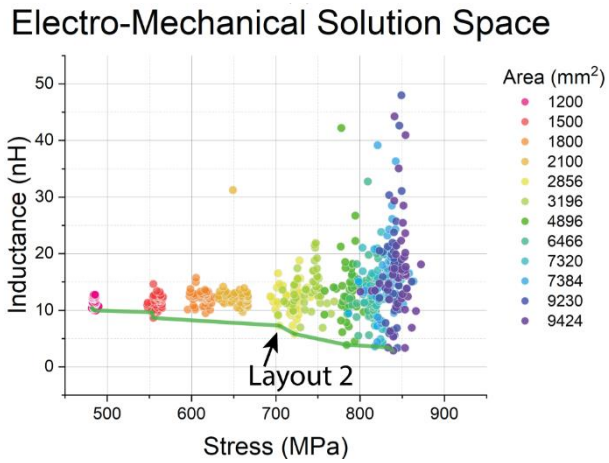



**Pareto frontier results for different solution spaces**



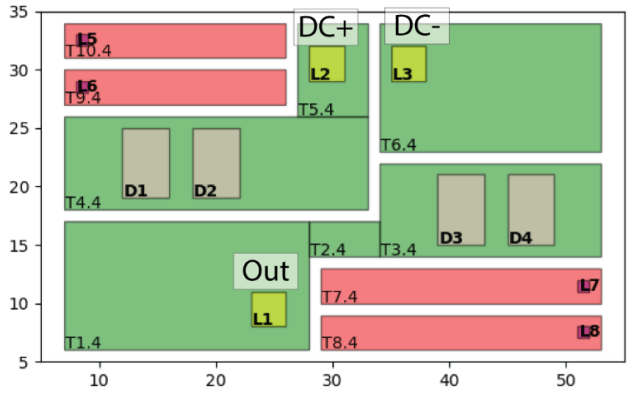

Initial Layout



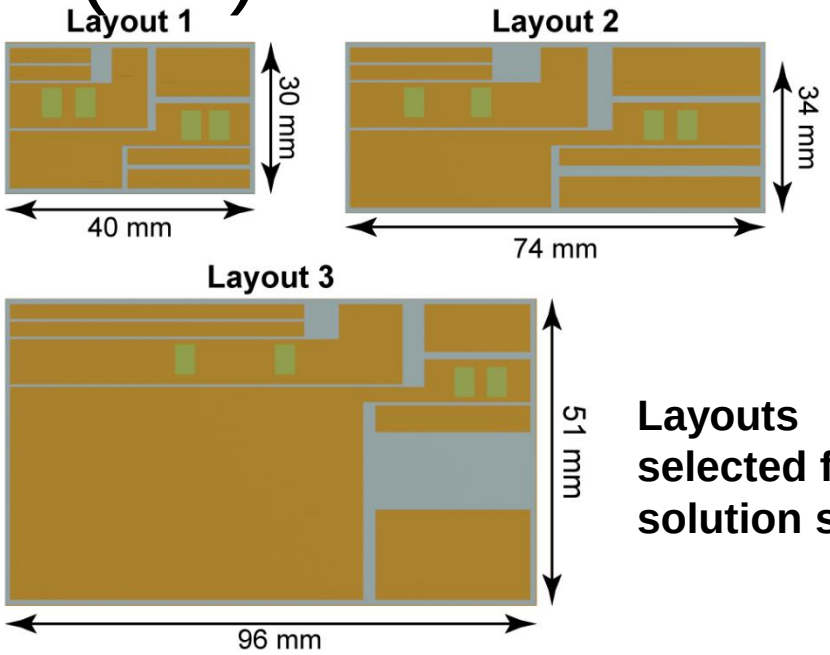




Tristan Evans, Shilpi Mukherjee, Yarui Peng, and H. Alan Mantooth. “Electronic Design Automation Tools and Considerations for Electro-Thermo-Mechanical Co-Design of High Voltage Power Modules.” In IEEE Energy Conversion Congress and Exposition, 2020.

# Co-Design Example (2/2)




**Initial Layout**




**Layouts selected from solution space**

Need more variation in starting-point layout designs

**Layout performance metrics**

| | Dimensions (mm) | Inductance (nH) | $R_{TH}$ ($Wm^{-1}K^{-1}$) | Stress (MPa) |
|---|---|---|---|---|
| Layout 1 | 40x30 | 9.93 | 0.204 | 556 |
| Layout 2 | 74x34 | 7.23 | 0.206 | 704 |
| Layout 3 | 96x51 | 9.26 | 0.203 | 816 |

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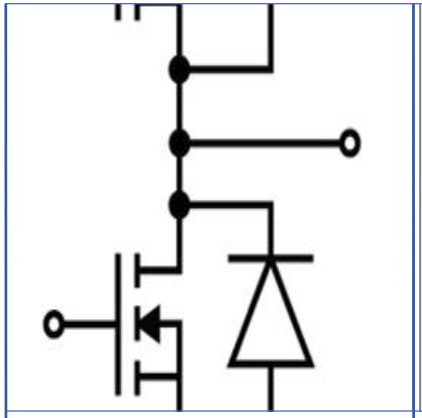
# PowerSynth Layout Synthesis Goals



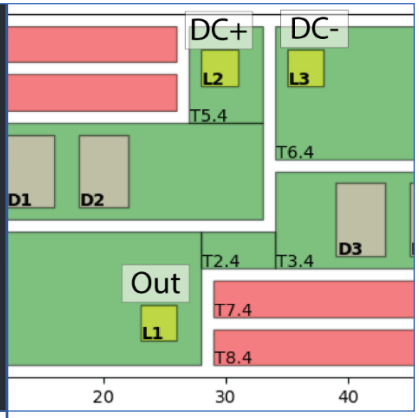
Schematic

```
M3 Out G_Low DC_Neg K_Low NMOS
M4 Out G_Low DC_Neg K_Low NMOS

.model NMOS NMOS
.model PMOS PMOS

*units: mm
*footprint: w=152.0, l=62.0
*terminal: DC_Pos, x=50.67, y=7.75
*terminal: DC_Neg, x=101.33, y=7.75
*terminal: Out, x=76.0, y=54.25
*terminal: G_High, x=25.33, y=31.0
*terminal: K_High, x=12.67, y=31.0
*terminal: G_Low, x=126.67, y=31.0
*terminal: K_Low, x=139.33, y=31.0
```

Netlist

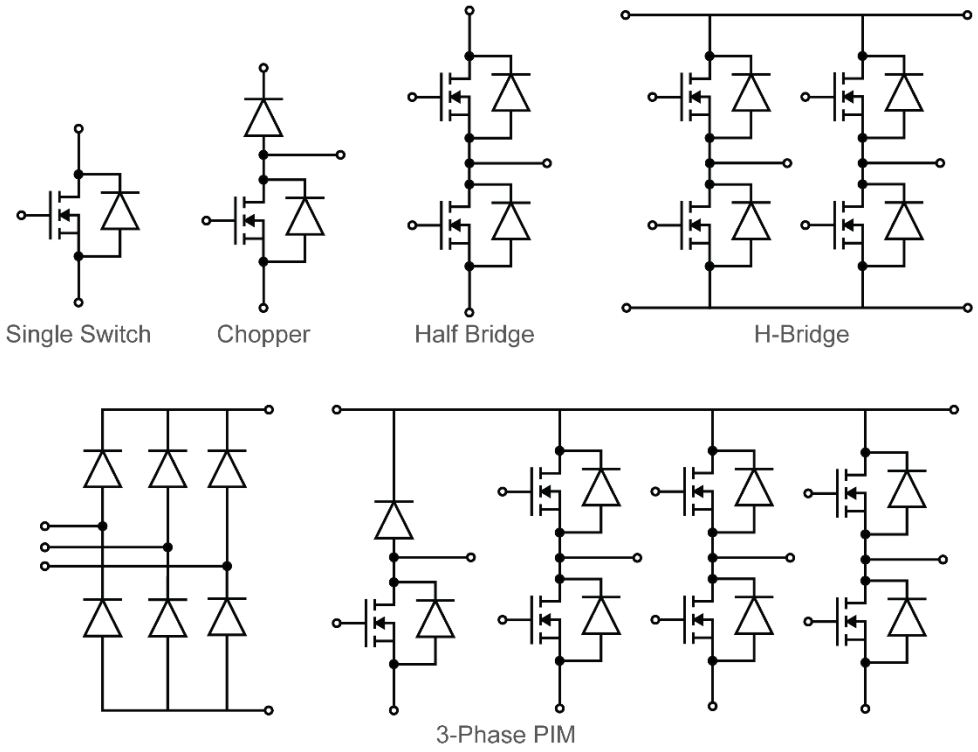
```
# Layout Information
I1 Z+
+ T1 signal 1 1 16 61
  + L1 signal_lead 8 31
+ T2 power 19 1 35 34
- T3 power 19 35 60 27
  + M2 MOS 38 22
  + M3 MOS 50 30
  + M1 MOS 70 45
  + L2 signal_lead 50 54
+ T4 power 59 1 65 29
- T5 power 86 30 38 16
  + L3 signal_lead 75 8
  + M4 MOS 88 20
  + M5 MOS 107 22
  + M6 MOS 93 37
```

Layout Script




PowerSynth Initial Layout

# From Very Large-Scale Integration (VLSI) to Power Electronics (1/3)

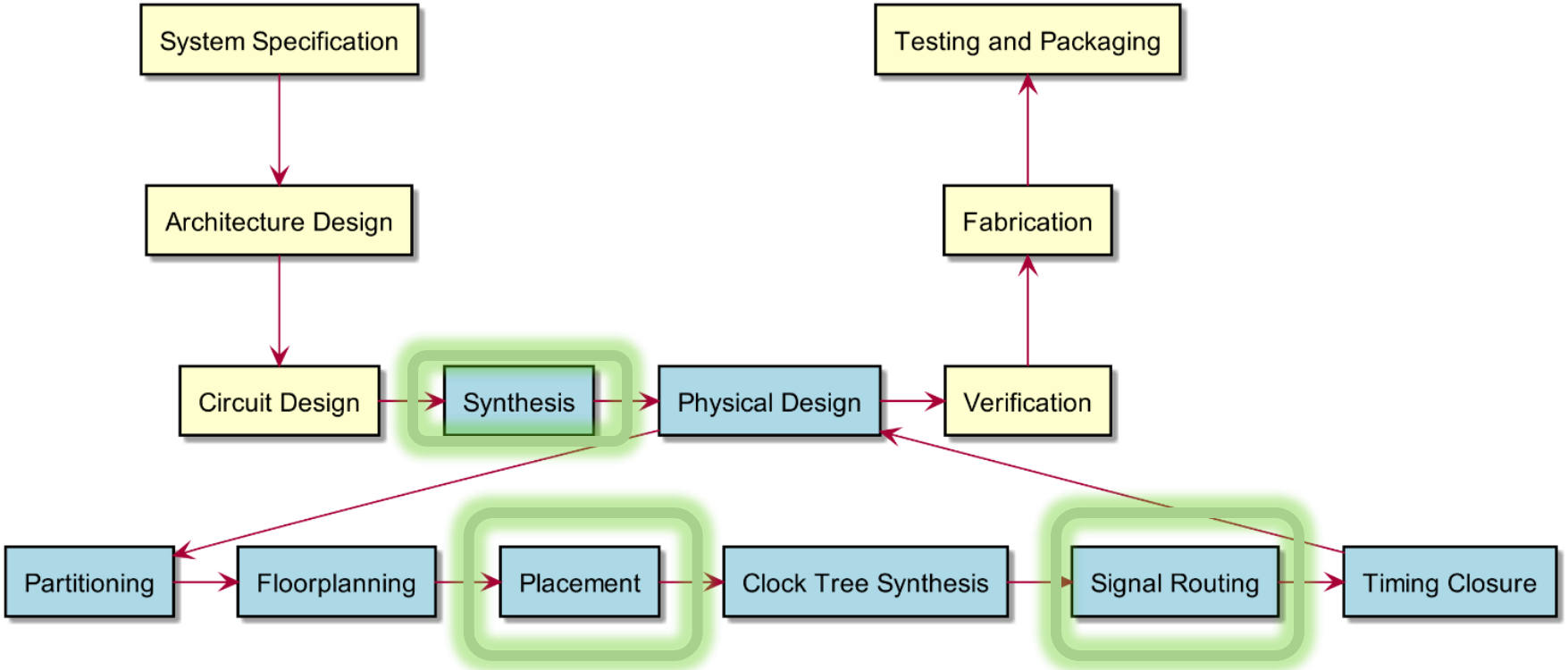



**Typical power module topologies**

## VLSI vs. Power Layout Aspects

| | VLSI Layout | Power Module Layout |
|---|---|---|
| **Component Count** | High (up to billions) | Low (generally <20 ) |
| **Component Dimensions** | Regular | Irregular |
| **Routing Layers** | Multiple | Single, Multiple (gaining traction) |
| **Primary Fitness Metrics** | Footprint, timing delay | Footprint, electrical parasitics, junction temperature, mechanical stress |

# From VLSI to Power Electronics (2/3)

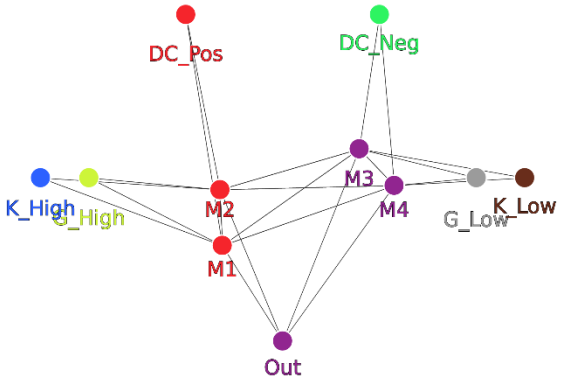


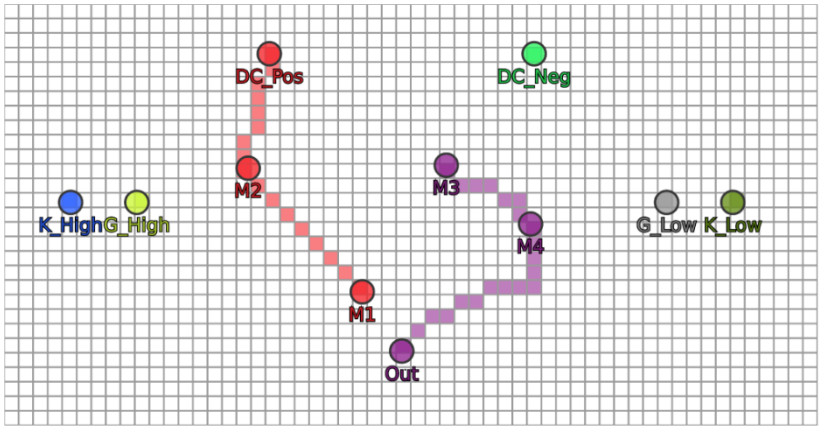

**Typical VLSI design flow**

# From VLSI to Power Electronics (3/3)

- Mature field of VLSI offers numerous techniques and algorithms to draw from
- Two broad topics considered:
  - Placement
  - Routing

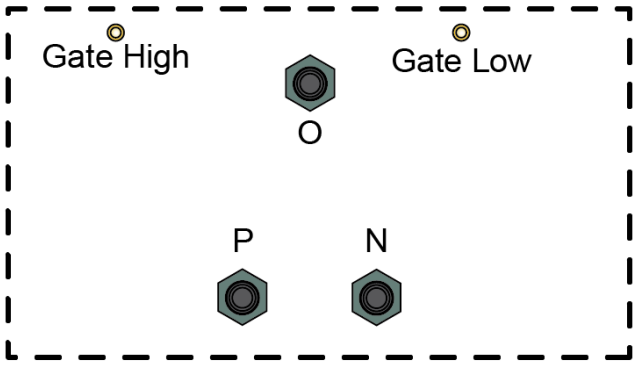
**Expected Outcomes:**
- Reduced design time
- Variation in starting-point layouts
- Expanded solution space



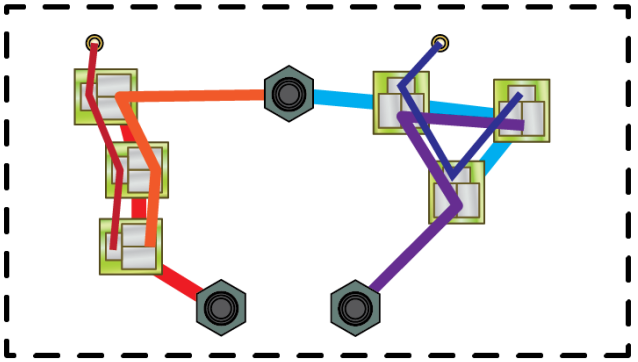



# Power Module Place-and-Route

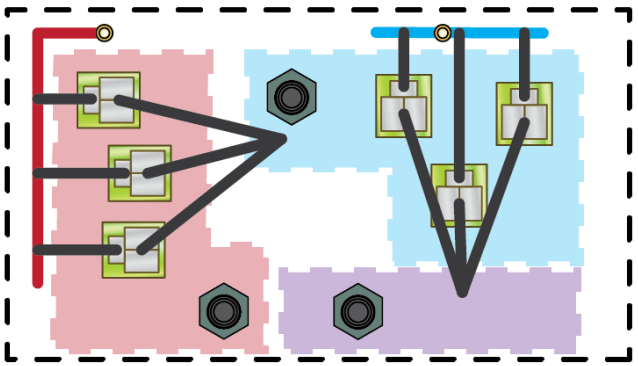
**Step 1: Fix Terminal Locations within Module Bounds**



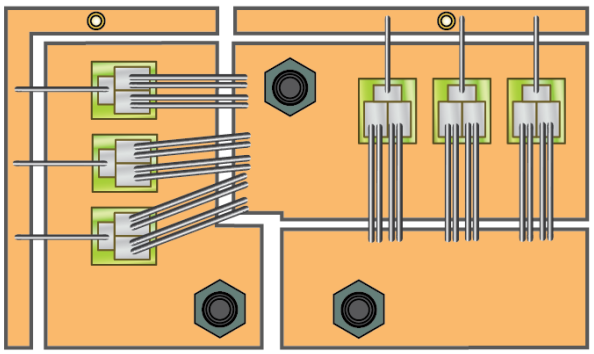

**Step 2: Parse Netlist and Place Devices Relative to Terminals**



**Step 3: Route Traces and Add Wirebone Connection**



**Step 4: Export for PowerSynth Layout Optimization**



# Annotated Netlist Input

- Specification of additional parameters for aiding layout synthesis
- Properties include:
  - Terminal names as nodes with locations specified
  - Overall footprint
  - Units
  - Device Kelvin connection
- Parsed netlist used for placement and routing

```
M1 DC_Pos G_High Out K_High  NMOS
M2 DC_Pos G_High Out K_High NMOS
M3 Out G_Low DC_Neg K_Low NMOS
M4 Out G_Low DC_Neg K_Low NMOS

.model NMOS NMOS
.model PMOS PMOS

*units: mm
*footprint: w=152.0, l=62.0
*terminal: DC_Pos, x=50.67, y=7.75
*terminal: DC_Neg, x=101.33, y=7.75
*terminal: Out, x=76.0, y=54.25
*terminal: G_High, x=25.33, y=31.0
*terminal: K_High, x=12.67, y=31.0
*terminal: G_Low, x=126.67, y=31.0
*terminal: K_Low, x=139.33, y=31.0

.end
```

**Half-bridge annotated netlist example**

# Force-Directed Placement

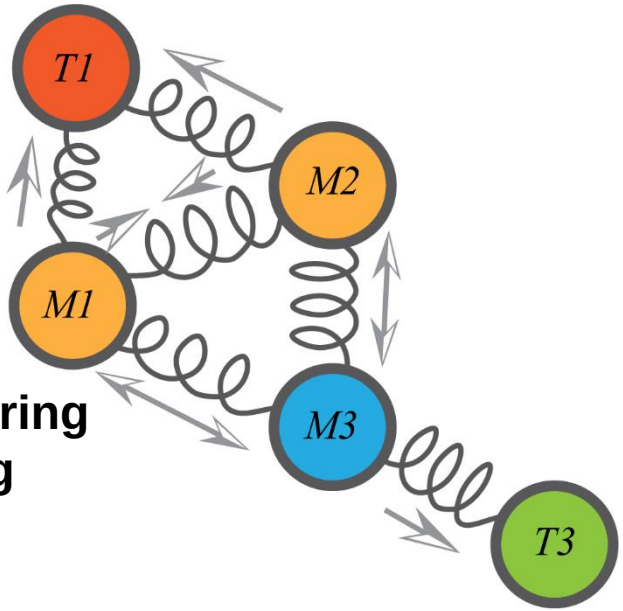



**Illustration of spring forces among devices and terminals**

## Design Variables:

- Initial device position
- Mass
- Damping
- Spring coefficients
- Spring rest length

## Governing Equations:

Attractive: $F = -k\Delta s$

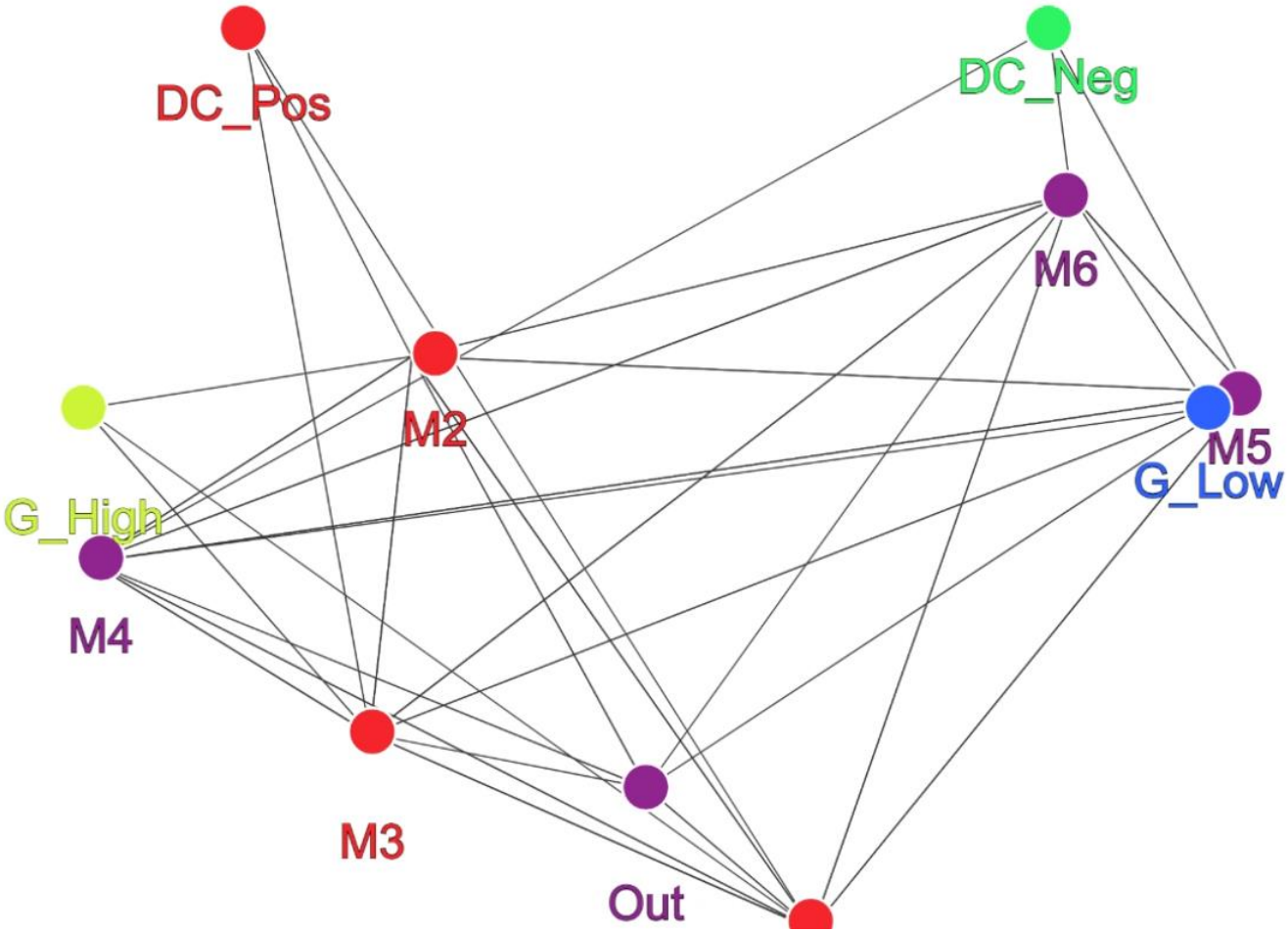
Repulsive: $F = -k \log\left(\frac{\Delta s}{c}\right)$

**Spring Force Assignment**

| Attractive Forces | Repulsive Forces |
|---|---|
| Device-Device (in-group) | Device-Device (out-group) |
| Device-Terminal (connected) | Device-Boundary |

Ref: Neil R. Quinn, Melvin A. Breuer, "A Forced Directed Component Placement Procedure for Printed Circuit Boards," IEEE Transactions on Circuits and Systems, 26(6):377-388 1979

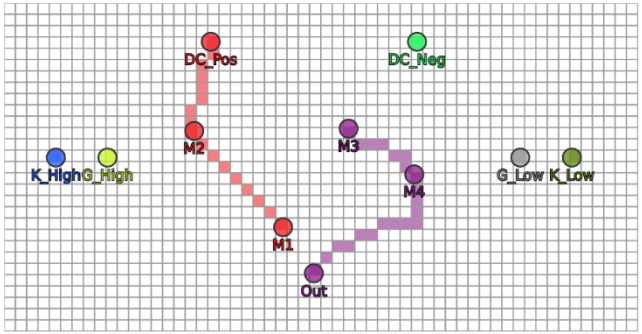
# Force Directed Placement Example



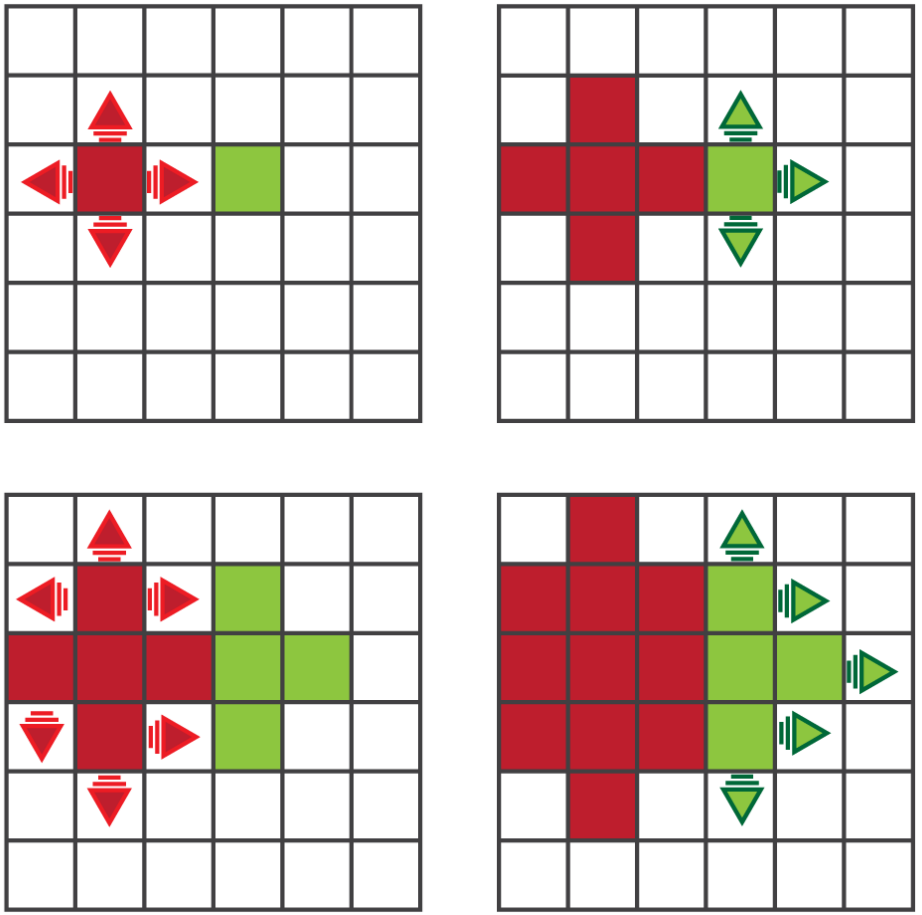
# Grid-Based Routing

**Data:** Layout as a 2D grid with cells initialized for routing
**Result:** Power and signal trace routing solution for given layout initialization;
**for** *cell in grid.cells* **do**
  **if** *cell.locked = True* **then**
    **for** *neighbor in cell.neighbors* **do**
      **if** *neighbor.group == None* **then**
        neighbor.group = cell.group;
      **else**
        continue;
      **end**
    **end**
  **end**
  **if** *all_cells_locked()* **then**
    loop = False;
  **end**
**end**

**Algorithm 1:** Simplified breadth-first search trace routing algorithm

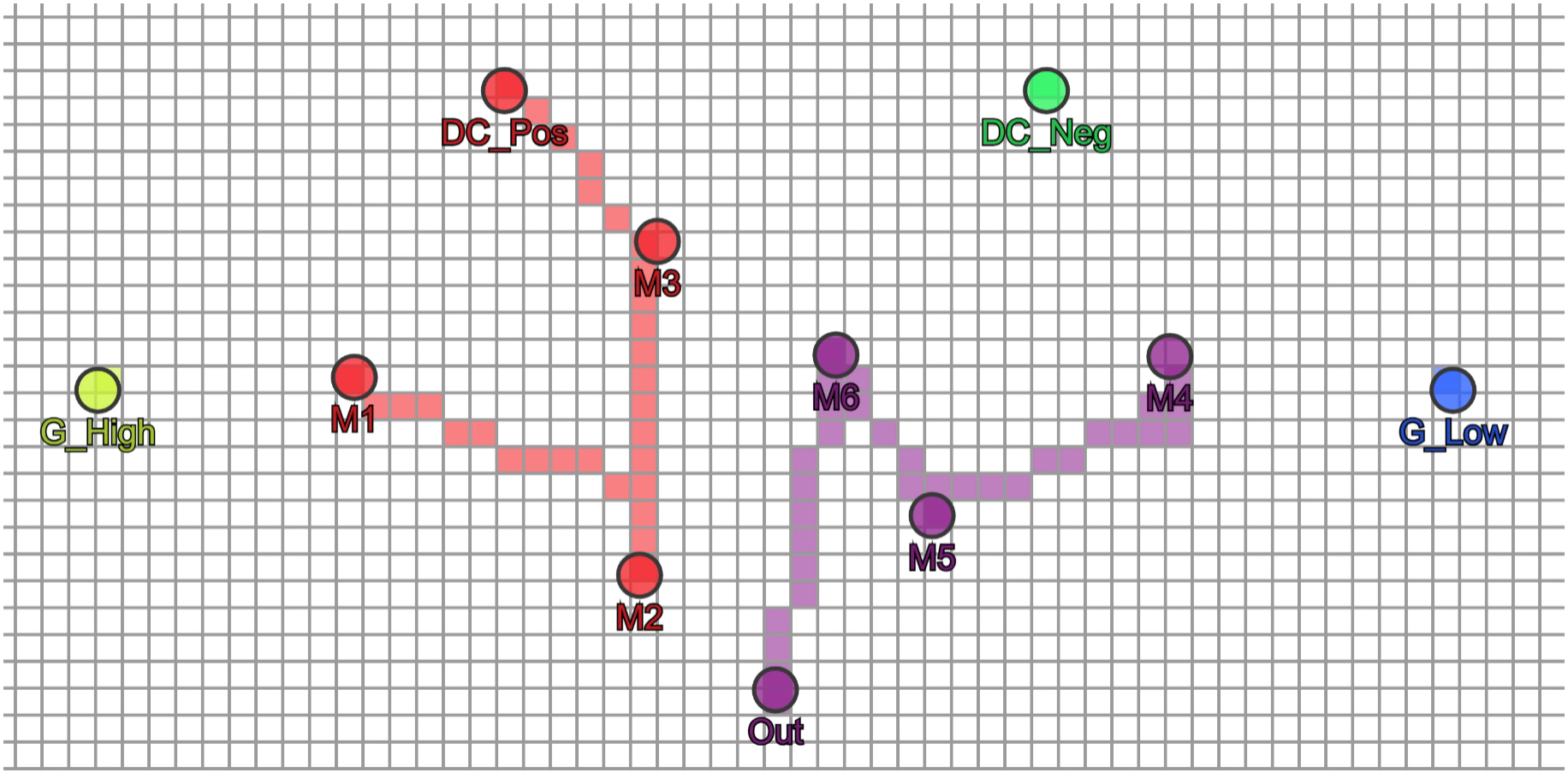



**Initial trace connectivity**

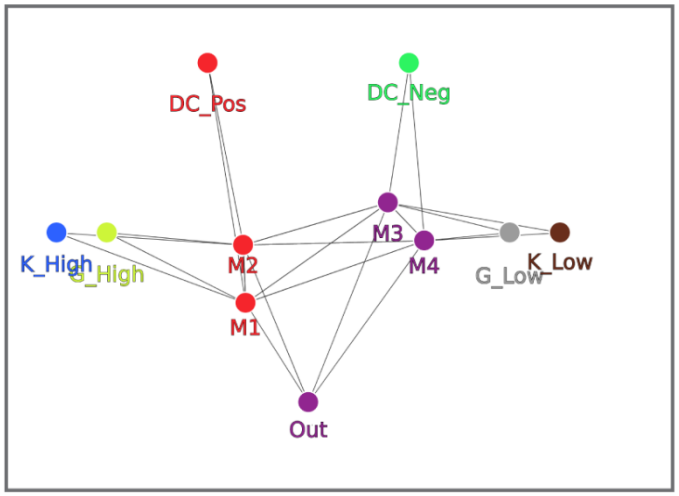


**Breadth-first search of neighboring cells during grid-based routing**

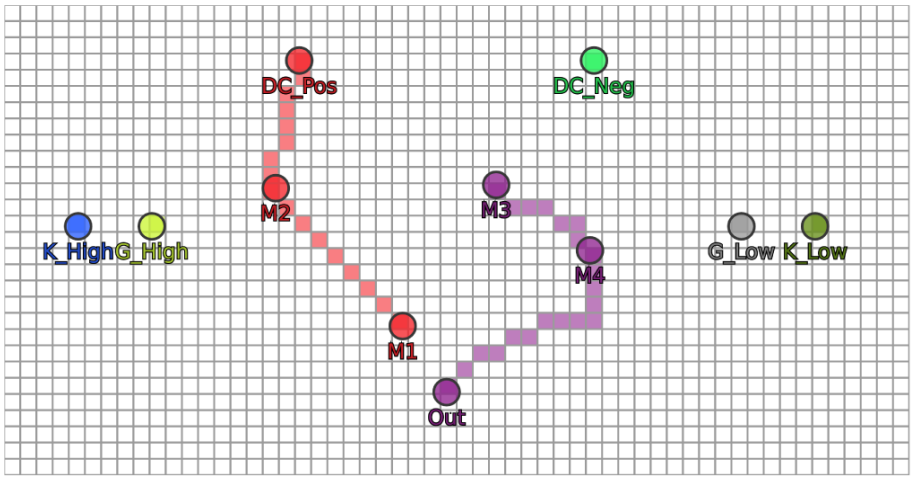
# Routing Example



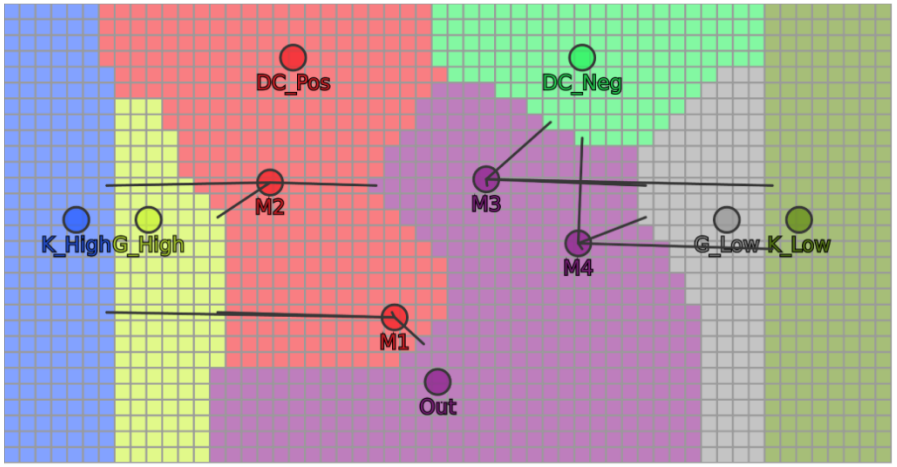
# Initial Results Example



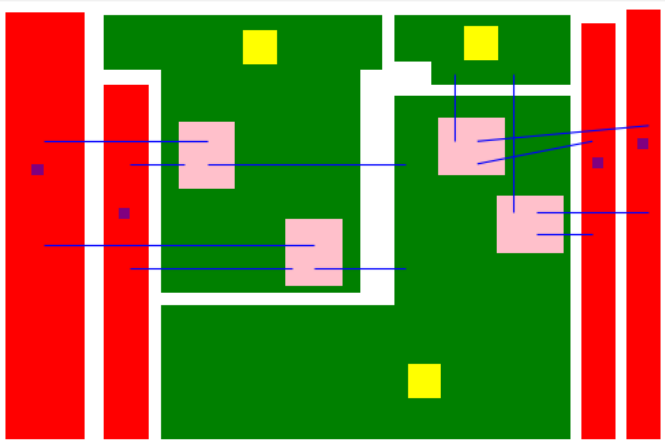

Placement




Routing

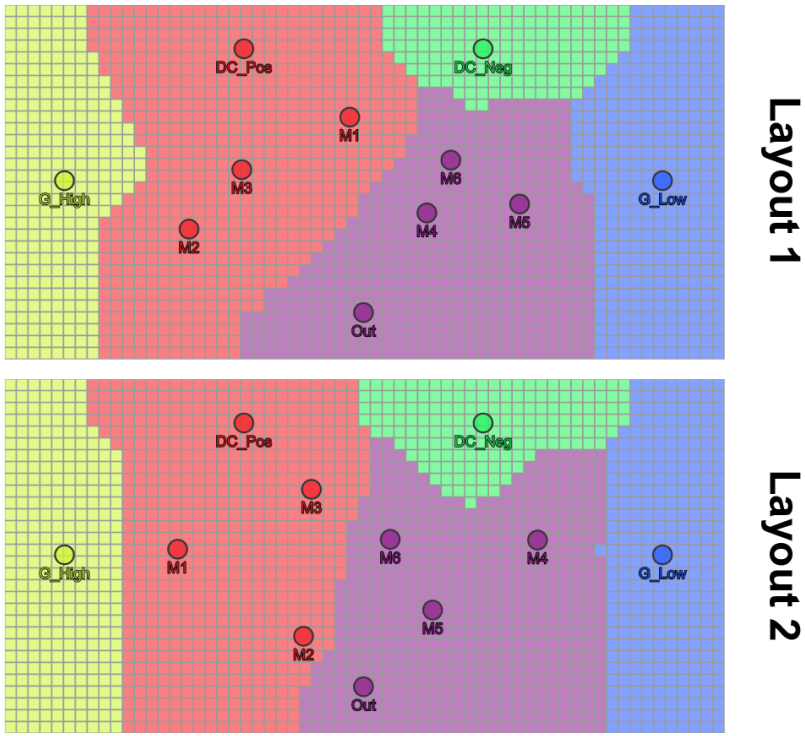



Finalized layout



Layout in PowerSynth

# Design Variations




**Place-and-route results**

**Initial layout in PowerSynth**

# Caveats and Future Work

- Limitations
  - Many assumptions have been made, including:
    - Planar, 2D structures
    - Vertical devices
    - Bondwire overlap
  - Prototype implementation
    - Not optimized for speed
    - Naïve
- Further Development
  - Validate hypothesis with case studies
  - Fully automate export
  - Expand capabilities into multi-layer, heterogeneous structures

# Summary

- PowerSynth is an EDA tool for power module layout under active development
- PowerSynth models and optimization results have been validated, but more work needs to be done to expand the solution space it produces
- VLSI techniques have been applied toward the placement and routing of components from a netlist starting point
- These features will be incorporated in PowerSynth and case studies performed to evaluate and refine the approach

# Thank you!