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PowerSynth Integrated CAD Flow for High Density

Quang Le[1], Imam Al Razi[2], Yarui Peng[2], H. Alan Mantooth[1]

[1]Electrical Engineering Department
[2]Department of Computer Science and Computer Engineering

Outline for today's talk

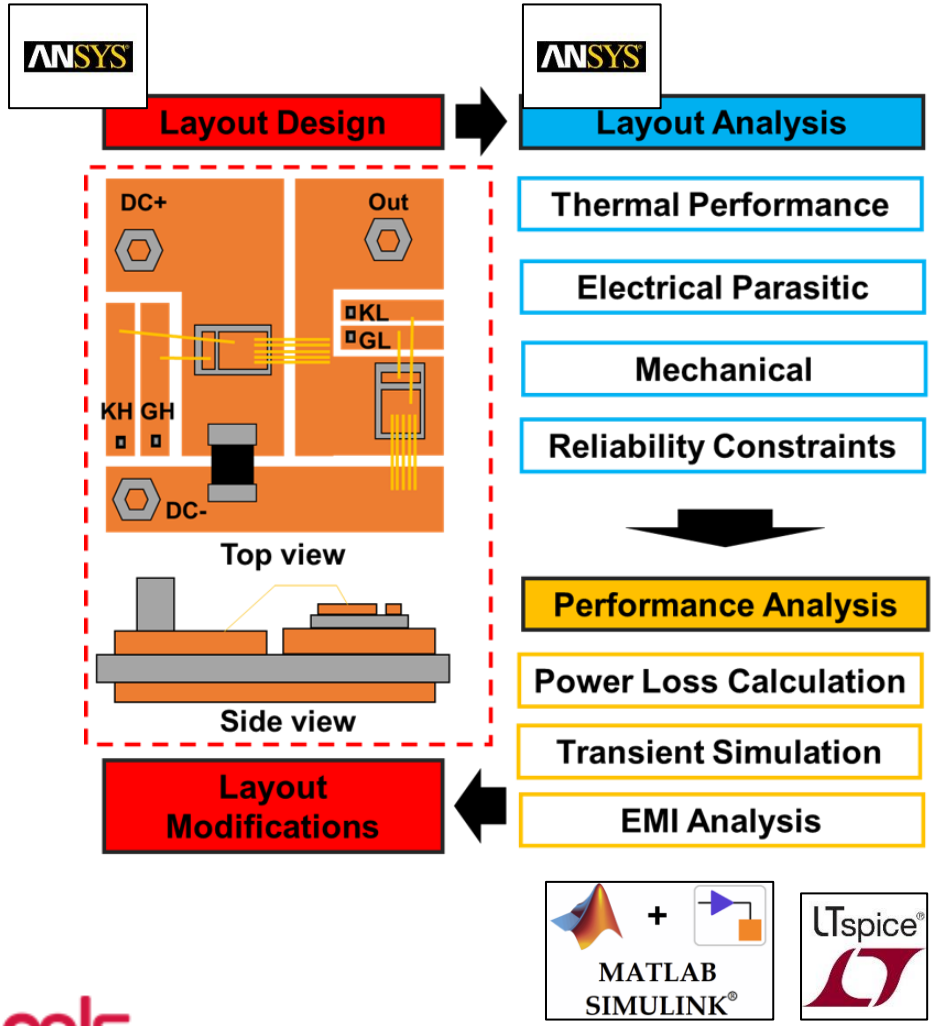
- MCPMs in Power Electronics
- Do we have the right tool ?
- PowerSynth Overview
- Constraints-Aware Layout Engine
- Reduced-order models APIs
  - Electrical Model
  - Thermal & Mechanical Model
- Reliability consideration
  - High-Voltage Design Rules Extraction
- Optimization Study
  - Results
- Conclusions and Future Works

Power Electronics is Everywhere !

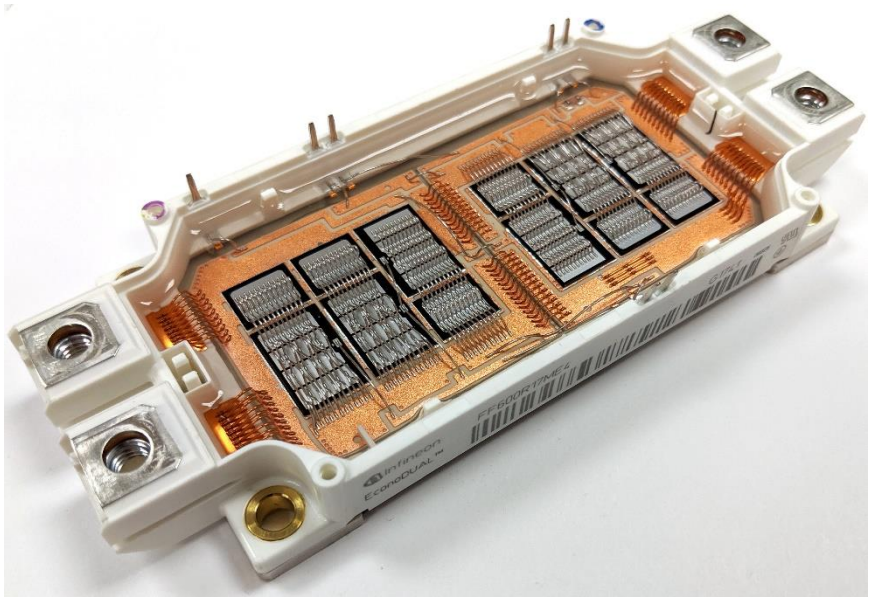
Do we have the right tool ?

https://medium.com/carl-pullein/why-you-should-stop-using-tools-for-jobs-they-were-not-designed-to-do-2985436d3c6a

MCPM traditional design flow

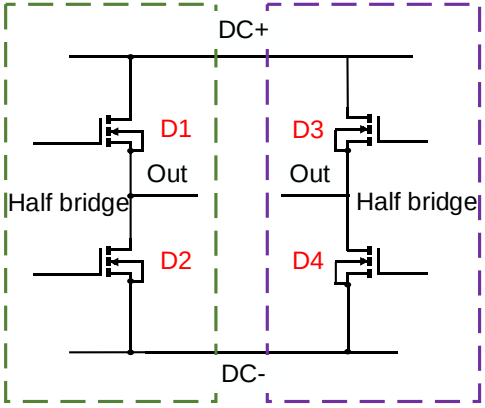


"The MCPMs traditional design flow involves many different computationally expensive tools in the process"

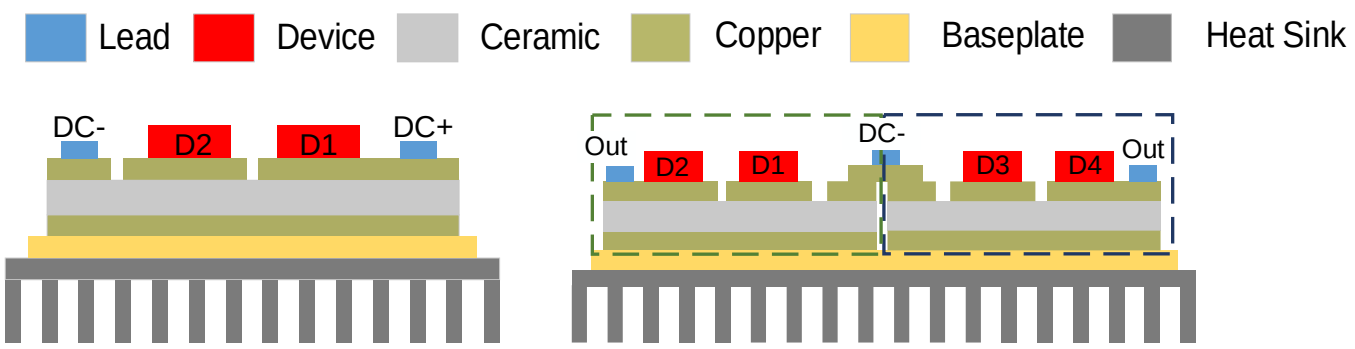


2D-2.5D-3D Layout Definition

- Definition under PowerSynth scope:
  - 2D layout: One device layer with routing layers on the same substrate
  - 2.5D layout: Multiple 2D designs connected on a supporting 2D plane
  - 3D layout: Multiple device layers stacked vertically on the same substrate



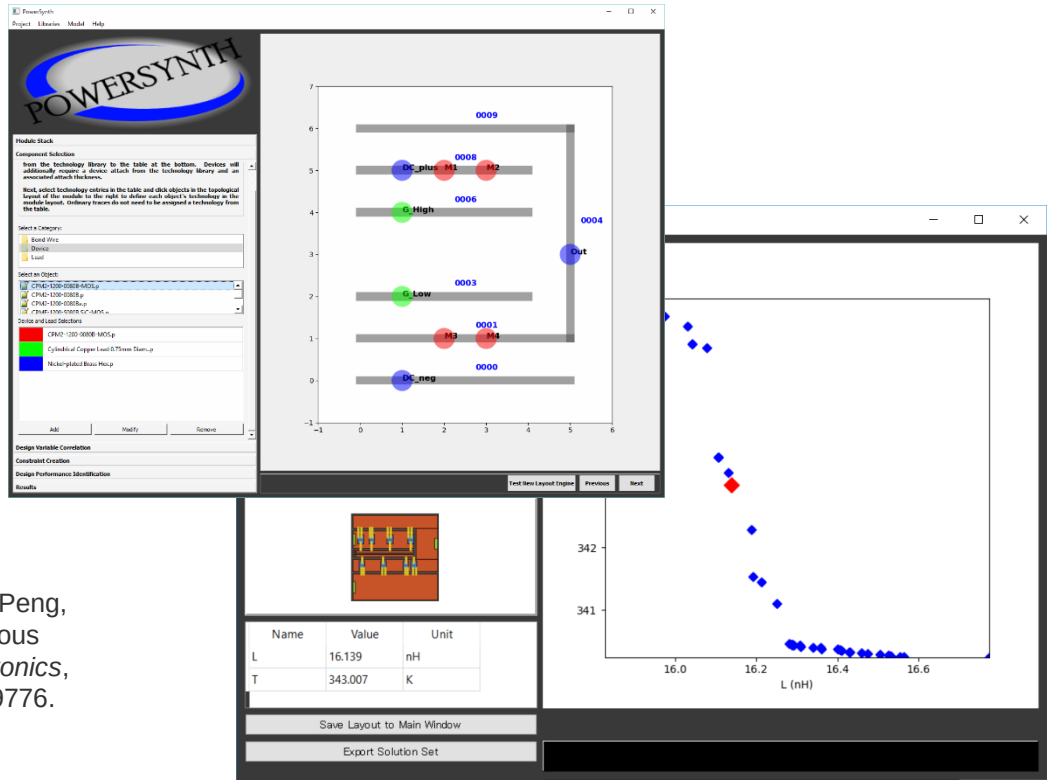
Circuit schematic of a full-bridge module



2D Half-bridge power module **2.5D Full-bridge power module** **3D half-bridge power module**

PowerSynth Overview

- EDA tool for multi-chip power modules (MCPM)
- Multi-objective layout optimization
- Reduced order models
- Pareto-front of tradeoffs
- Design export



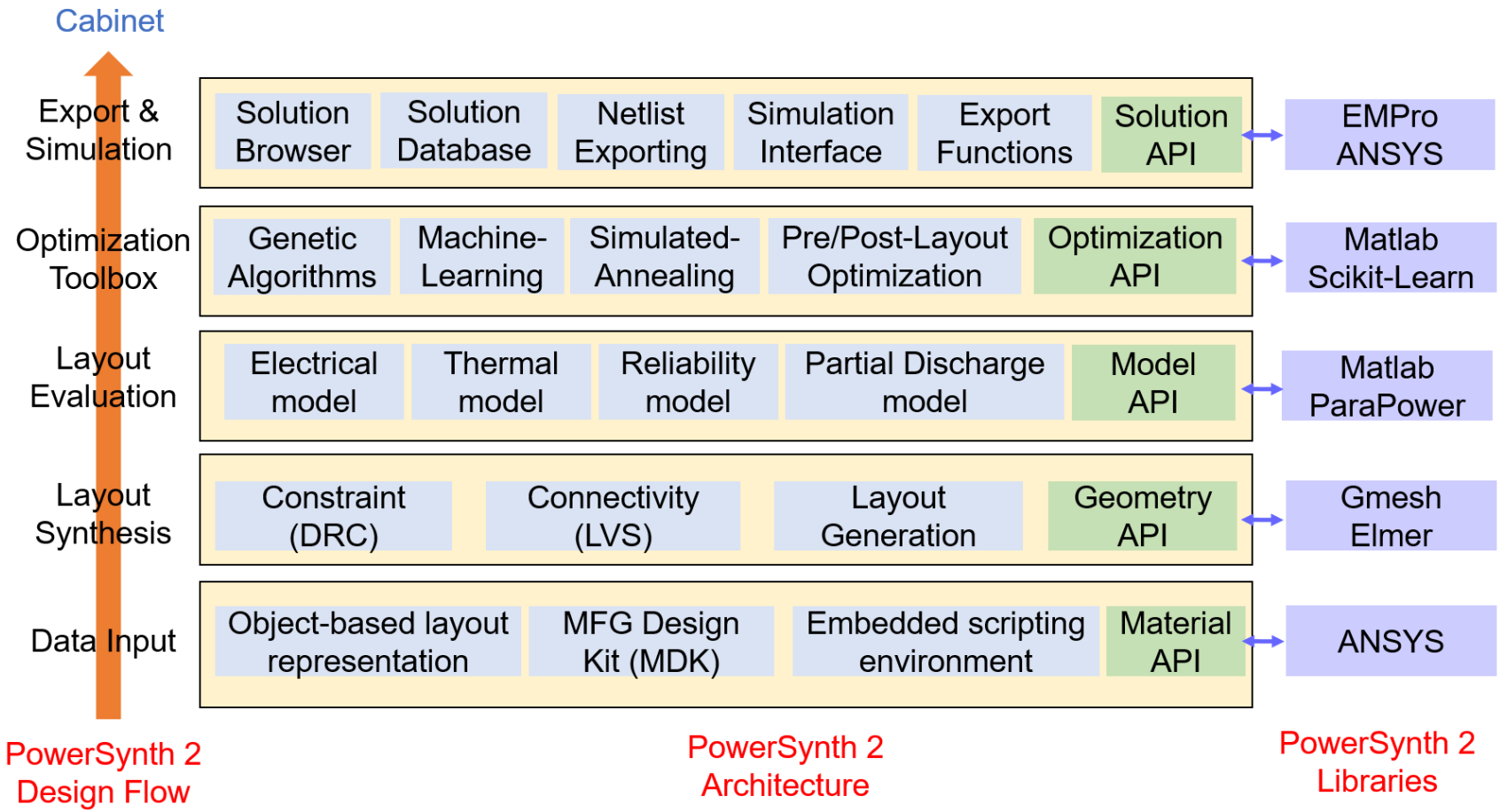
Power Synth V 1.1

[1] Tristan M. Evans, Quang Le, Shilpi Mukherjee, Imam Al Razi, Tom Vrotsos, Yarui Peng, H. Alan Mantooth , "PowerSynth: A Power Module Layout Generation Tool," in *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5063-5078, June 2019. doi: 10.1109/TPEL.2018.2870346 **Highlighted Paper**

Power Synth V 1.9

[2] I. Al Razi, Q. Le, T. M. Evans, S. Mukherjee, H. A. Mantooth and Y. Peng, "PowerSynth Design Automation Flow for Hierarchical and Heterogeneous 2.5-D Multichip Power Modules," in *IEEE Transactions on Power Electronics*, vol. 36, no. 8, pp. 8919-8933, Aug. 2021, doi: 10.1109/TPEL.2021.3049776.

PowerSynth 2 Architecture



Constraint-Aware Layout Engine

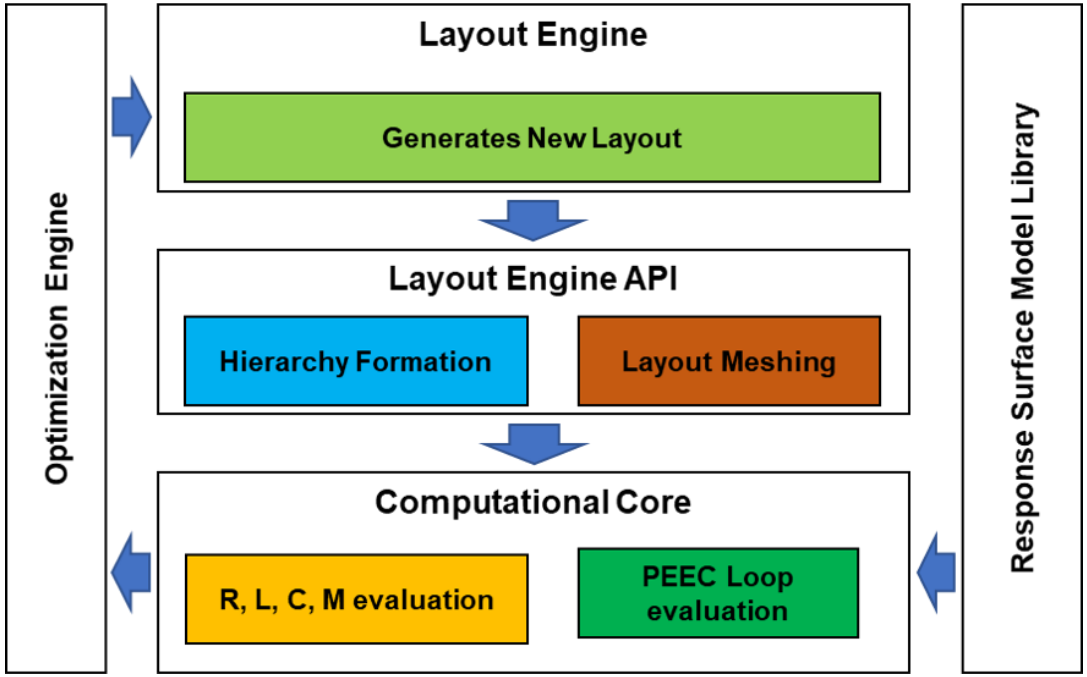
- Features:
  - Generic, hierarchical layout description script
  - Different types of constraints can be declared : design/reliability
  - 100% DRC-clean solutions
  - Hierarchical approach enables 2.5D and 3D layout handling.
  - Generic, scalable, and efficient methodology→ SOA 2D/3D packaging solutions
    - Hierarchical corner stitch data structure: layer-based geometry representation
    - Hierarchical constraint graph (CG) evaluation guarantees DRC-clean solutions
    - Randomization: layout solution generation method (exhaustive search)
  - Three types of layout generation capability:
    - Minimum-sized layout
    - Variable floorplan sized
    - Fixed floorplan sized

PowerSynth Modeling Libraries

Electrical Modeling Overview

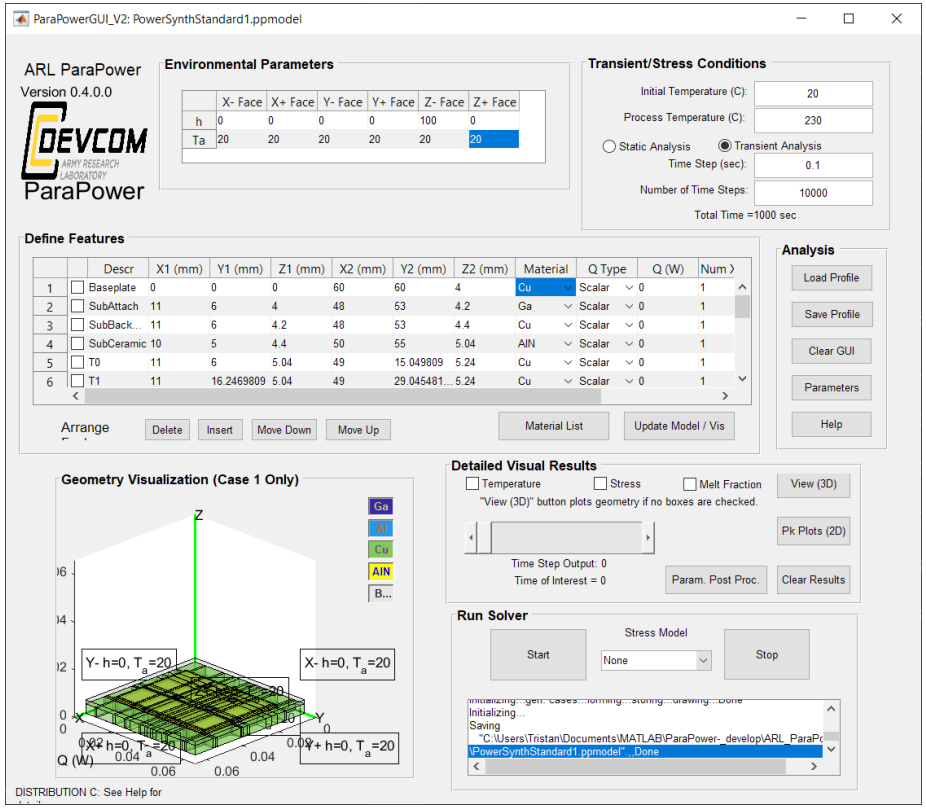
Features:

- Response Surface technique to formulate equations the MCPM trace parastic parameters.
- Fast and efficient Meshing algorithm based on Corner-Stitch data structure.
- A PEEC-based model considers mutual coupling among conductors.
- Fast and accurate results in compared to FEA



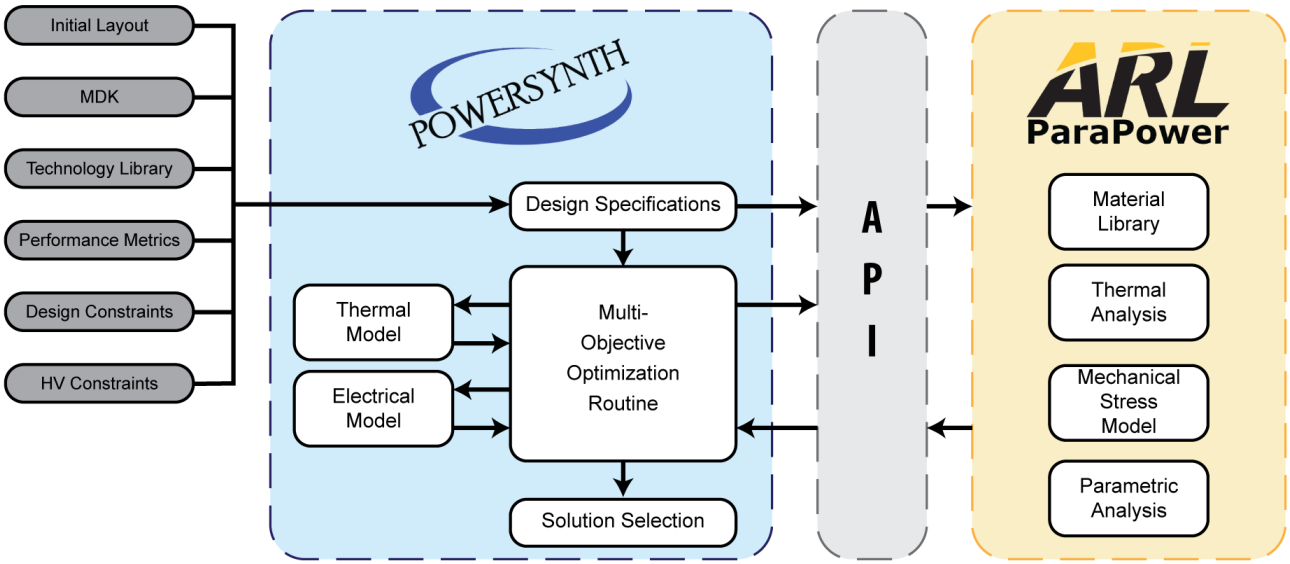
Thermal and Mechanical Modeling

- Open source co-design tool by US Army Research Lab
- Fast, thermo-mechanical analysis of power electronics modules
- Parametric analysis tools
- Support for phase change materials



https://github.com/USArmyResearchLab/ParaPower

Thermal and Mechanical Modeling



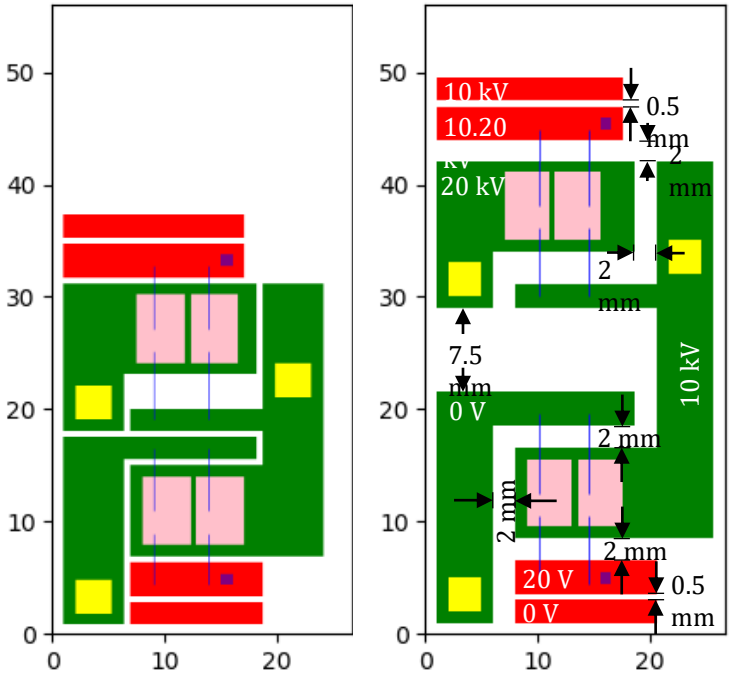
API to leverage:

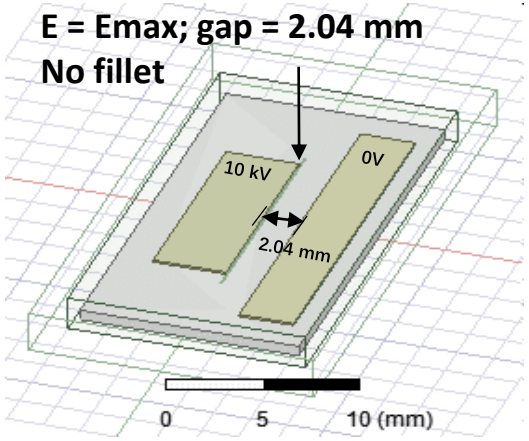
- PowerSynth layout generation and electrical parasitics extraction
- ParaPower 3D thermo-mechanical analysis

High-Voltage Design Rules Extraction

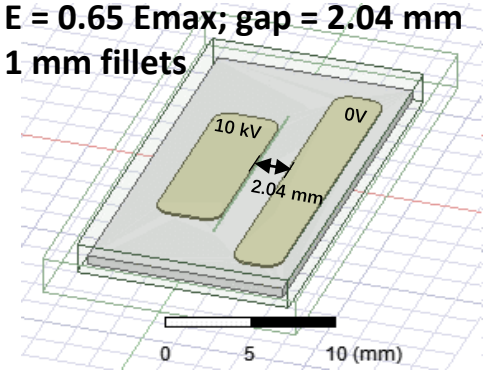
- Design rules to prevent partial discharge

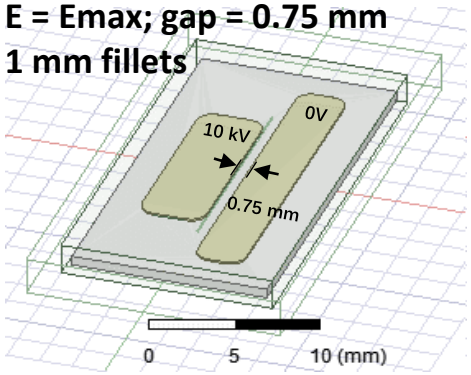
Default layout vs.
Layout with design rules applied





Gap can be reduced to about 40% of the original gap if fillets are used.





On-going: Analytical model development based on experimental results

[3] Shilpi Mukherjee et. al, "General Equation to Determine Design Rules for Mitigating Partial Discharge and Electrical Breakdown in Power Module Layouts", in WiPDA-Asia, 2020.

Results

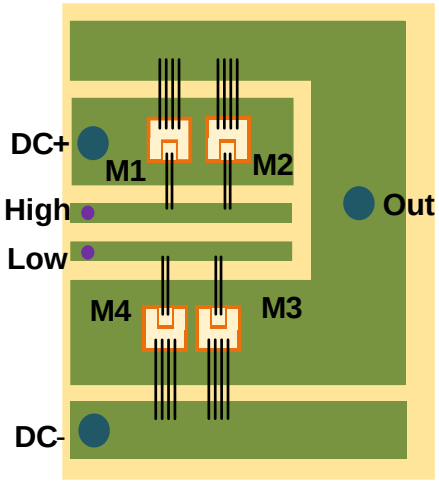
In this work:

1. An electro-thermal performance comparison has been performed between 2D and 3D MCPM layouts.

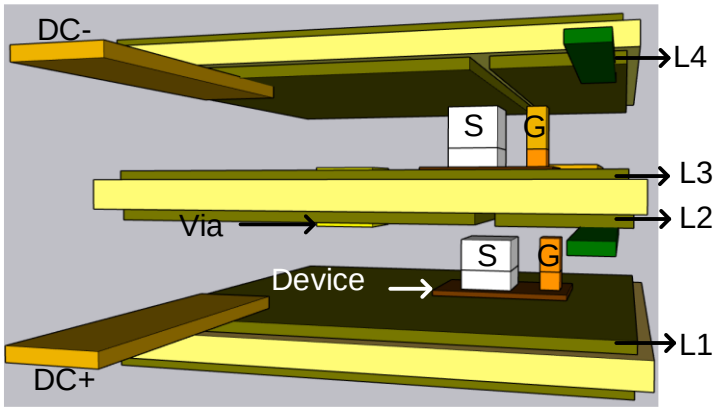
2. A wire-bonded 3D layout has been optimized aiming at reducing power loop inductance and maximum junction temperature.

2D vs. 3D Performance Comparison

- **Initial layout for Half-bridge module:**

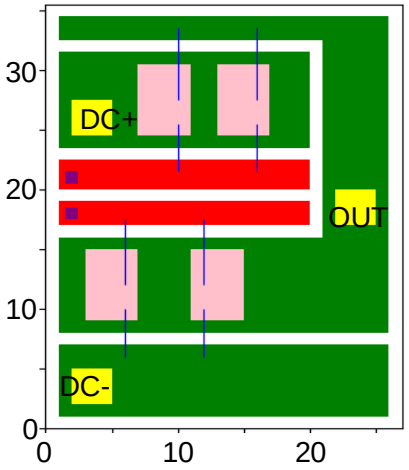


2D wire-bonded

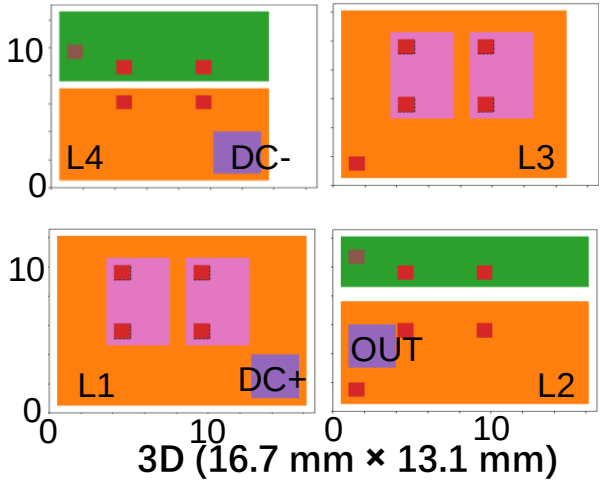


3D wire-bondless

- **Min-sized Result:**



2D (25.3 mm × 35.2 mm)

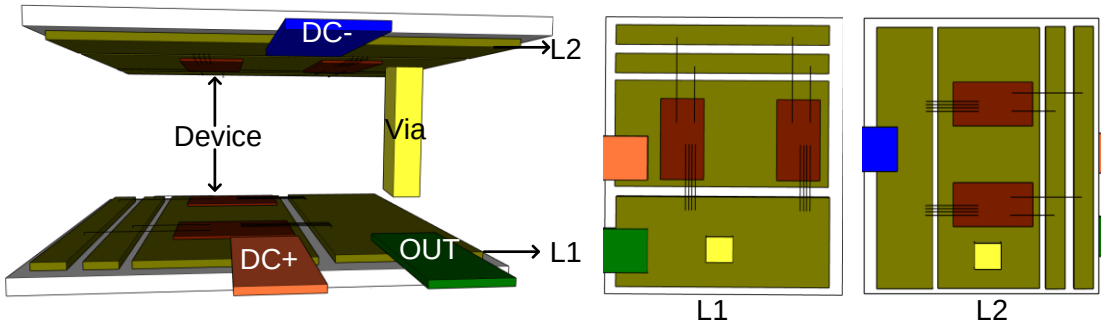


3D (16.7 mm × 13.1 mm)

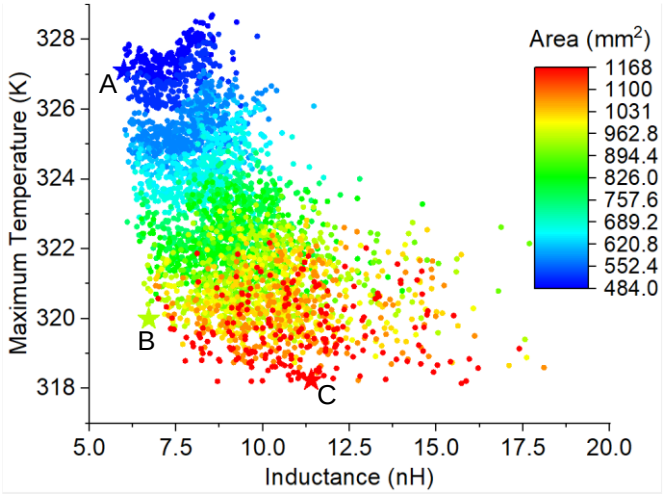
Performance Metric	2D	3D
Loop Inductance (@100 KHz)	20.23 nH	1.52 nH
Max Temperature	332.64 K	354.94 K

3D Layout Optimization

- Initial layout

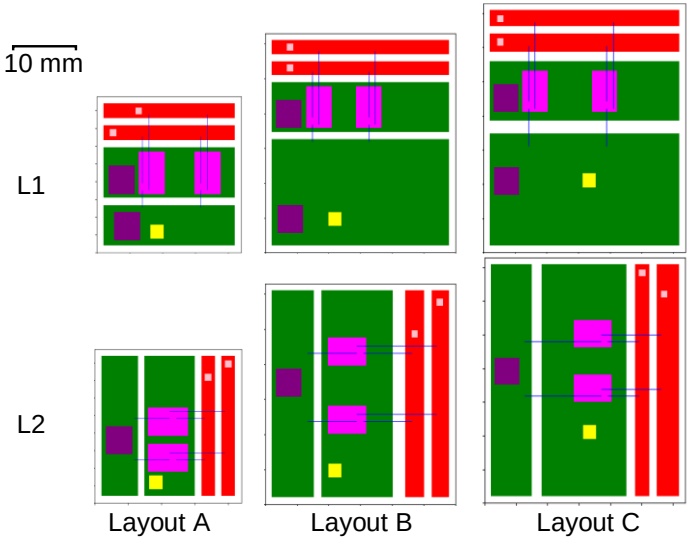


3D structure of a wire-bonded MCPM



Complete solution space

- Optimization:
  - Electro-thermal optimization
  - ParaPower thermal + PowerSynth electrical
  - 5000 solutions with varying floorplan sizes
  - Layout generation runtime ~ 6 mins
  - Three selected layouts:
    - Layout A → Electrically optimized
    - Layout B → Balanced
    - Layout C → Thermally optimized



Three selected layouts

Conclusion and Future works

- The latest architecture of PowerSynth v2.0 has been demonstrated.
- Shows the tool capabilities for 2D/2.5D/3D MCPM layouts optimization.
- Promising results toward high-density MCPM layout optimization.
- More modeling efforts in the future to further reduce the computational complexity in 3D layout.
  - New electrical modeling approach using loop-based method from VLSI

[4] Q. Le, I. A Razi, H. A Mantooth and Y. Peng, “Fast and Accurate Inductance Extraction For Power Module Layout Optimization Using Loop-Based Method” in *IEEE Energy Conversion Congress and Exposition*, 2021 (Accepted)

Thank you !
Question ?

qmle@uark.edu