IEEE ENERGY CONVERSION CONGRESS & EXPO
Vancouver, Canada Oct. 10-14

Fast and Accurate Inductance Extraction for Power Module Layout Optimization Using Loop-Based Method

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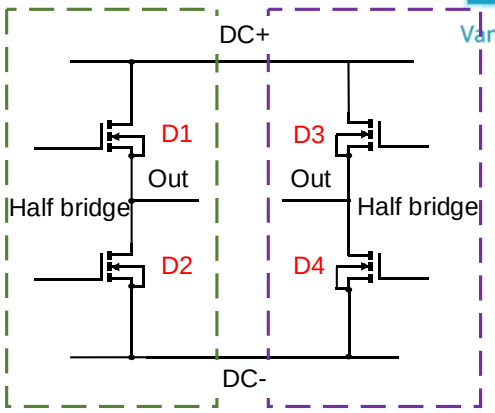
Outline

- Overview
  - Traditional design flow
  - PowerSynth (an EDA tool) Introduction
- Motivation
- Methodology
  - Loop-based parasitics extraction
- Results
  - Accuracy and Performance comparison among different models
  - Optimization study
- Conclusions and Future Works

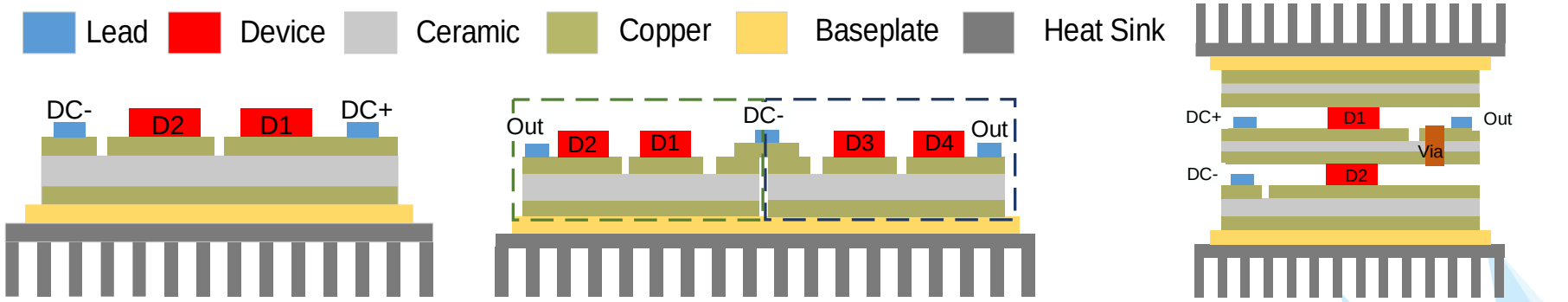
Power Electronics is Everywhere !

2D-2.5D-3D Layout Definition

- Definition under PowerSynth scope:
  - 2D layout: One device layer with routing layers on the same substrate
  - 2.5D layout: Multiple 2D designs connected on a supporting 2D plane
  - 3D layout: Multiple device layers stacked vertically on the same substrate

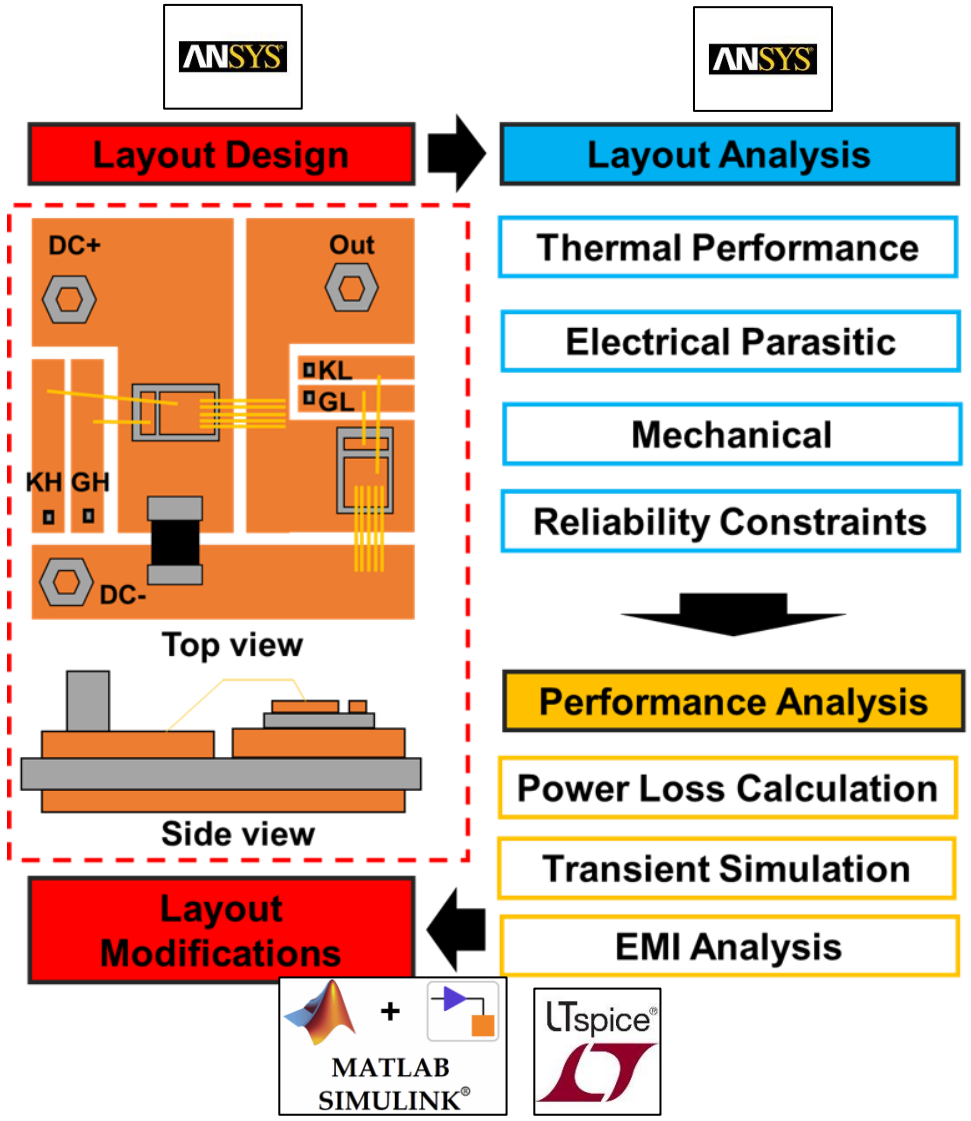


Circuit schematic of a full-bridge module

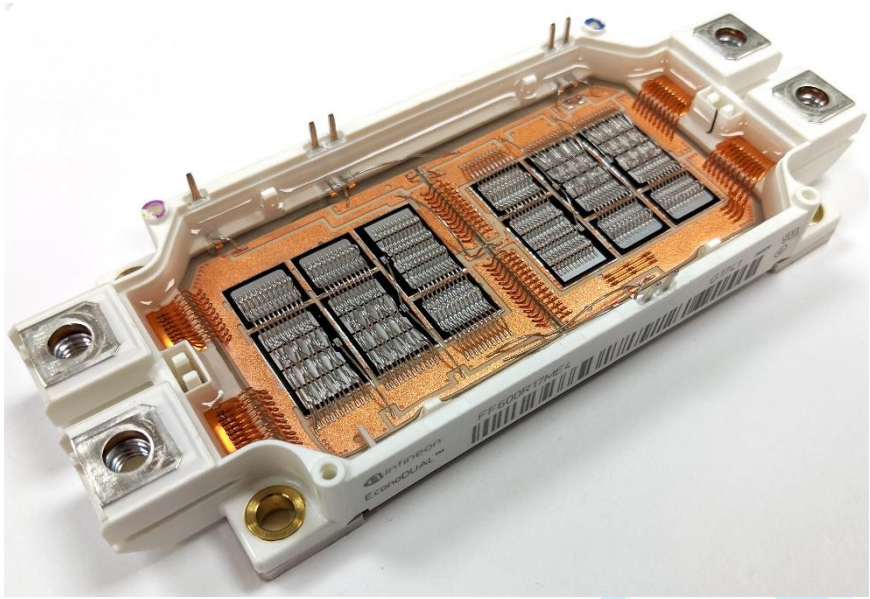


2D Half-bridge power module **2.5D Full-bridge power module** **3D half-bridge power module**

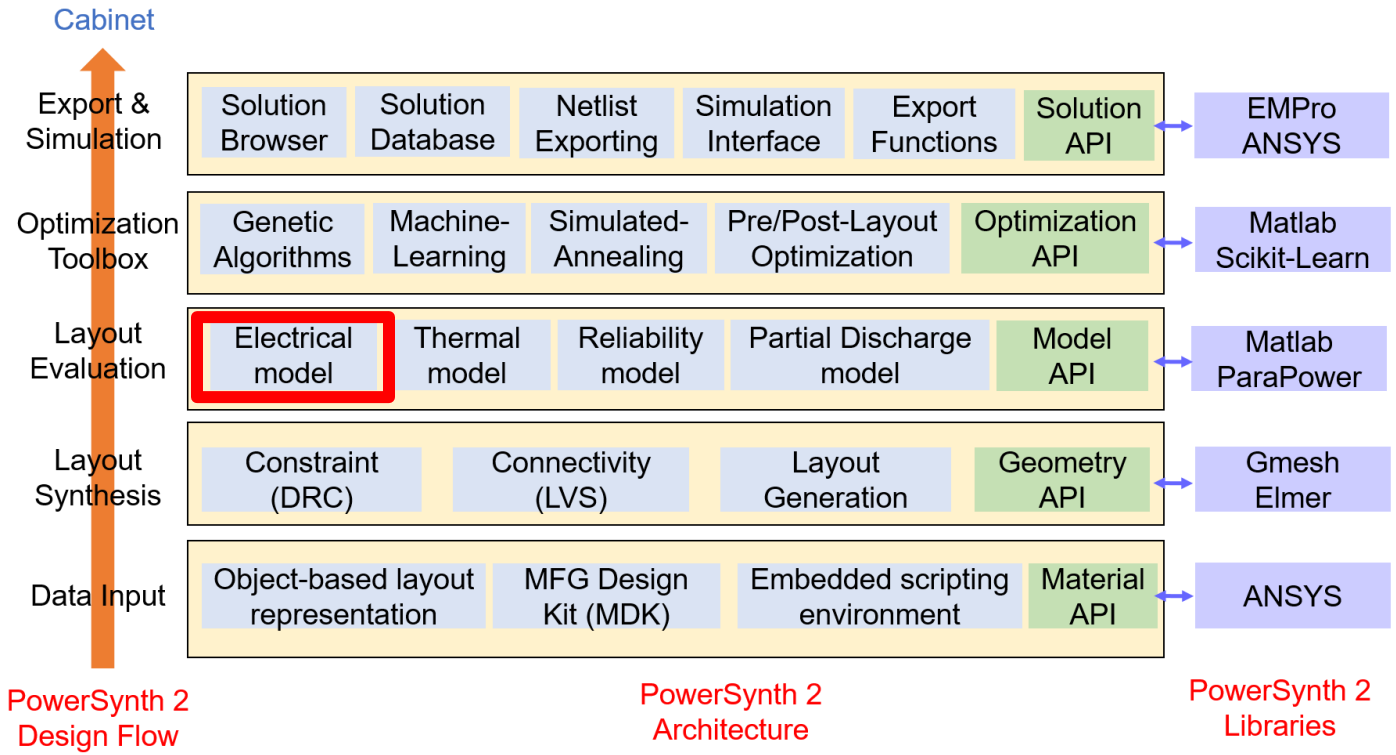
MCPM traditional design flow



"The MCPMs traditional design flow involves many different computationally expensive tools in the process"



PowerSynth Overview



- EDA tool for multi-chip power modules (MCPM)
- Multi-objective layout optimization
- Reduced order models
- Pareto-front of tradeoffs
- Design export

Motivation

- Wide band-gap devices operate at high frequency, and high voltage and currents:
  - High voltage overshoot
  - Higher switching losses
- Layout parasitic analyses need to be done during design states:
  - FEA simulations
  - FastHenry

These analyses are accurate, but very time consuming and therefore not suitable for a layout optimization process

Previous approach in PowerSynth

PEEC approach:

- Fast and accurate for most 2D layout cases
- Response surface methodology.

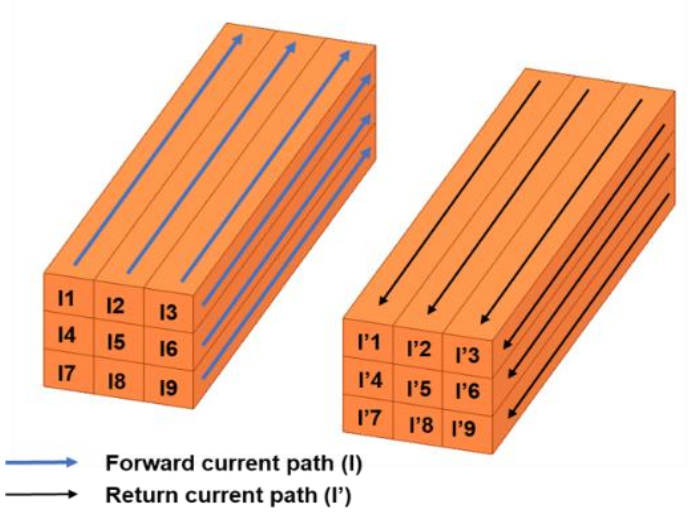
However:

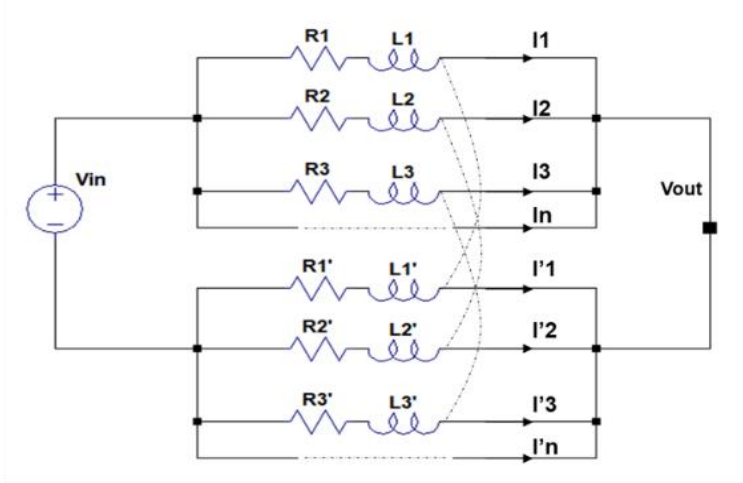
- Huge number of elements when going to more complicated layout
- Hard for post layout circuit simulation study since the netlist size is large

Loop-Based Parasitic Extraction

New loop-based modeling approach:

- Efficient mutual inductance calculation
- Divide and conquer strategy during evaluation
- Less elements in the extracted netlist → more suitable for time domain circuit simulation
- Have been proven to be efficient in VLSI

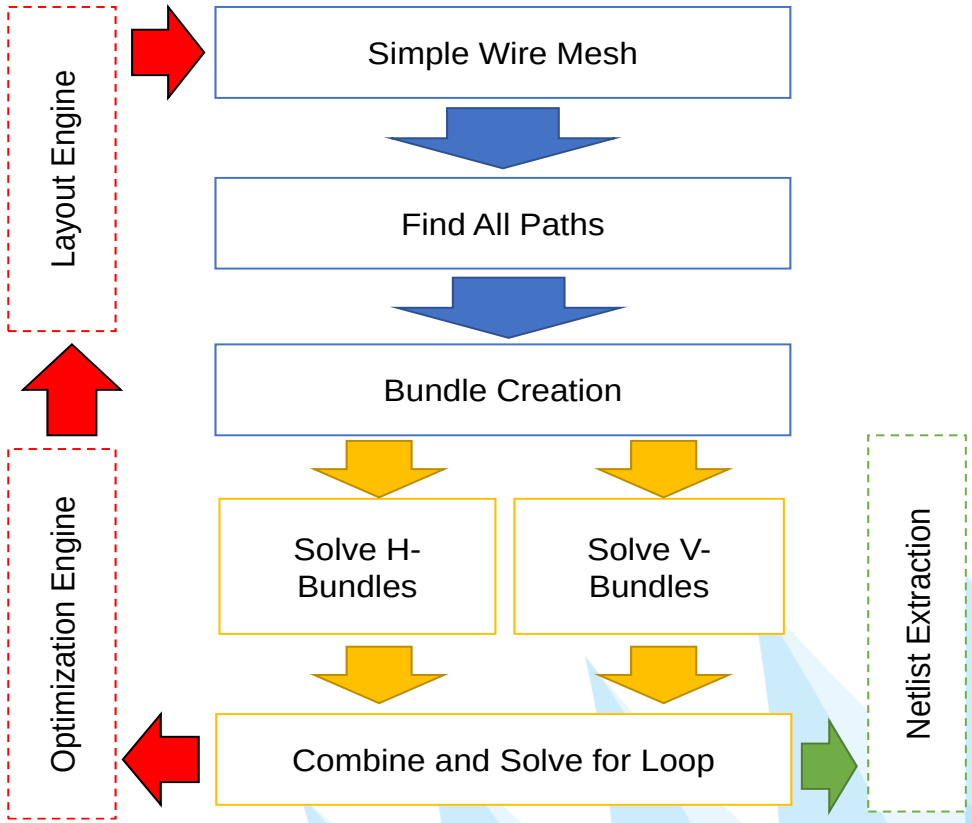




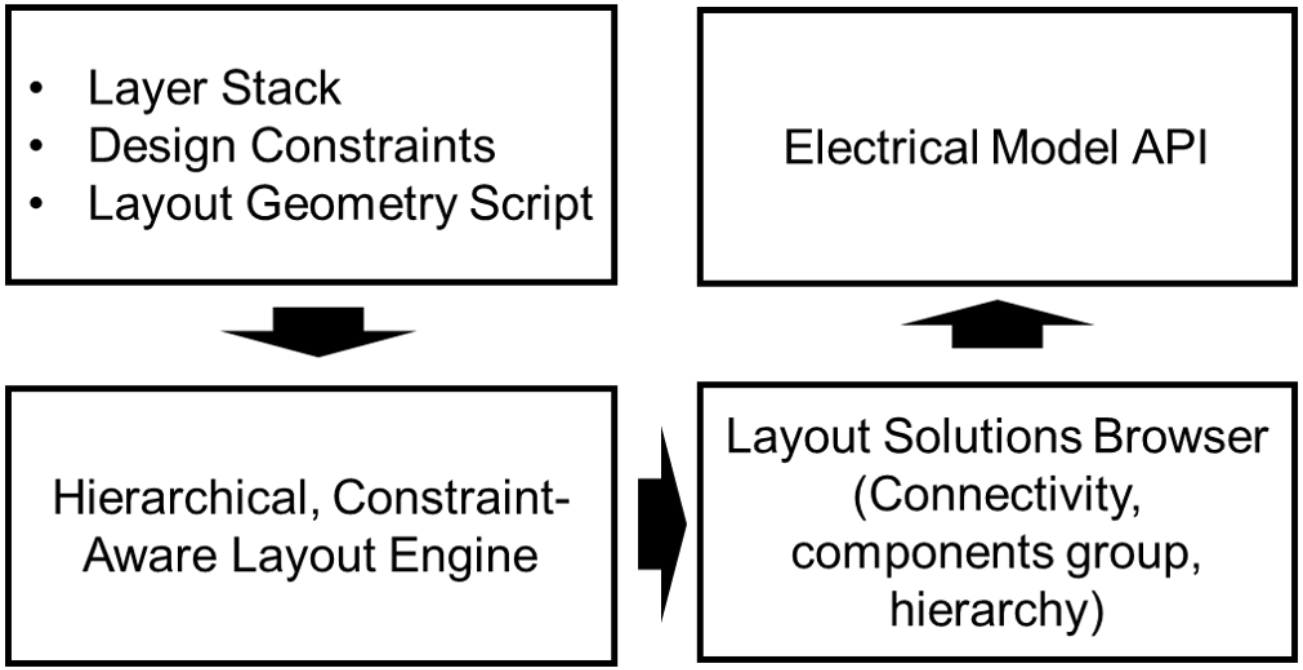
Methodology

Modeling methodology:

- Path finding algorithm has been used to define the return paths.
- Directed graph stores the information of the path
- The layout can be divided in multiple Horizontal and Vertical bundles
- Each bundle's parasitic result is evaluated separately using matrix calculations
- Combined solutions to solve for the final result

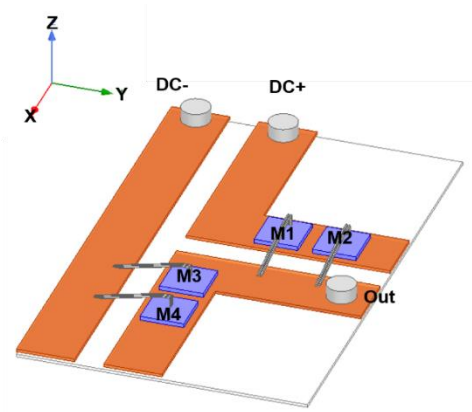


Layout Engine API

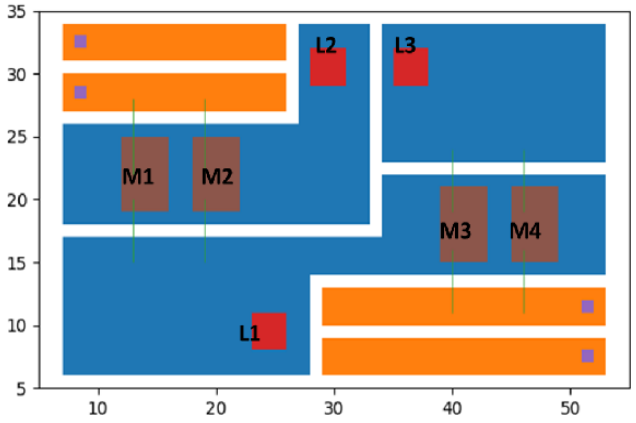


- Converts Layout information into geometrical data used in the electrical model.
- Ensure the correct hierarchical connection among electrical components.

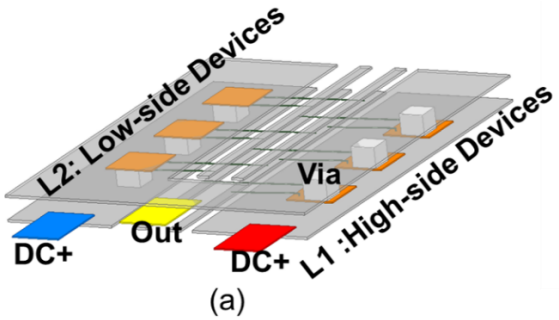
Example layout cases

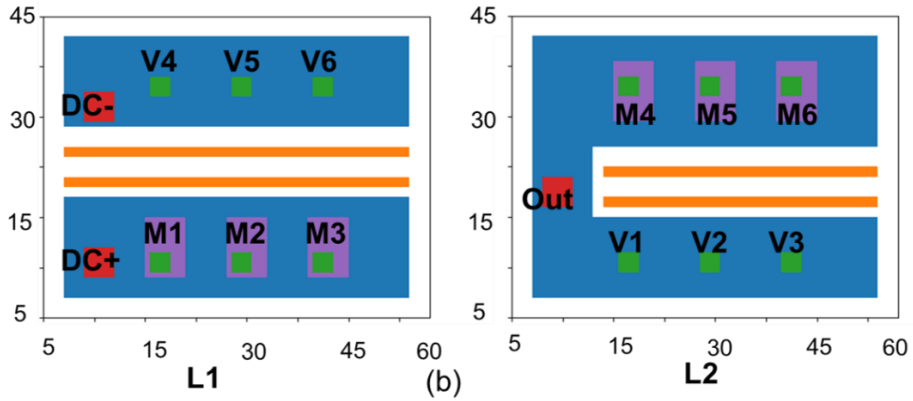


Simple 2D layout



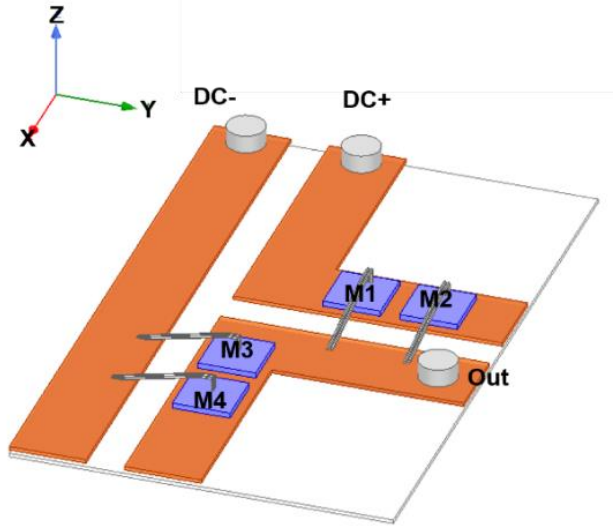
2D layout for optimization study



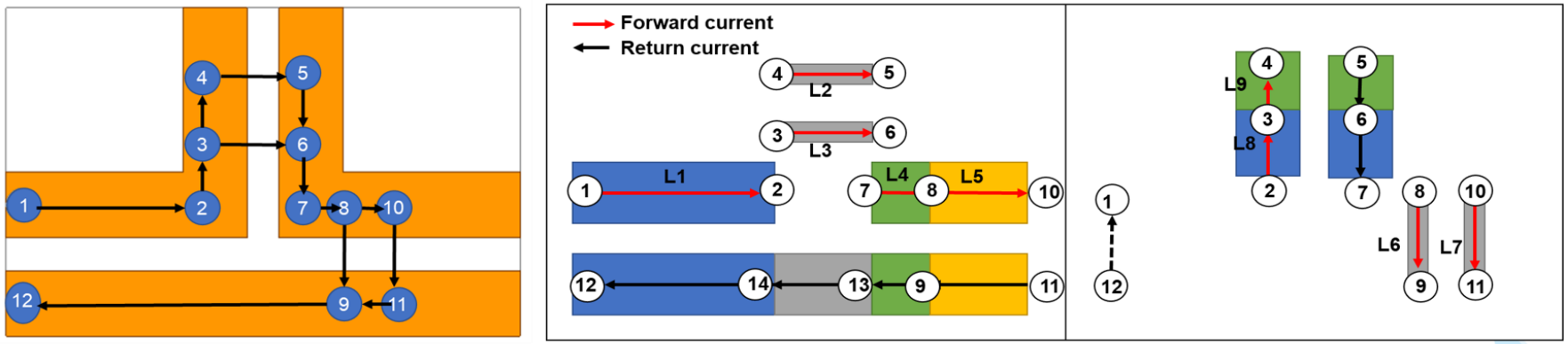


A 3D Half-bridge module (a) 3D view of MCPM layout example (b) Layouts of bottom (L1) and top (L2) layers.

Evaluation for each bundle



Simple layout case to demonstrate the bundle creation process



(a) Digraph formation for half-bridge (b) Horizontal bundles (c) Vertical bundles.

Loop-Based Parasitic Extraction

Key equations:

$$\boldsymbol{Pa} = \boldsymbol{u} \qquad (1)$$

$$\boldsymbol{PB} = \boldsymbol{M} \qquad (2)$$

$$\boldsymbol{I}(j) = \boldsymbol{B}(j) - V_{out} \times a \qquad (3)$$

$$V_{out} = \frac{\sum \boldsymbol{B}\,(i,j)}{\sum a} \qquad (4)$$

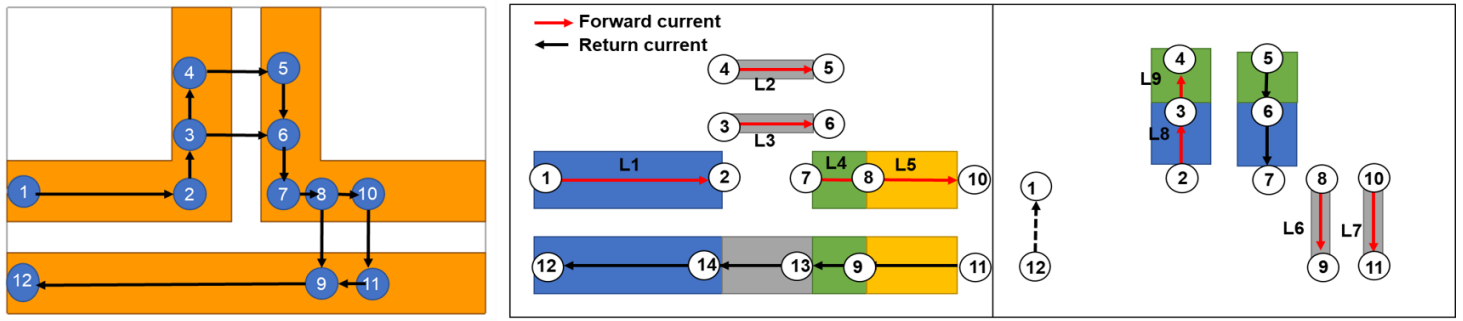
$$\boldsymbol{Z}_{\text{loopi}} = \left(M^T \times \boldsymbol{I}\right)^{-1} \qquad (5)$$

$$\mathbf{P} = \begin{pmatrix} Z_{1,1} & Z_{1,2} & \cdots & Z_{1,n} \\ Z_{2,1} & Z_{2,2} & \cdots & Z_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{n,1} & Z_{n,2} & \cdots & Z_{n,n} \end{pmatrix}$$

$$\boldsymbol{Z}_{i,j} = R_{ij} + j\omega L_{ij}$$

$\boldsymbol{Z_i}$ is evaluated for each bundle. The final loop result from: $\boldsymbol{AI} = \boldsymbol{V}$ (6)

$$\mathbf{A} = \begin{pmatrix} Z_{loop_{1,1}} & Z_{loop_{1,2}} & \cdots & Z_{loop_{1,k}} \\ Z_{loop_{2,1}} & Z_{loop_{2,2}} & \cdots & Z_{loop_{2,k}} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{loop_{k,1}} & Z_{loop_{k,2}} & \cdots & Z_{loop_{k,k}} \end{pmatrix}$$



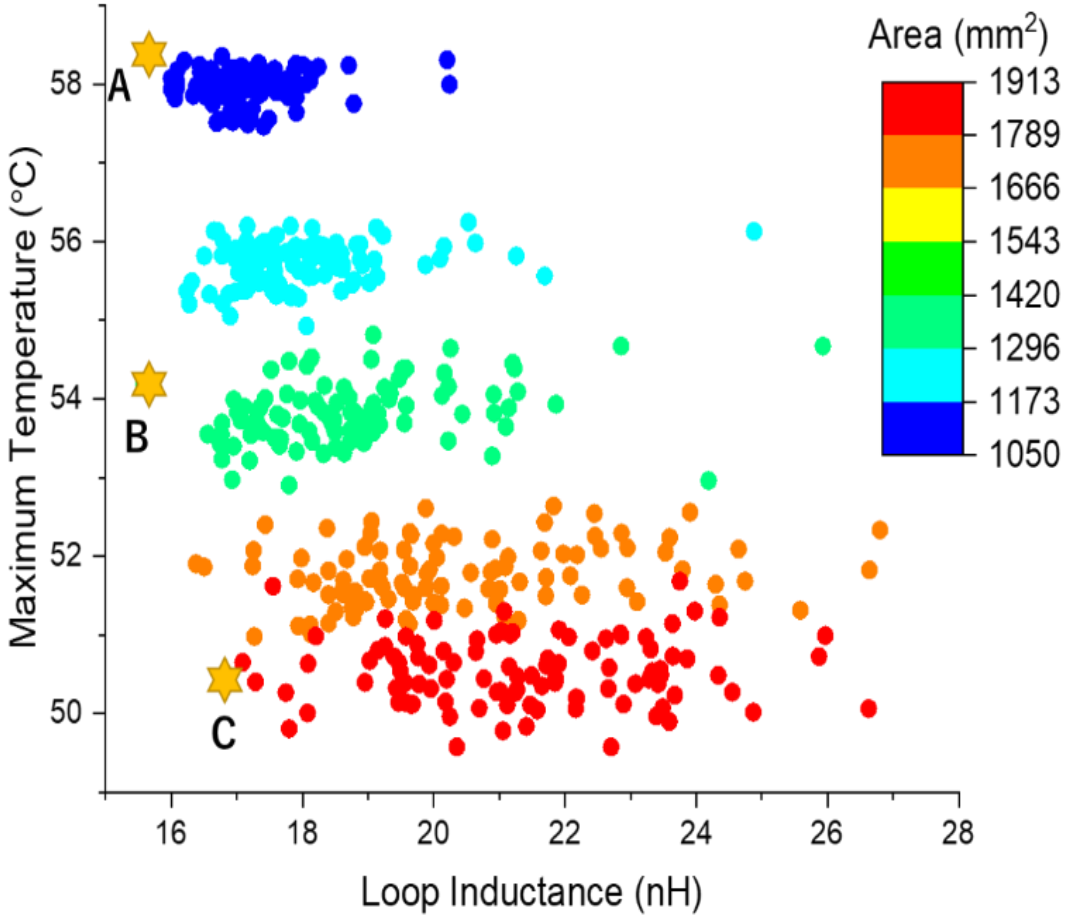
(a) Digraph formation for half-bridge (b) Horizontal bundles (c) Vertical bundles.

Model Validation Results

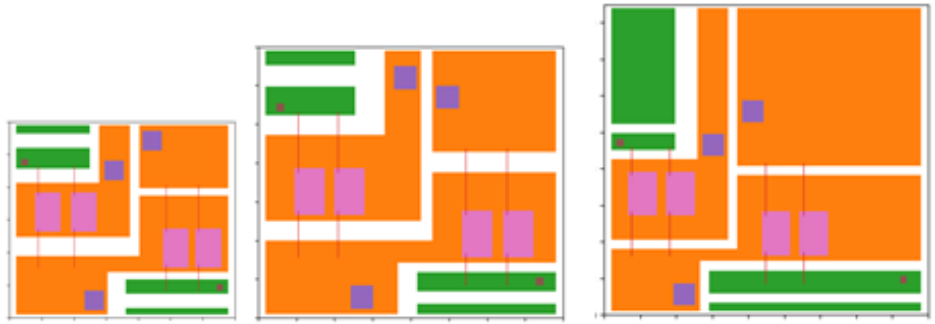
- Extraction results show less than 7% error compared to FastHenry extraction using both PEEC and loop-based methods.
- The formulation time is similar to the PEEC method.
- The loop-based method shows up to **800**× speed up for matrix evaluation in the second layout case.
- The netlist size from the loop-based method is much smaller than that of PEEC

Layout Case	Methods	L_{Loop} (nH)	Run Time (s)			Netlist size	Speed up	Error
			Formulation	Evaluation	Total Time			
Layout 1	**FastHenry**	17.3	---	---	8	1	---	---
	PEEC	16.1	0.5	0.345	0.8345	1820	9.6×	6.9%
	This work	16.5	0.42	1.4m	0.434	9	18.6×	4.6%
Layout 2	**FastHenry**	15.3	---	---	22.9	1	---	---
	PEEC	14.5	1.3	2	3.3	32310	11.5×	5%
	This work	15.6	0.26	2.5m	0.285	18	82×	1.9%
Layout 3	**FastHenry**	7.93	---	---	25	1	---	---
	This work	8.54	0.8	2.43m	0.824	50	30×	7.1%

Layout Optimization Results



Solution space for the electrothermal optimization



A **B** **C**

	L_{loop} (nH)	Max Temp. ($°C$)	Area (mm^2)
A	15.7	58.4	30 × 35
B	15.5	54.2	40 × 35
C	16.8	50.4	45 × 42

Validation of the Optimization Capability

Optimization trend comparison

- 50 layouts with the same design footprint of $30 \times 35\ (mm^2)$ in the solution space are evaluated
- Normalized inductance result is used for comparison
- The loop-based method shows the same trend while having a 2% average error.

Conclusion and future works

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Conclusion

- A new loop-based technique for inductance extraction in power module layout has been demonstrated
- Fast and accurate, suitable for the layout optimization objective
- Works for both 2D and 3D layouts cases

In the future:

- More work needs to be done to improve the bundle creation algorithms for 3D layout
- Consideration of vias, solder ball array for 3D layout cases

Thank you !
Question ?

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