Hierarchical Layout Synthesis and Optimization Framework for High-Density Power Module Design Automation

Imam Al Razi[1], Quang Le[2], H. Alan Mantooth[2], Yarui Peng[1]

Computer Science and Computer Engineering Department[1]

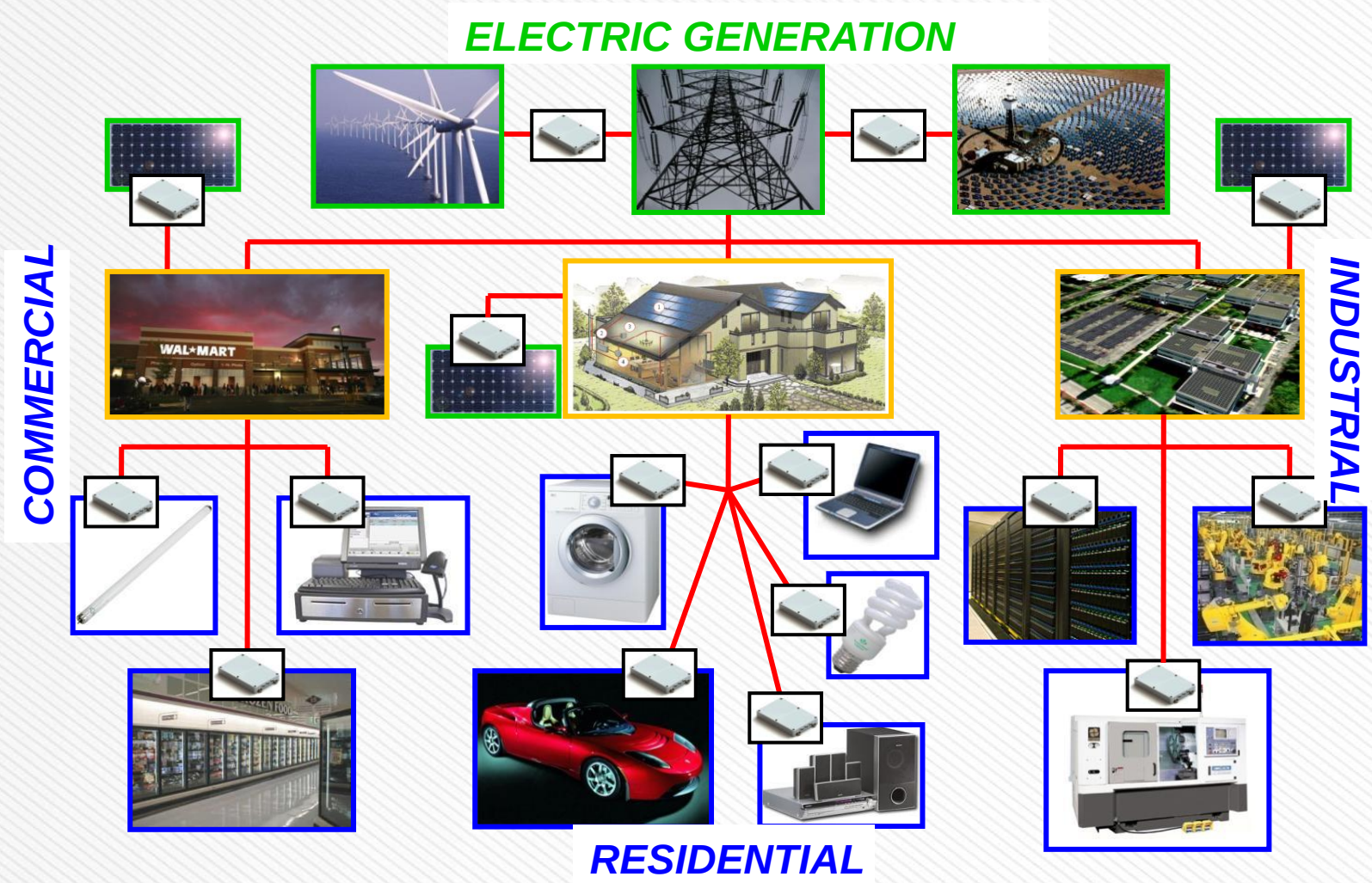
Electrical Engineering Department[2]

University of Arkansas, Fayetteville, AR, US

https://e3da.csce.uark.edu ialrazi@uark.edu +1 (479) 575-6043

Power Electronics is Everywhere

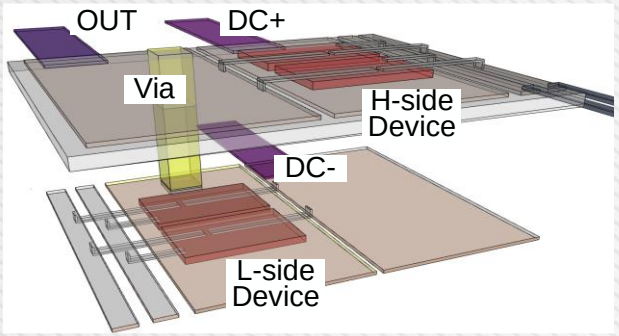
- Electric automobiles
- Aircrafts
- Smart grid
- Consumer electronics
- .....



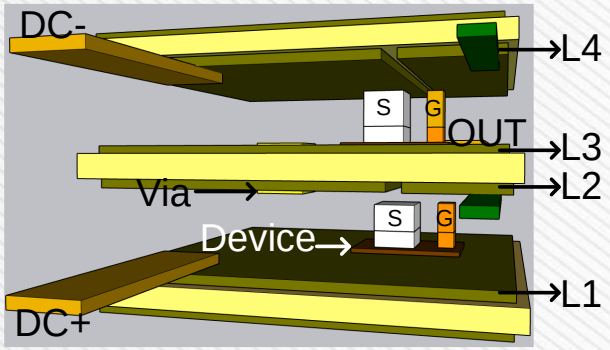
Power converters are essential parts of power systems

Multi-Chip Power Modules

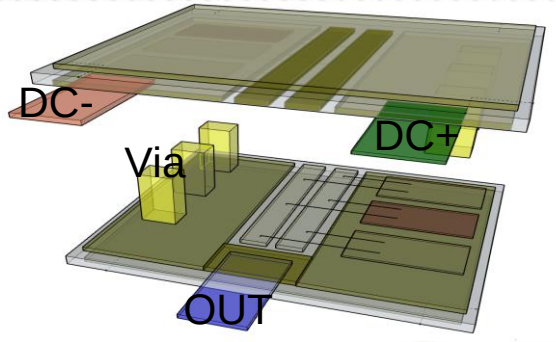
- **Foundation element of power converters**
- **Integrates power devices and control circuitry in a single package**
- **Wide Bandgap Devices (SiC/GaN)**
  - Increased power density
  - New packaging technologies
  - Heterogeneous integration



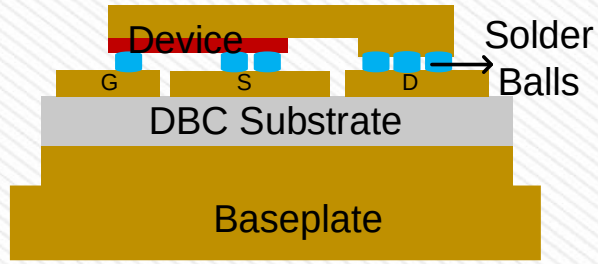
Wire-bonded 3D



Wire bondless 3D



Hybrid 3D



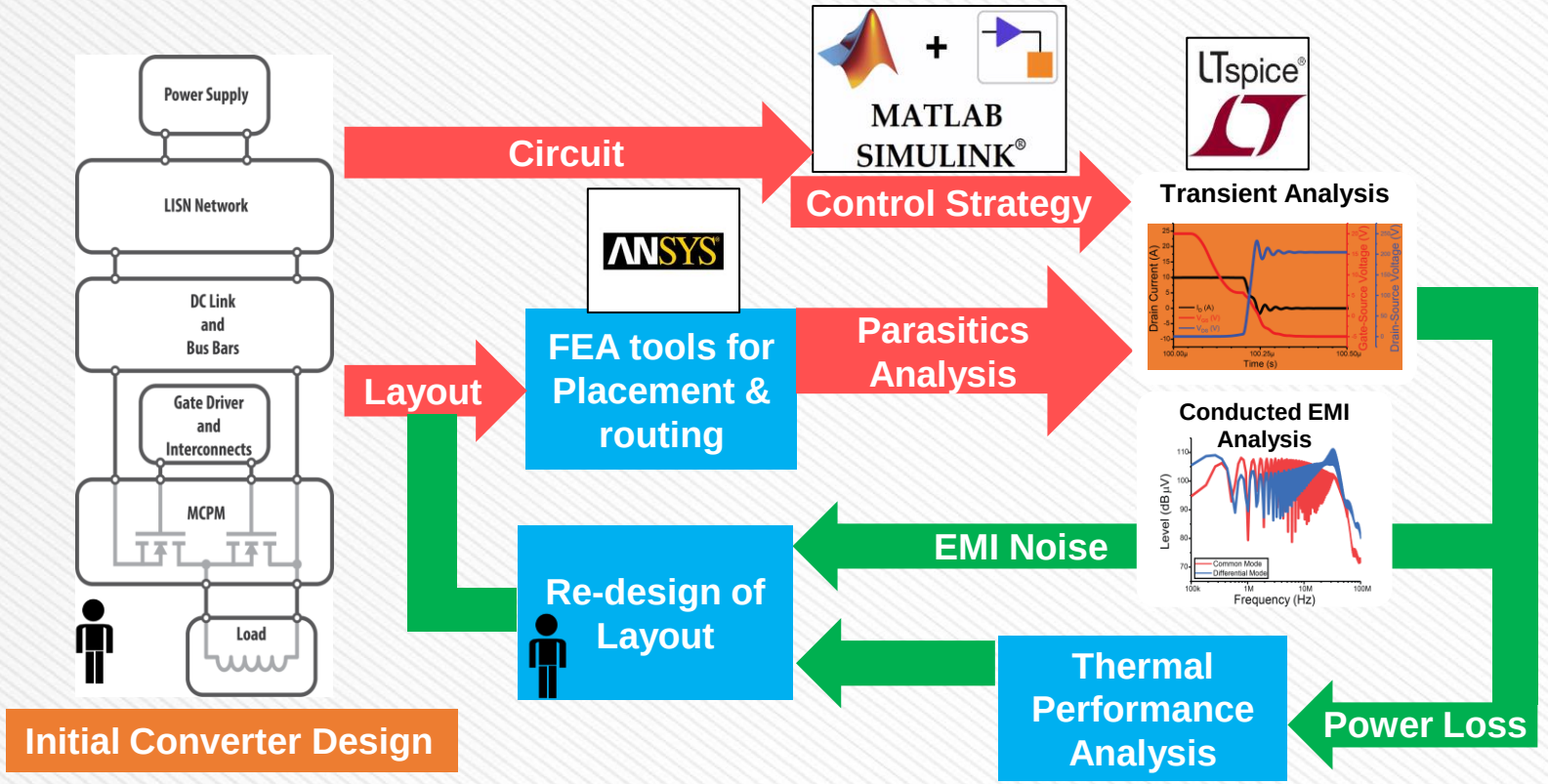
Flip-chip Module

MCPM layout design complexity is increasing

UNIVERSITY OF ARKANSAS

Traditional Design Flow

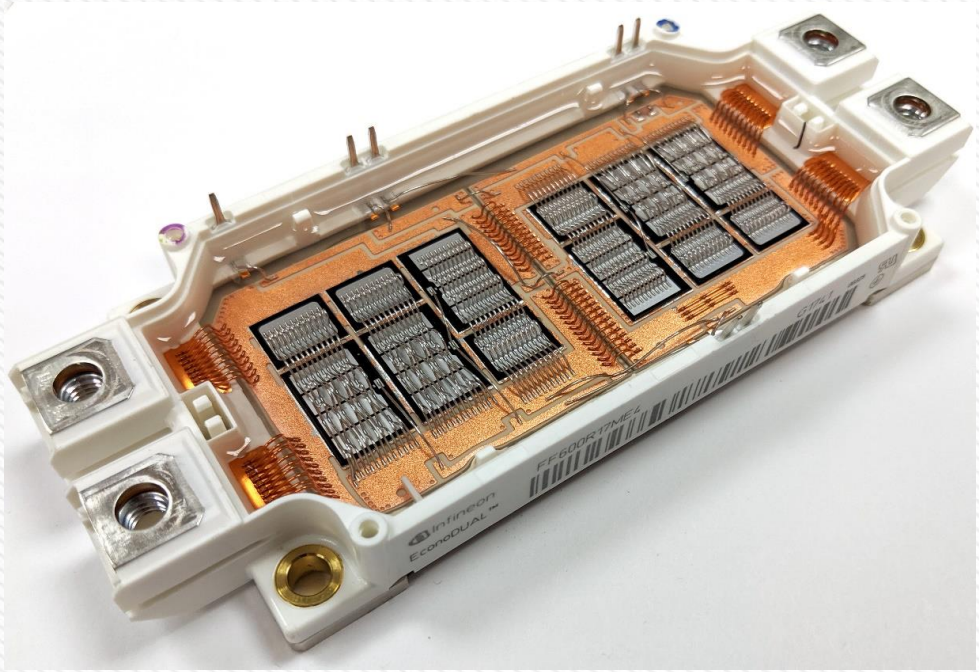
- **Typical power electronics design flow:**
  - **Manual, iterative, and computationally expensive**
  - **Single solution at a time**
  - **Multiple conflicting aspects**
    - Electrical
    - Thermal
    - Mechanical
  - **Requires human expertise**



No quick turnout solution flow

Automation in MCPM Design

- **Electronic design automation (EDA) tool can**
  - Overcome the limitations with the manual approach
  - Reduce both engineering time and cost
  - Handle multi-objective optimization
- **Requirements:**
  - Capability of producing layout solutions
    - Manufacturable
    - Reliable
    - Electro-thermo-mechanically optimized
  - Ability to export
    - Commercially available 3D FEA tools
    - Parasitic netlist for circuit simulation

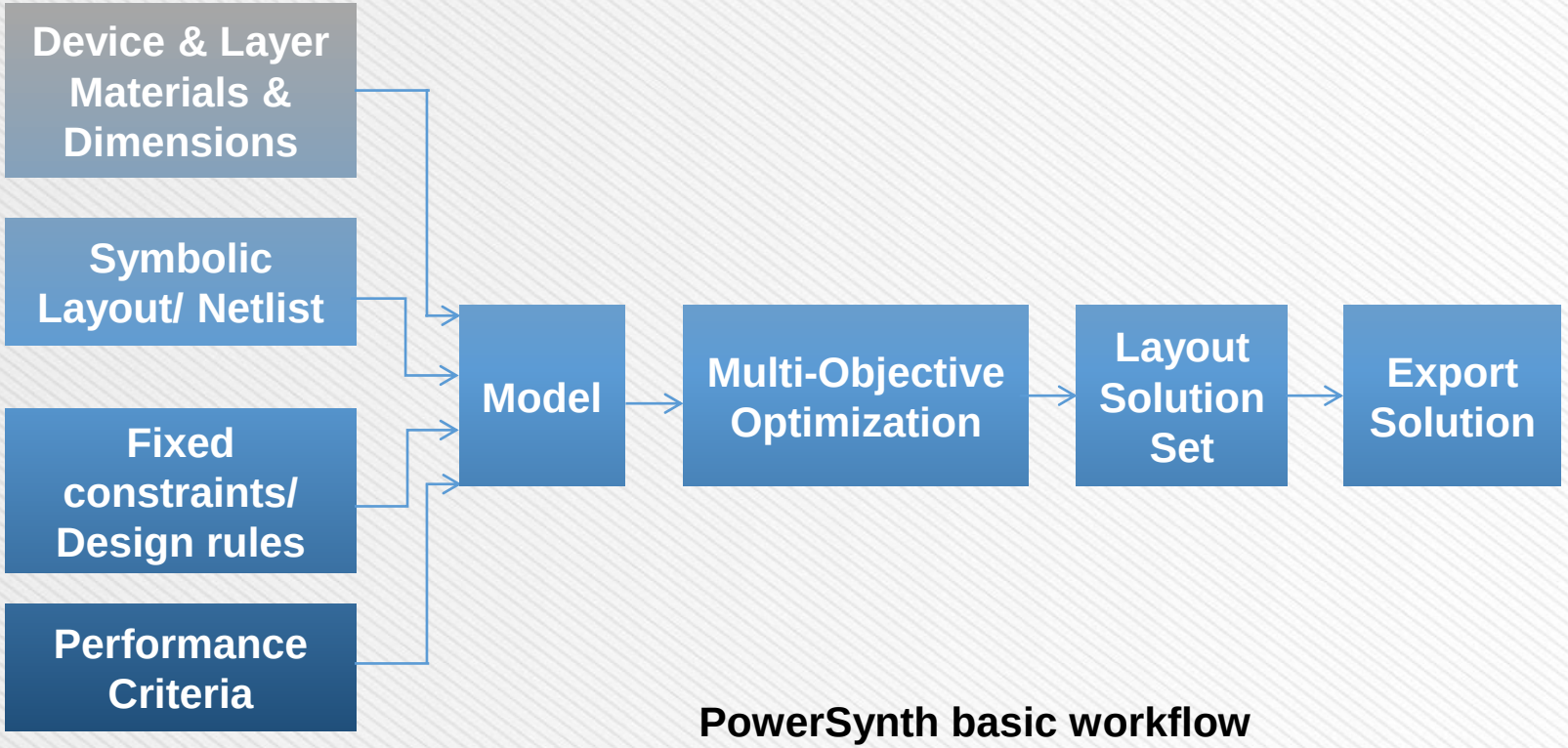


Commercial half-bridge power module

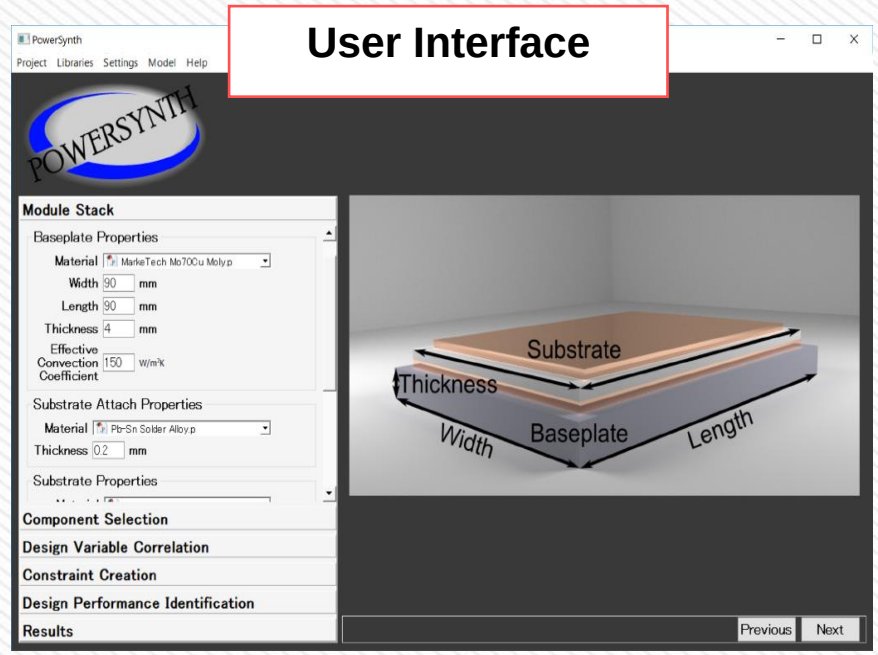
EDA tool can bridge the gap between circuit design and physical design

Layout Synthesis and Optimization

- **PowerSynth: An EDA tool with the goal streamlining the MCPM design process in a multi-objective optimization framework.**



PowerSynth basic workflow



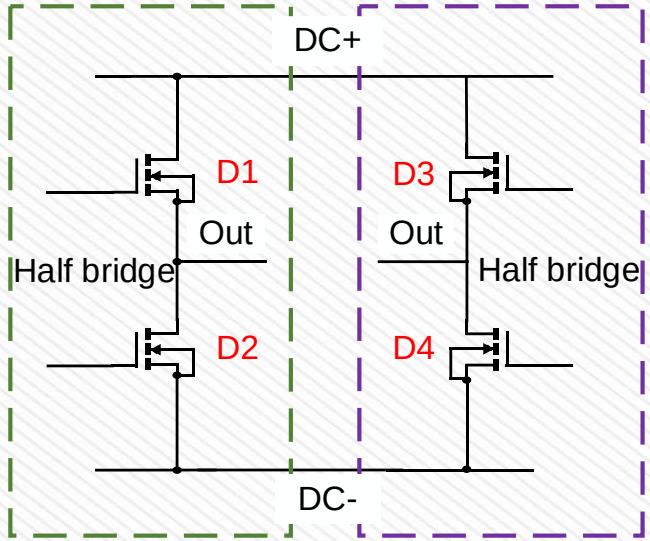
T. M. Evans *et al.*, "PowerSynth: A Power Module Layout Generation Tool," in *IEEE Transactions on Power Electronics,2019* (Highlighted paper)

UNIVERSITY OF ARKANSAS

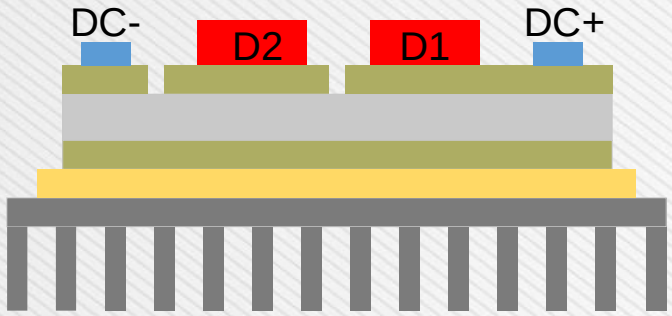
2D-2.5D-3D Layout Definition

❑ Definition under PowerSynth scope:

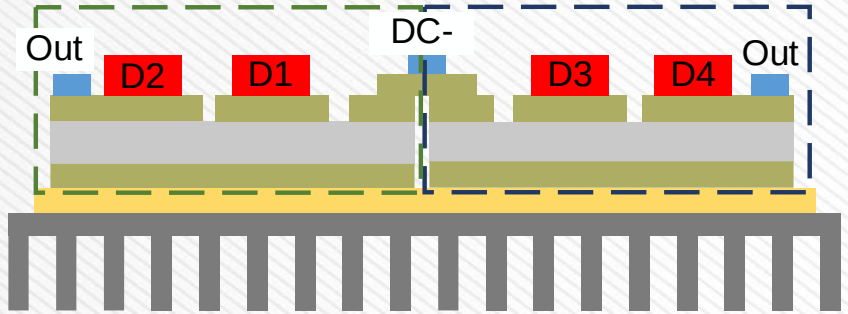
- 2D layout: Single substrate with one device layer
- 2.5D layout: Multiple substrates connected horizontally
- 3D layout: Multiple substrates stacked vertically



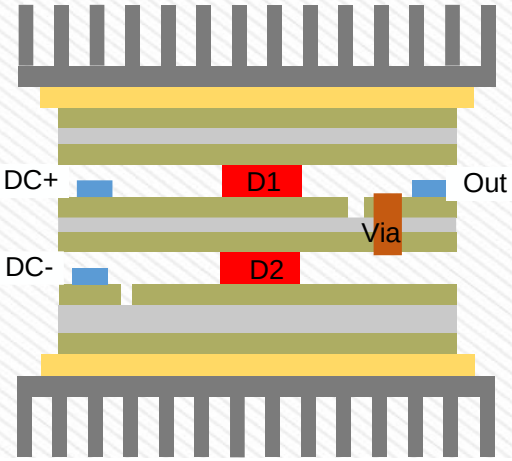
Circuit schematic of a full-bridge module



2D Half-bridge power module



2.5D Full-bridge power module



3D half-bridge power module

PowerSynth Progression

PowerSynth Development History

Release Webpage:
https://e3da.csce.uark.edu/release/PowerSynth/

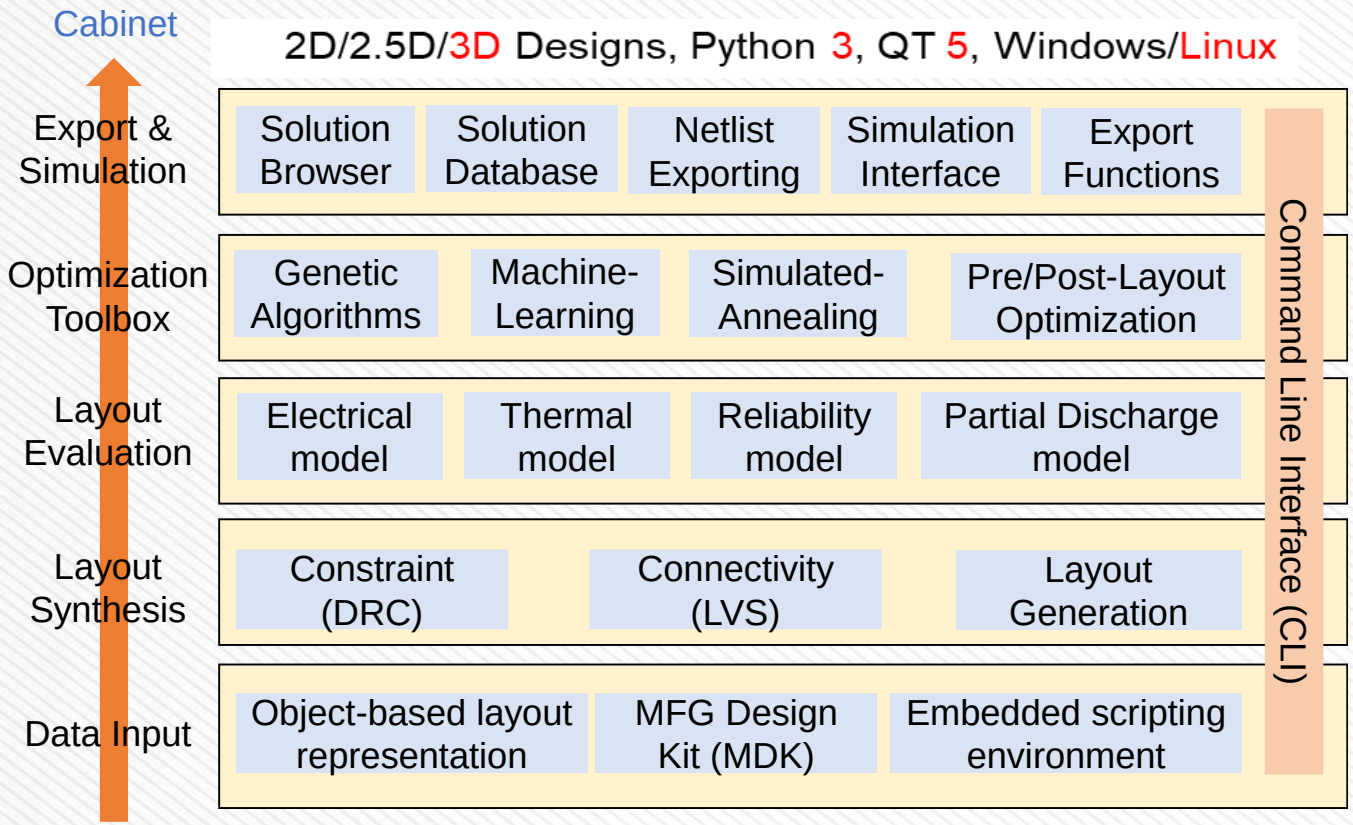
- **Features**

▪ Simple 2D layouts ▪ Symbolic layout representation ▪ Matrix-based layout engine ▪ Iterative DRC-checking	PS v1.1
▪ 2D layouts with complex geometry ▪ Constraint-aware, flat-level layout engine ▪ Heterogeneous components ▪ Multiple optimization techniques	PS v1.3/1.4
▪ All 2D/2.5D Manhattan geometries ▪ Hierarchical layout representation ▪ Hierarchical layout optimization ▪ Larger solution space ▪ Hardware-validated optimization result	PS v1.9

UNIVERSITY OF ARKANSAS

PowerSynth v2

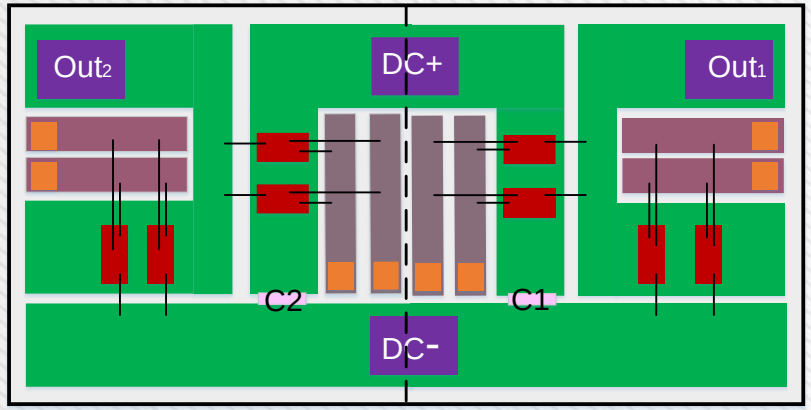
- **Data Input**
  - Hierarchical input script
  - Manufacturer Design Kit (MDK)
- **Layout Synthesis**
  - Generic, scalable, and efficient algorithms
  - 100% DRC-clean
- **Layout Evaluation**
  - Electrical/Thermal/Mechanical model
    - High-speed, reduced-order, accurate
  - Reliability optimization
- **Optimization Toolbox**
  - Multi-objective optimization
    - Different approaches
- **Export & Simulation**
  - Commercial CAD/FEA tools
  - Parasitic netlist



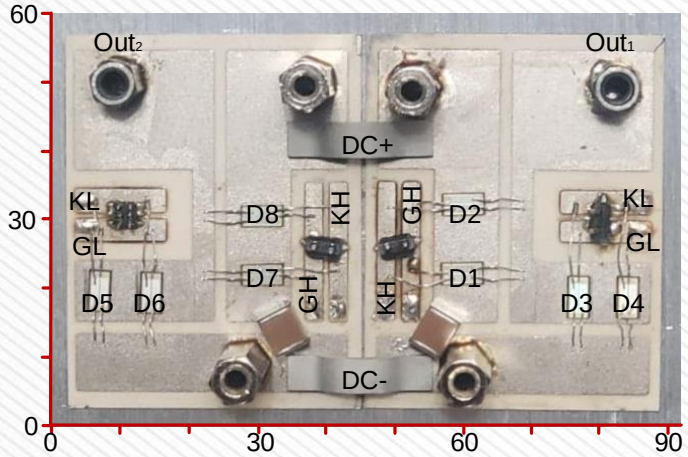
PowerSynth architecture (v2)

PowerSynth Optimization Result Validation

❑ 2.5D Full-Bridge MCPM Optimization



Initial layout



Fabricated optimized design

- **Electrical performance validation**
  - Metric: Power loop inductance

Source	Ringing Freq.	Inductance
PowerSynth	86.0 MHz	8.54 nH
Measurement	89.4 MHz	8.70 nH

- **Thermal performance validation**
  - Metric: Maximum junction temperature

Case	Maximum Temperature (K)				Temp. Rise Diff.
	D1	D2	D3	D4	
Measurement	416.8	416.5	427	427.7	-
ANSYS	418.9	416.8	422.4	422.9	-3.57%
PowerSynth	418	417.9	418.3	418.5	-7.15%

Imam Al Razi et. al., "PowerSynth Design Automation Flow for Hierarchical and Heterogeneous 2.5D Multi-Chip Power Modules", IEEE Transactions on Power Electronics, vol. 36, no. 8, pp. 8919-8933, 2021.

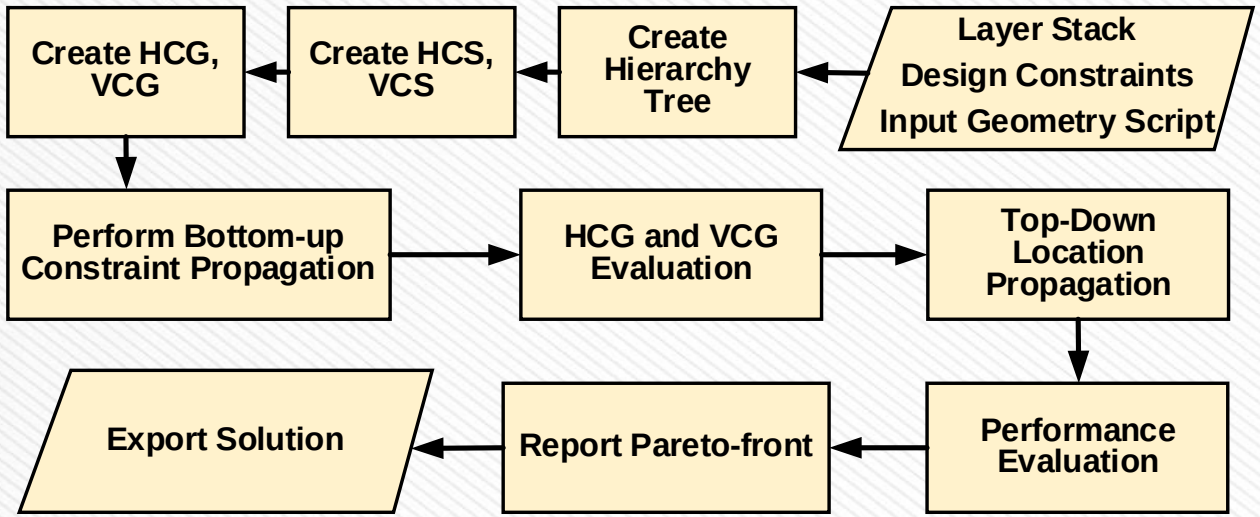
Methodology

❑ Input Layout

- Hierarchical input geometry script
- Manufacturer Design Kit (MDK)

❑ Layout Engine

- Hierarchical corner stitch tree
  - Horizontal (HCS) and Vertical (VCS)
- Hierarchical constraint graph:
  - Horizontal (HCG) and Vertical (VCG)
- Built-in randomization algorithm
- Generic rigid constraint handling
- Generic connection handling



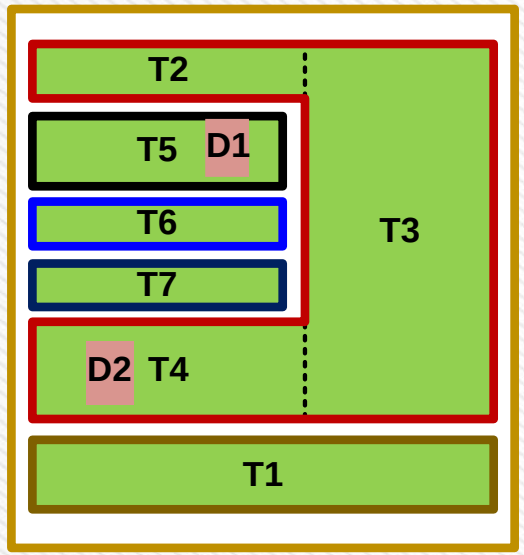
High-level workflow

❑ Multi-Objective Optimization

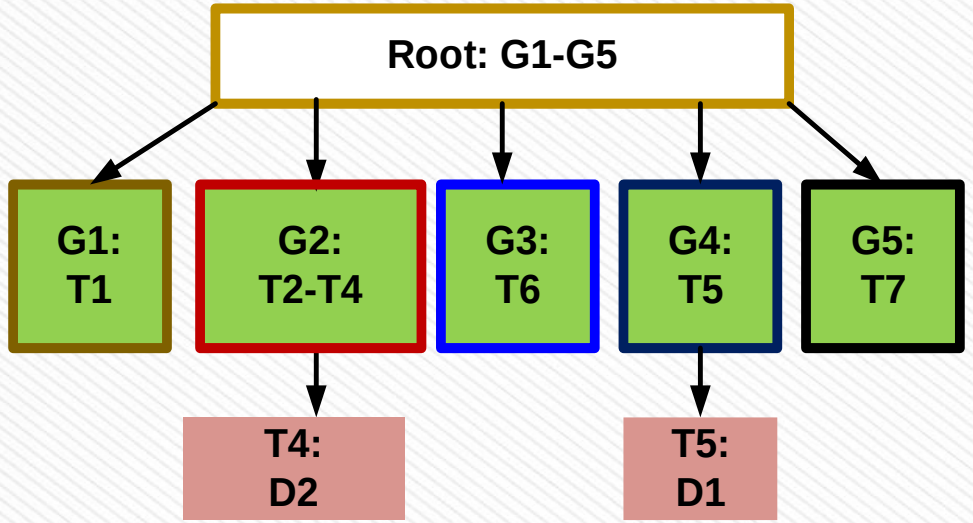
- Genetic algorithm
- Performance evaluation models: Electrical, Thermal

Hierarchical Corner Stitch

- **Tree structure is maintained to preserve component hierarchy**
  - **Tree structure construction:**
    - The root is the initial empty tile (substrate rectangle).
    - All components are inserted in a group-wise manner.
    - Two types of tile in each node: parent (background tile) and children (foreground tile).
  - **Two tree for each layout: HCS tree and VCS tree**
  - **In the example:**
    - All traces are in the root.
    - T2,T3, and T4 are connected → Same group.
    - D1 is placed on T5, that makes D1 child and T5 parent.



2D power module Layout

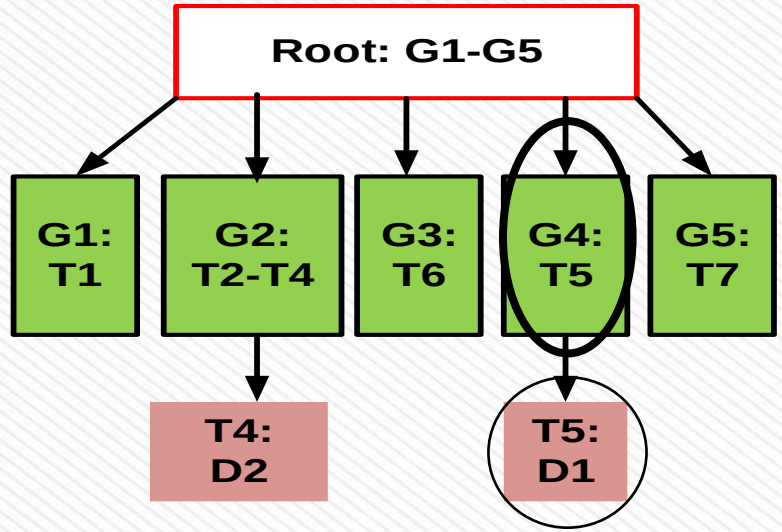


Tree Structure

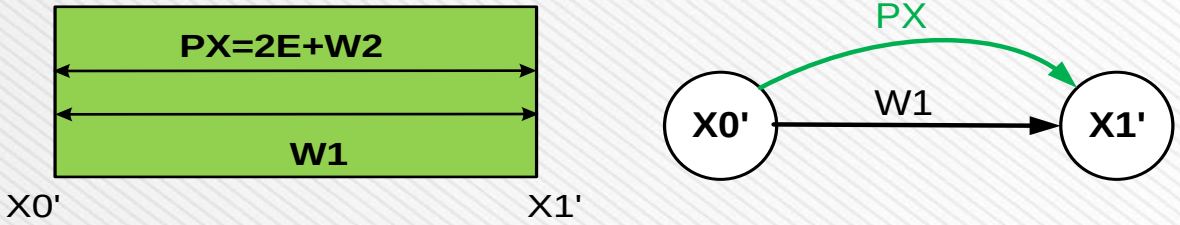
UNIVERSITY OF ARKANSAS

Hierarchical Constraint Graph

- **Each node in the tree → Constraint graph**
  - Mapping of the design constraints
- **Example**
  - From the tree, G4 (parent) and T5:D1 (child), hierarchical horizontal constraint graph is shown:



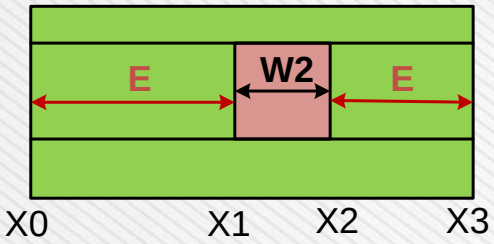
Tree Structure



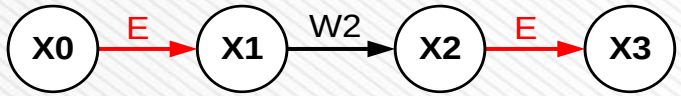
Parent Node

Child Node

W2= min width of device (Child Node)
W1= min width of trace (Parent Node)

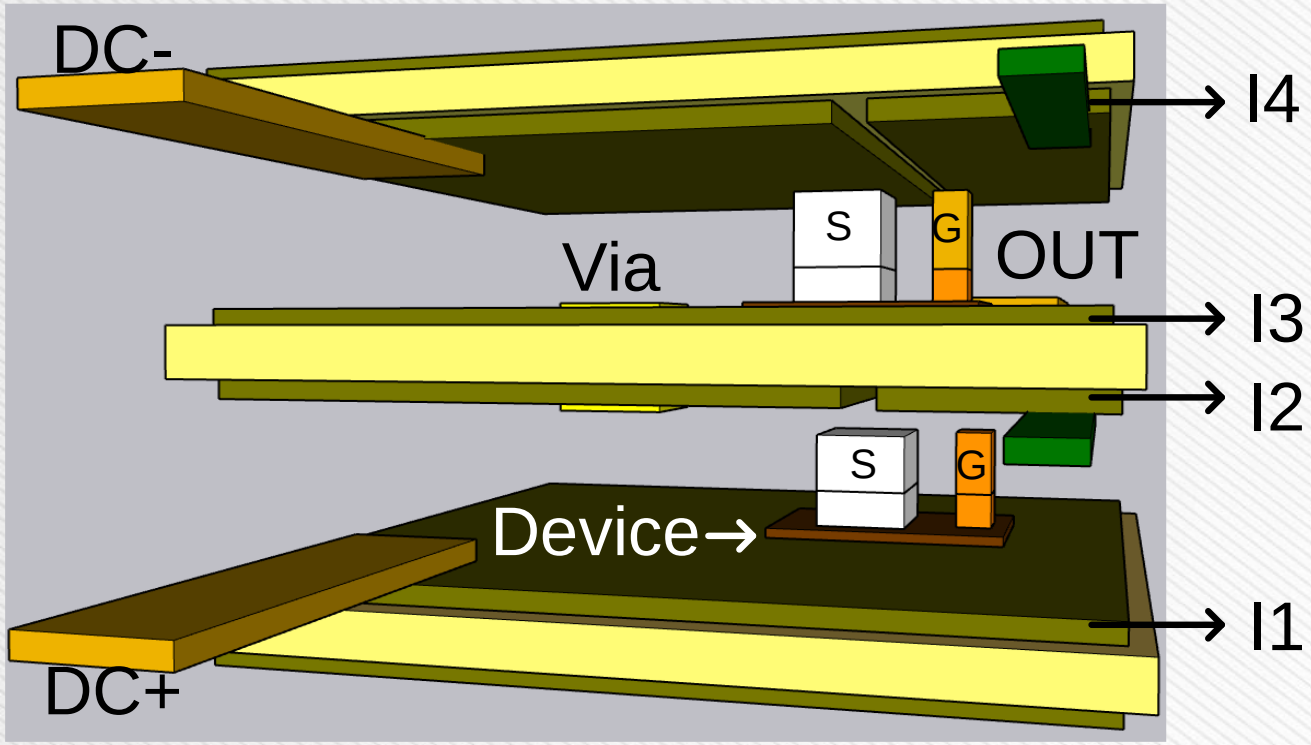


PX = Longest path from X0 to X3

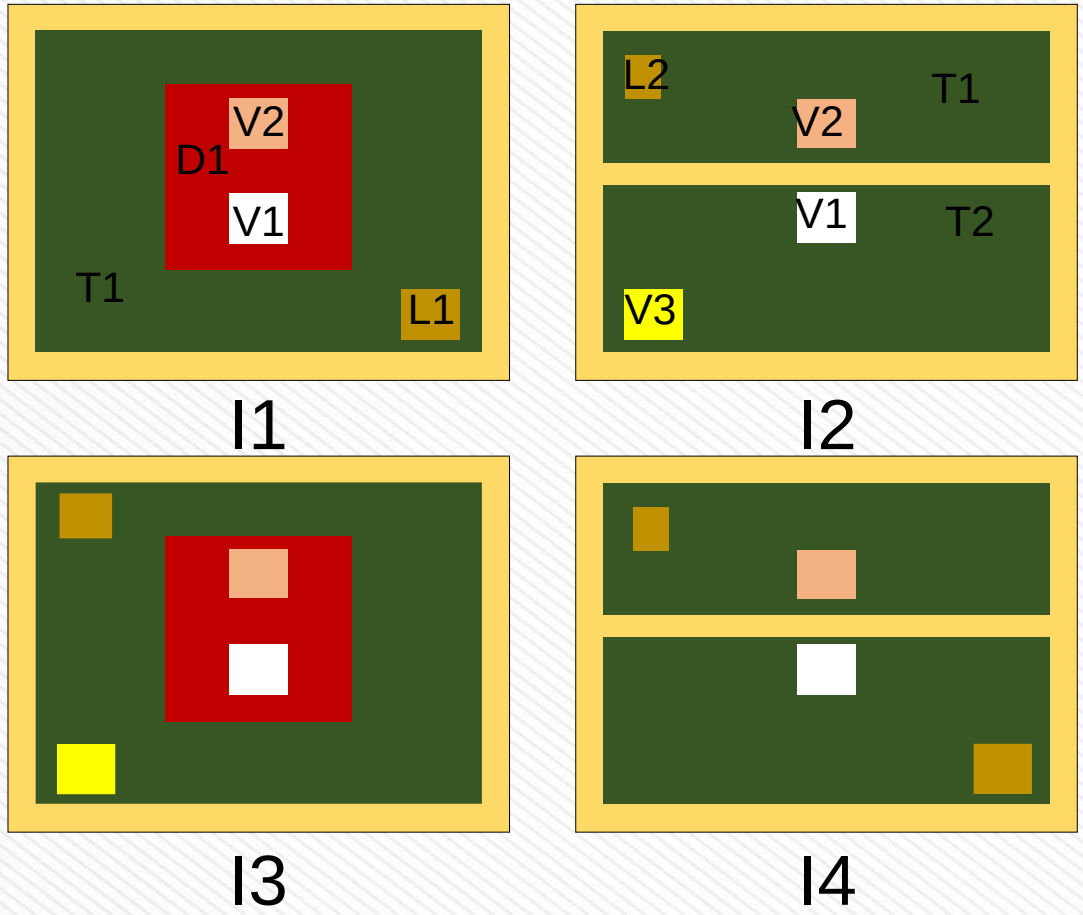


UNIVERSITY OF ARKANSAS

Input Layout

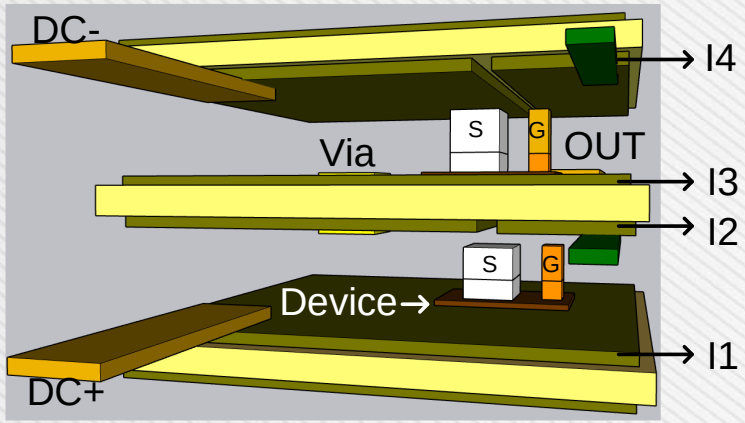


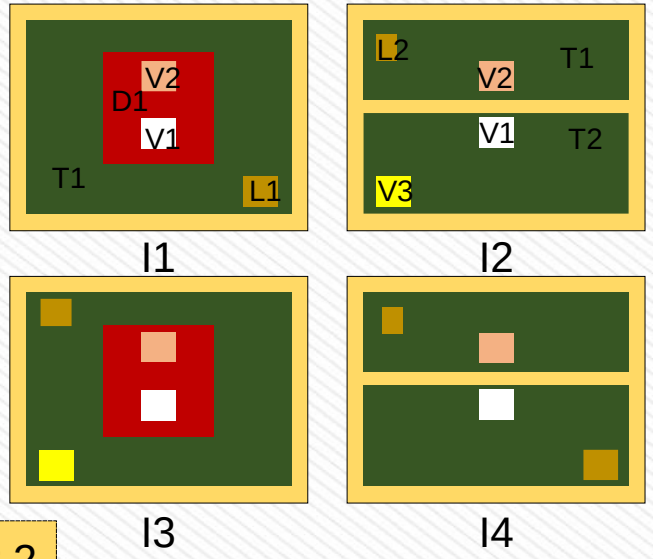
3D wire bondless half-bridge module

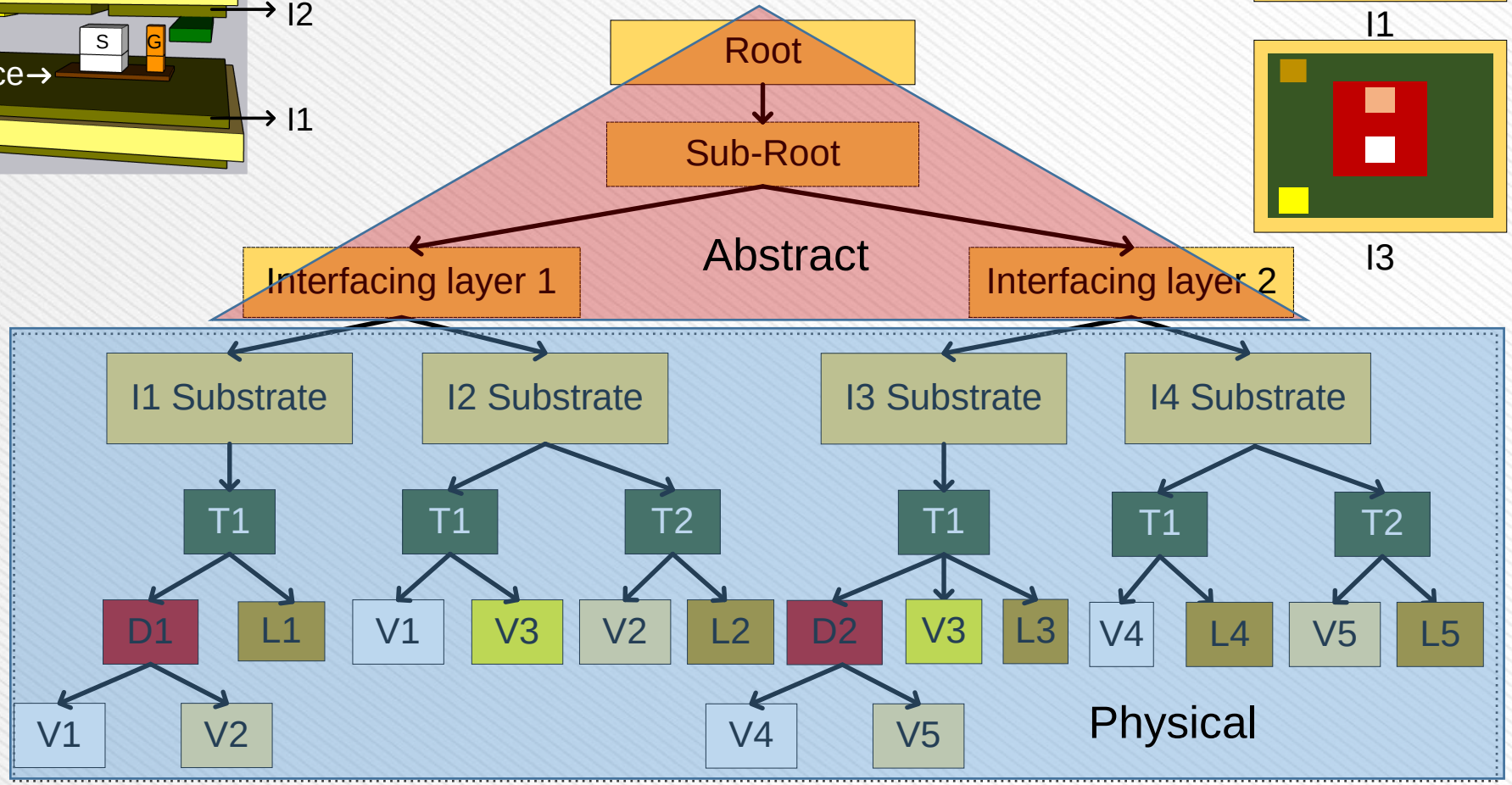


2D layout of each layer

Input Layout Hierarchy

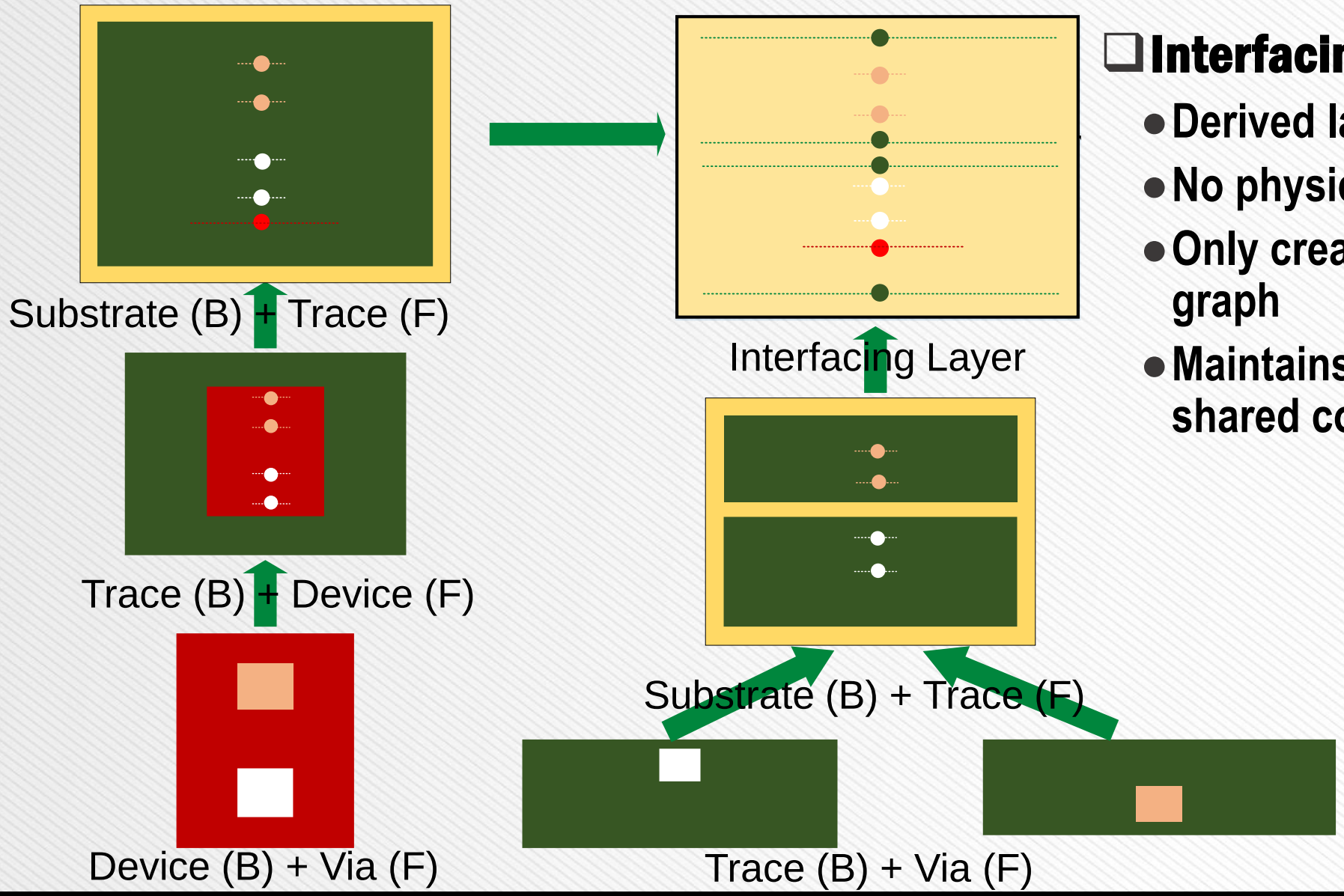






UNIVERSITY OF ARKANSAS

Hierarchy Tree Creation

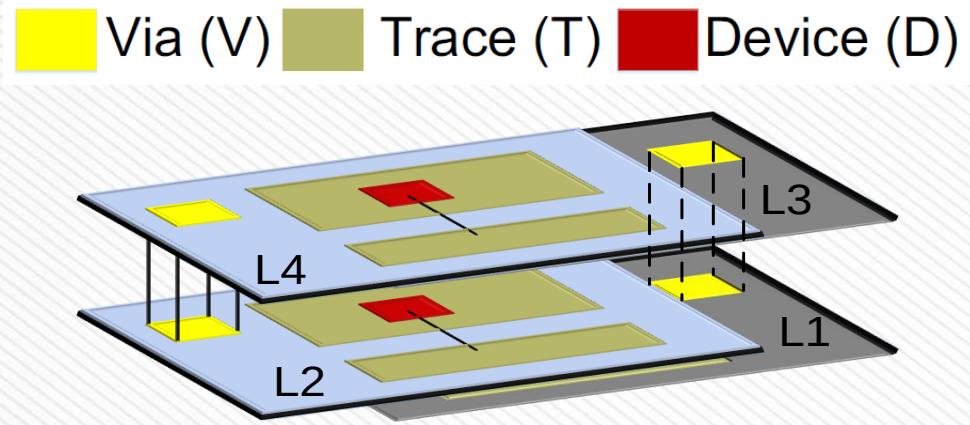


- **Interfacing layer**
  - Derived layer from it's child nodes
  - No physical existence
  - Only created in the constraint graph
  - Maintains constraints among shared components of child nodes

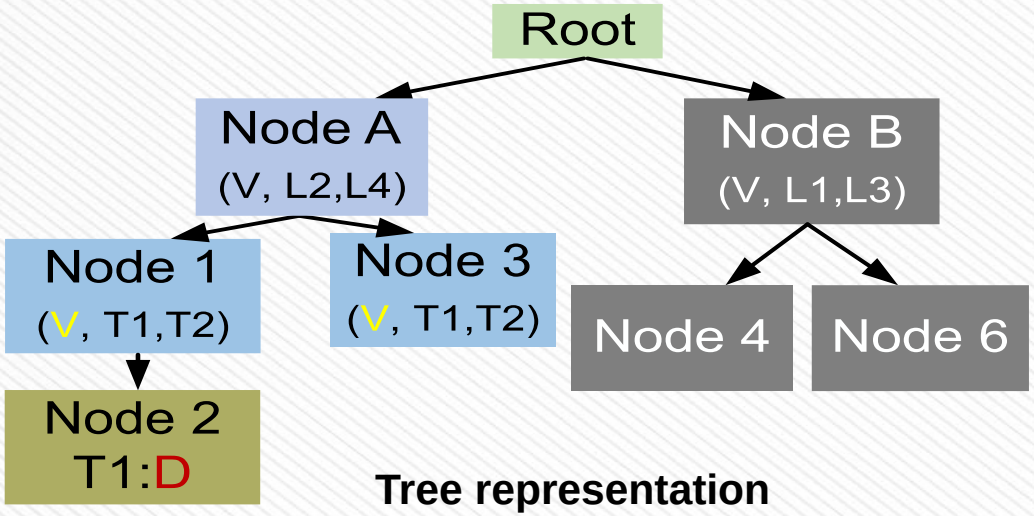
Layout Generation

❑ High-level steps:

```
1   Read Input Script
2   Create a root node
3   Create group of layers connected with same via

4   For each via connected group
5     Create a sub-root
6     For each layer
7        Create HCS, VCS
8        Create and Evaluate HCG, VCG
9   For each ancestor from leaf to root
10    Perform bottom-up constraint propagation

11  Evaluate root node and compute available space

12  For each sub-tree from root to leaf
13    Perform top-down location propagation

14  Evaluate independent nodes
```



Sample 3D structure

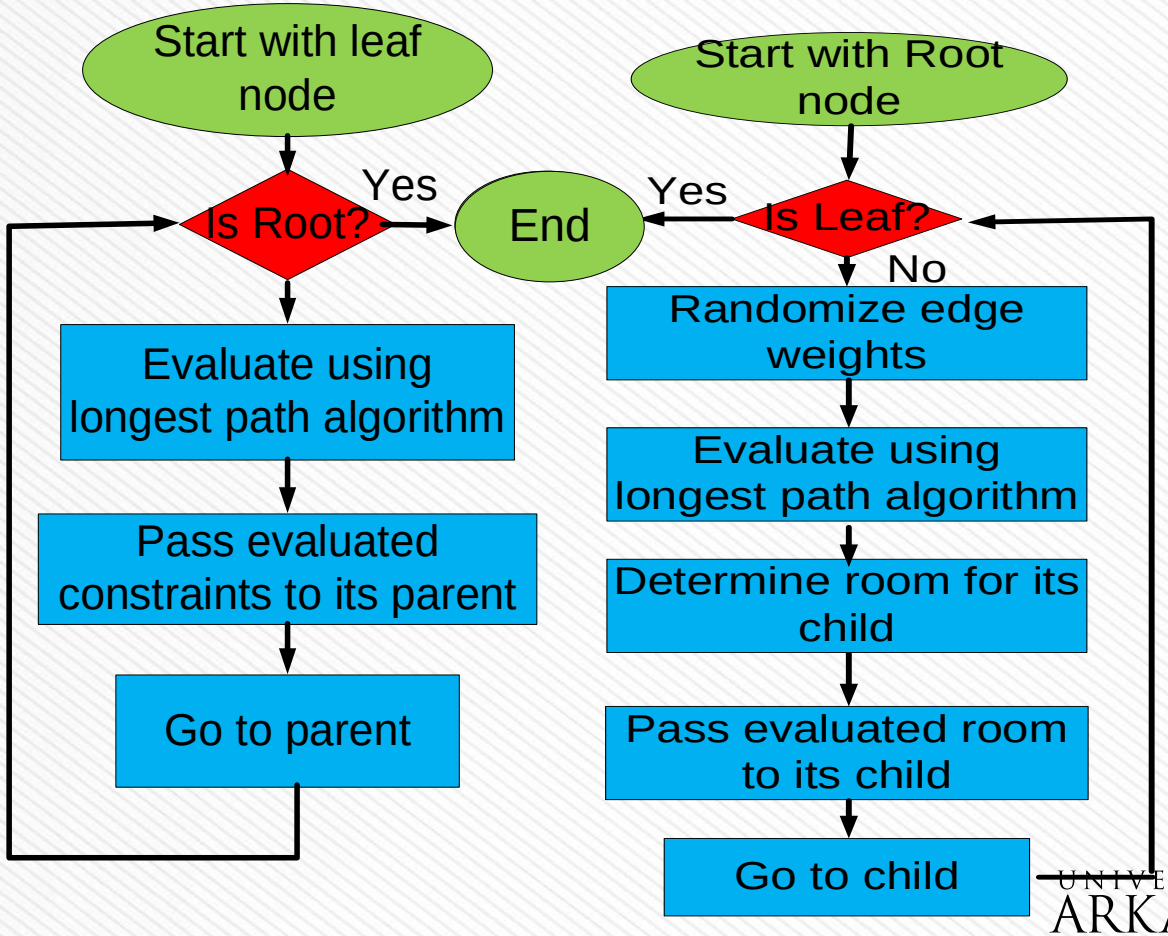


Tree representation

Constraint Propagation and Evaluation

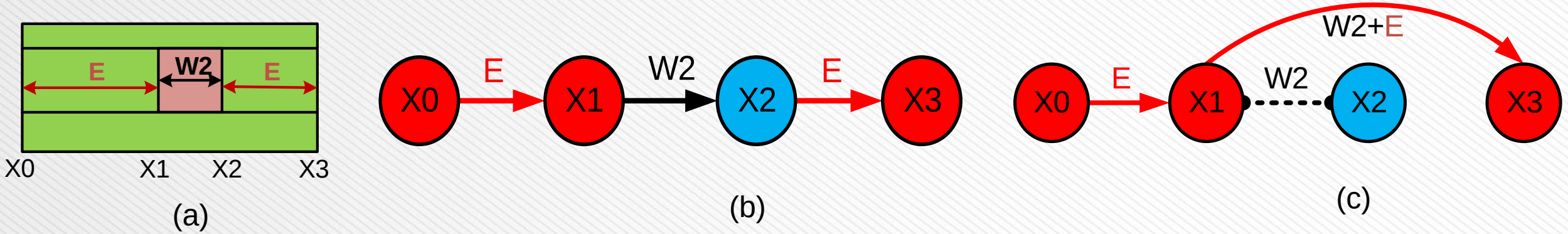
- **Each constraint graph is evaluated using longest path algorithm.**
- **The evaluated constraints are propagated in a bidirectional manner.**

- **Bottom-up constraint propagation**
  - Propagates from leaf towards root
  - Evaluated minimum constraints
  - Ensures room for child component
- **Top-down location propagation**
  - Starts on arrival of all minimum constraint values in the root
  - Root node evaluation can generate three types of solutions:
    - Minimum-sized
    - Variable-sized
    - Fixed-sized
  - Propagates from root towards child
  - Shared vertices locations are propagated



Rigid Constraints Handling

- **Two types of edges:**
  - Rigid edge: Having fixed (constant) weight (●·····●)
  - Flexible edge: weight can be varied (⟶)
- **Two types of vertices:**
  - Independent: locations are randomized independently. (●)
  - Dependent: all incoming or outgoing edges are rigid edges. (●)

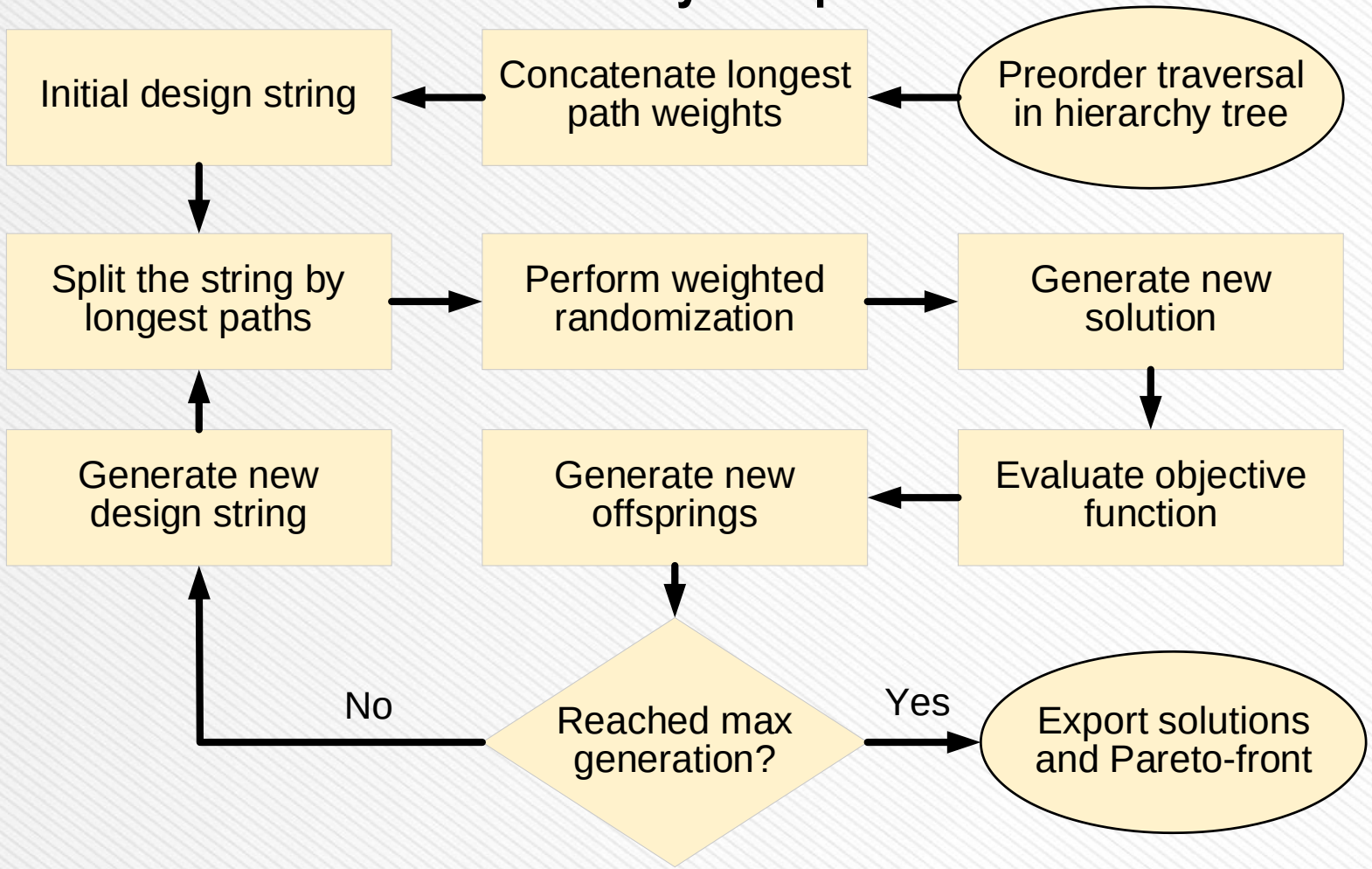


(a) Horizontal corner-stitched layout of a trace with a device, (b) HCG of the layout in (a), (c) Modified HCG : after bypassing dependent vertex

Genetic Algorithm Workflow

❑ Non-dominated Sorting Genetic Algorithm II (NSGAII)

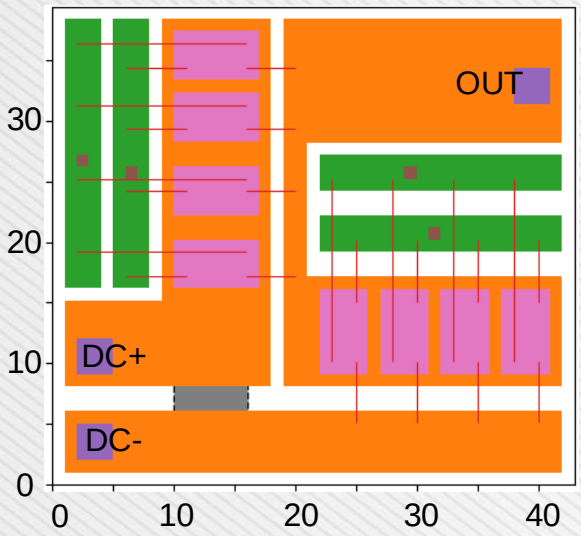
- Customized flow for 2D/2.5D/3D MCPM layout optimization



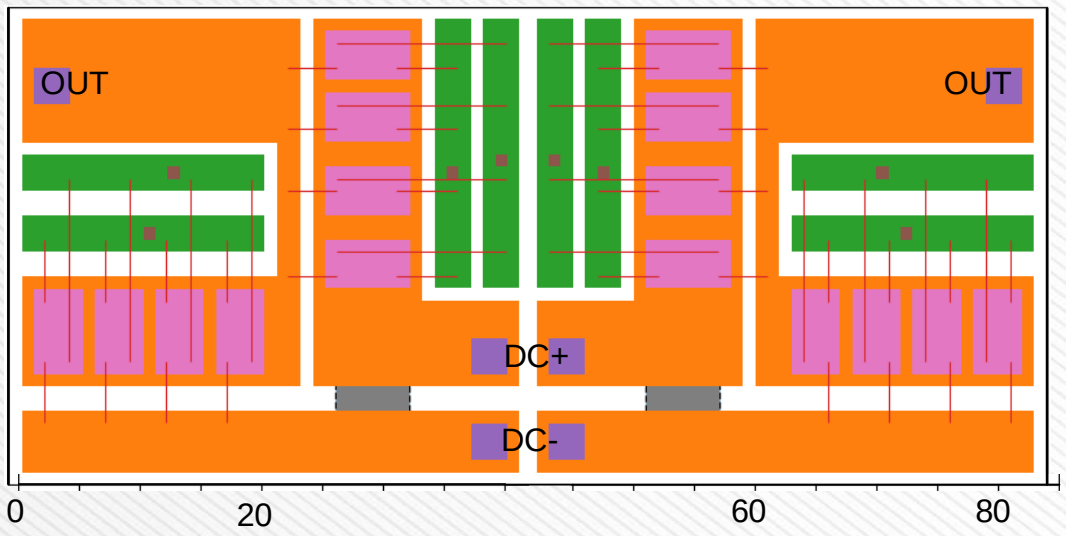
Results

❑ 2D/2.5D/3D Layout Solutions

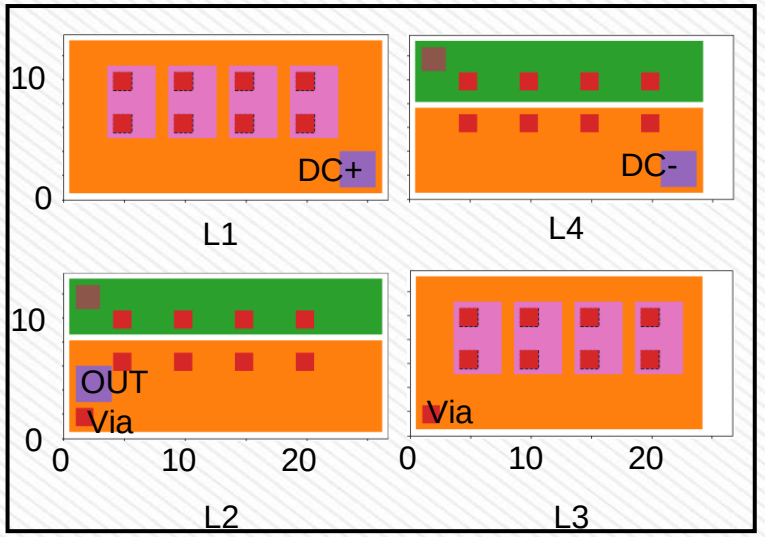
- Minimum-sized solutions
- Heterogeneous 2D/2.5D design
- Power loop inductance 2.11 nH (3D) vs 7.12 nH (2.5D/3D)



2D MCPM
(43 mm × 38.4 mm)



2.5D MCPM
(84 mm × 38.4 mm)



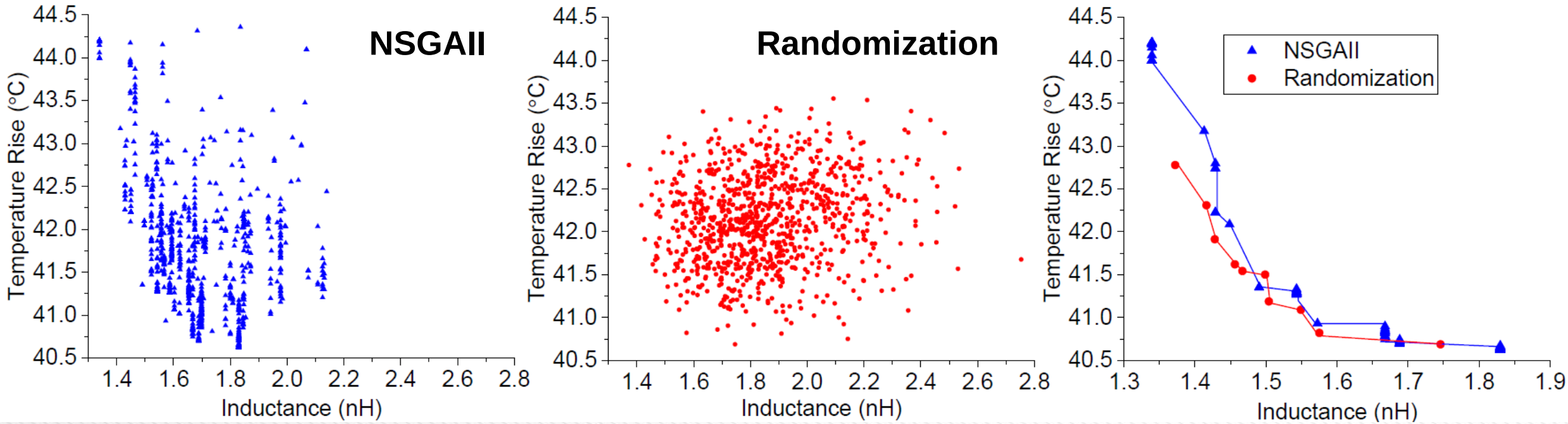
3D MCPM
(26.7 mm × 13.7 mm)

UNIVERSITY OF ARKANSAS

NSGAII vs Randomization

❑ Runtime comparison

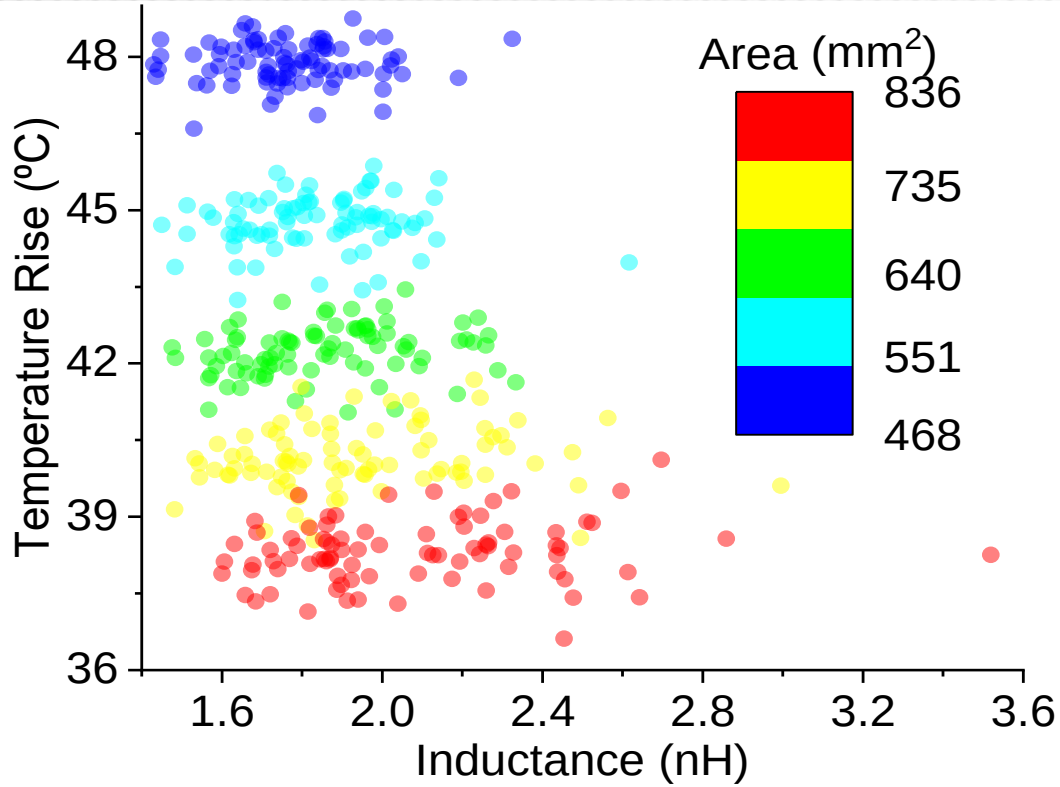
Algorithm	Total Layouts	Approximate runtime(min)		On Pareto-front
		Generation	Evaluation	
NSGAII	937	25	206	148
Randomization	937	1	212	10



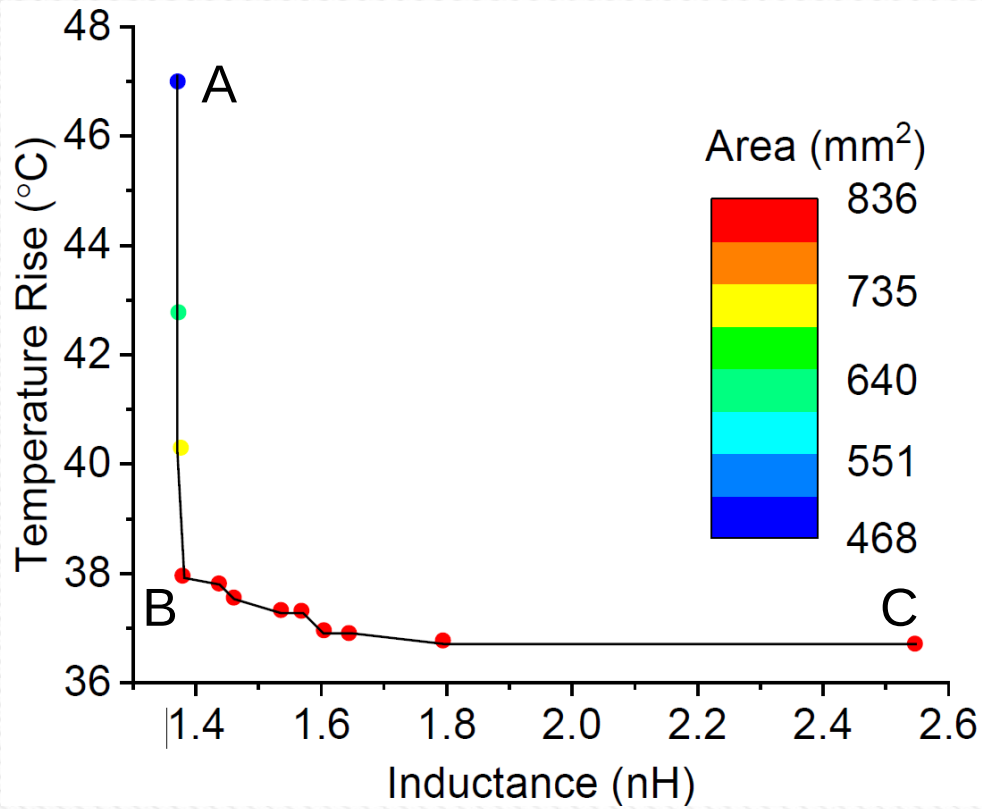
K. D. et al., "A Fast and Elitist Multiobjective Genetic Algorithm: NSGA-II," IEEE Transactions on Evolutionary Computation, vol. 6, no. 2, pp. 182–197, Apr 2002

Optimization Results

- **Electro-thermal optimization**
  - 5 floorplan sizes (85 solutions/size)
  - FastHenry electrical model + ParaPower thermal model



Complete solution space

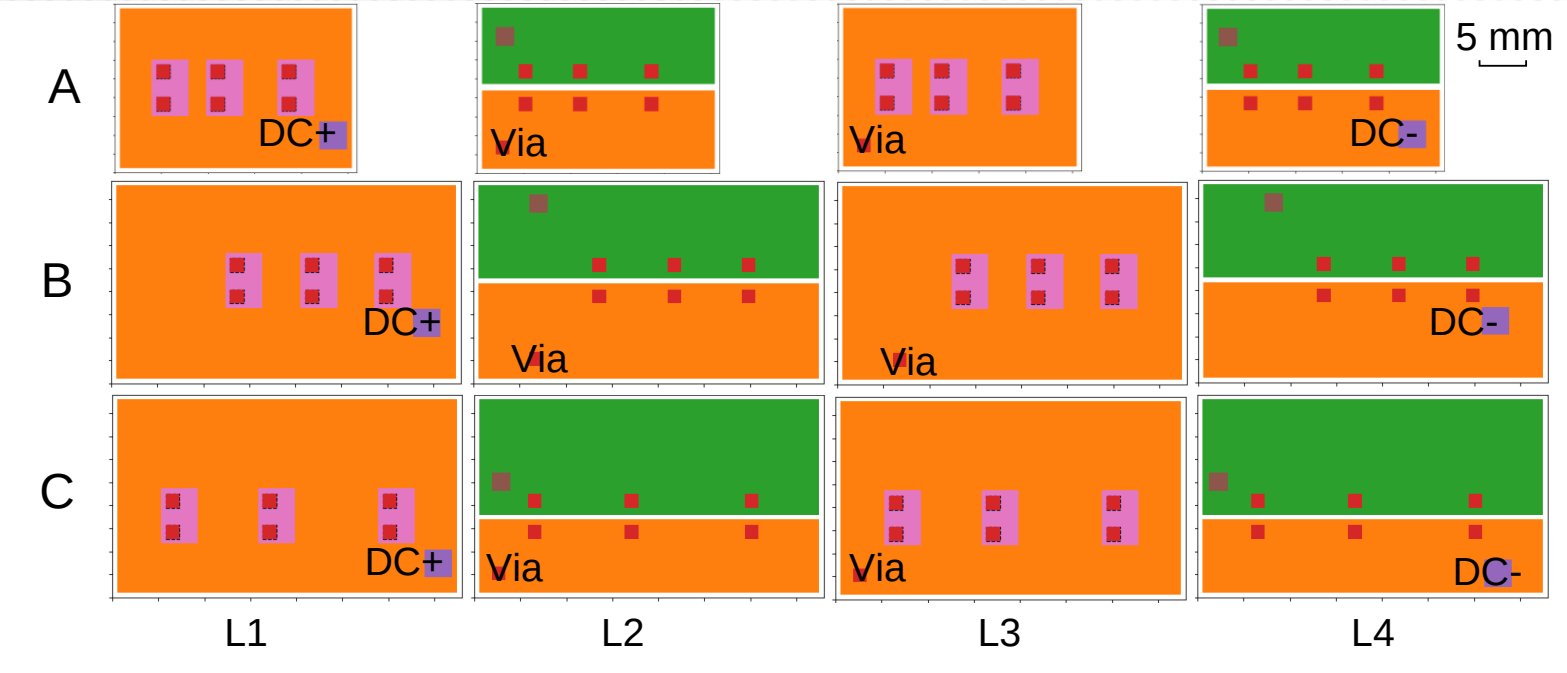


Pareto-front

ARL ParaPower, "https://github.com/USArmyResearchLab/ParaPower".

Pareto-Front Solutions

❑ Three selected solution layouts



Performance metrics

Layout ID	Inductance (nH)	Temperature Rise (ºC)	Size (mm × mm)
A	1.37	46.99	26 ×18
B	1.37	37.96	38 × 22
C	2.54	36.72	38 × 22

Conclusions and Future Work

❑ Conclusions

- PowerSynth is a power module layout synthesis and optimization framework promising for design automation in the power electronics industry.
- The capability to optimize all 2D/2.5D/3D power modules reaches state-of-the-art.
- The generic, scalable, and efficient algorithms can adapt to most existing packaging technologies in the industry.
- The current version relies on external tools and models, resulting in a relatively long performance evaluation runtime.

❑ Future Work

- Implement built-in, reduced-order 3D performance evaluation models
- Apply parallel processing for performance evaluation
- Validate 3D MCPM optimization results through hardware validation.

UNIVERSITY OF ARKANSAS

Thank You!

UNIVERSITY OF ARKANSAS

https://e3da.csce.uark.edu ialrazi@uark.edu +1 (479) 575-6043