PowerSynth-Guided Reliability Optimization of Multi-Chip Power Module

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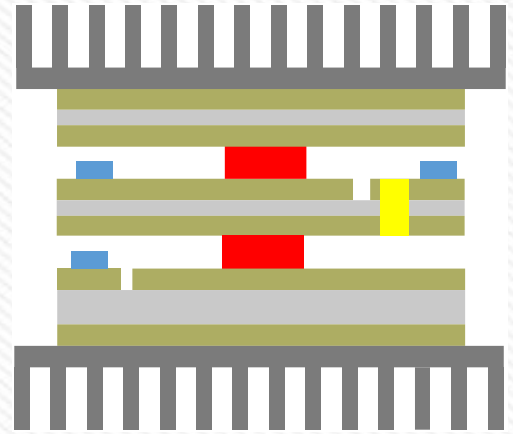
Outline

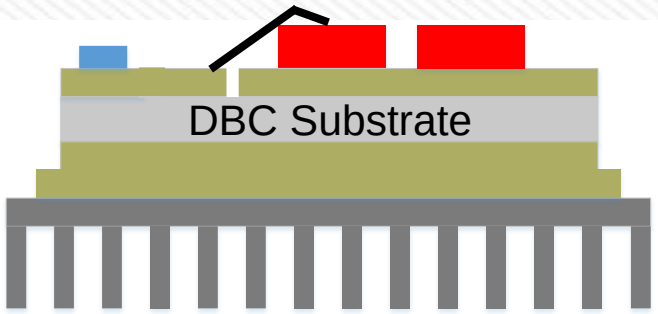
- **Overview**
  - Introduction to Design for Reliability
  - PowerSynth (an EDA tool) Introduction
- **Motivation**
- **Methodology**
  - Optimization Workflow
  - Transient Thermal Model
- **Results**
  - Model Validation
  - Optimization Case Study
- **Conclusions and Future Works**

Design for Reliability

- **2D/2.5D/3D Multi-Chip Power Module (MCPM)**
  - **Wide application in more-electric world**
  - **Innovative packaging technologies boost power density**
  - **Reliability optimization becomes increasingly challenging**
    - Varieties of materials with different CTE are combined
    - Critical components (e.g., solder joints, wire bond, substrate)
    - Thermal management is a challenge with new technologies
- **Two types of reliability optimization approaches:**
  - **Optimization aiming at specific failures**
    - Specific component and connection
    - Physic-based modeling + Finite Element Analysis (FEA)
  - **Optimization to reduce thermal cycling effects**
    - Full module layout
    - Layer stack material and structure



3D Half-Bridge Power Module



2D Half-Bridge Power Module

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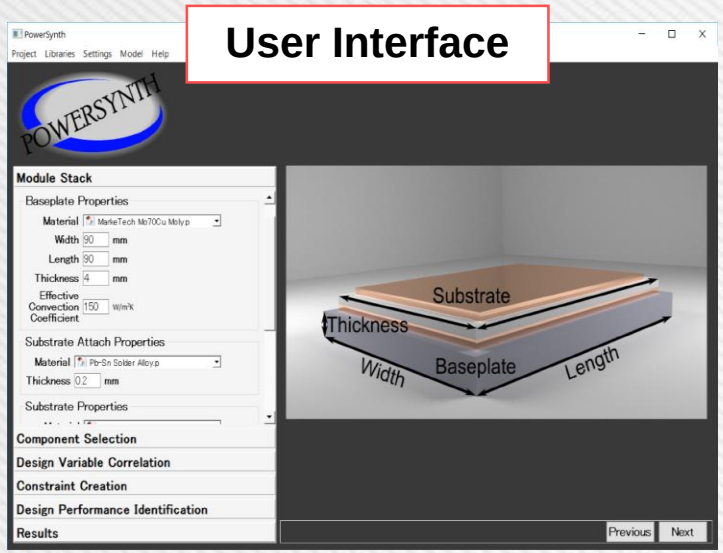
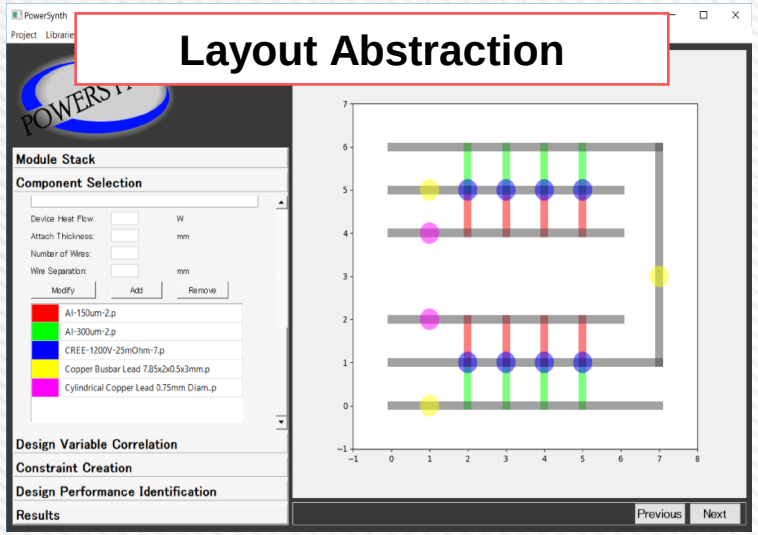
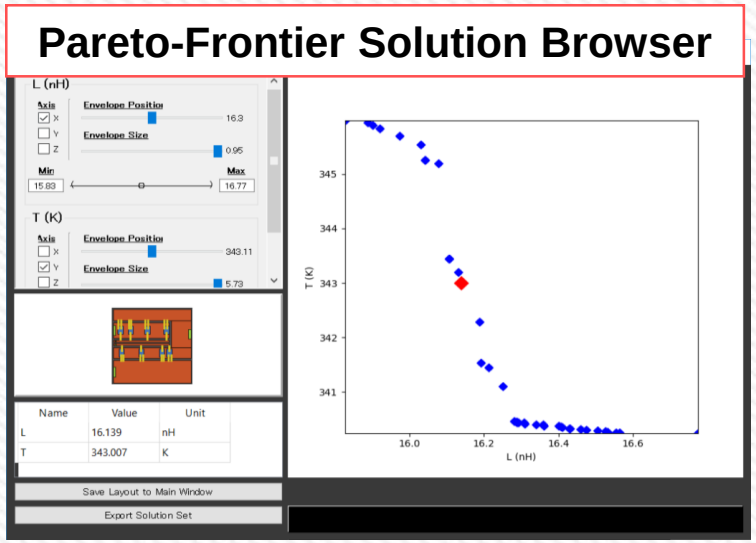
Layout Synthesis and Optimization

❑ PowerSynth

- A software tool for the design and layout of multi-chip integrated power modules







T. M. Evans *et al.*, "PowerSynth: A Power Module Layout Generation Tool," in *IEEE Transactions on Power Electronics,2019*.

PowerSynth Overview

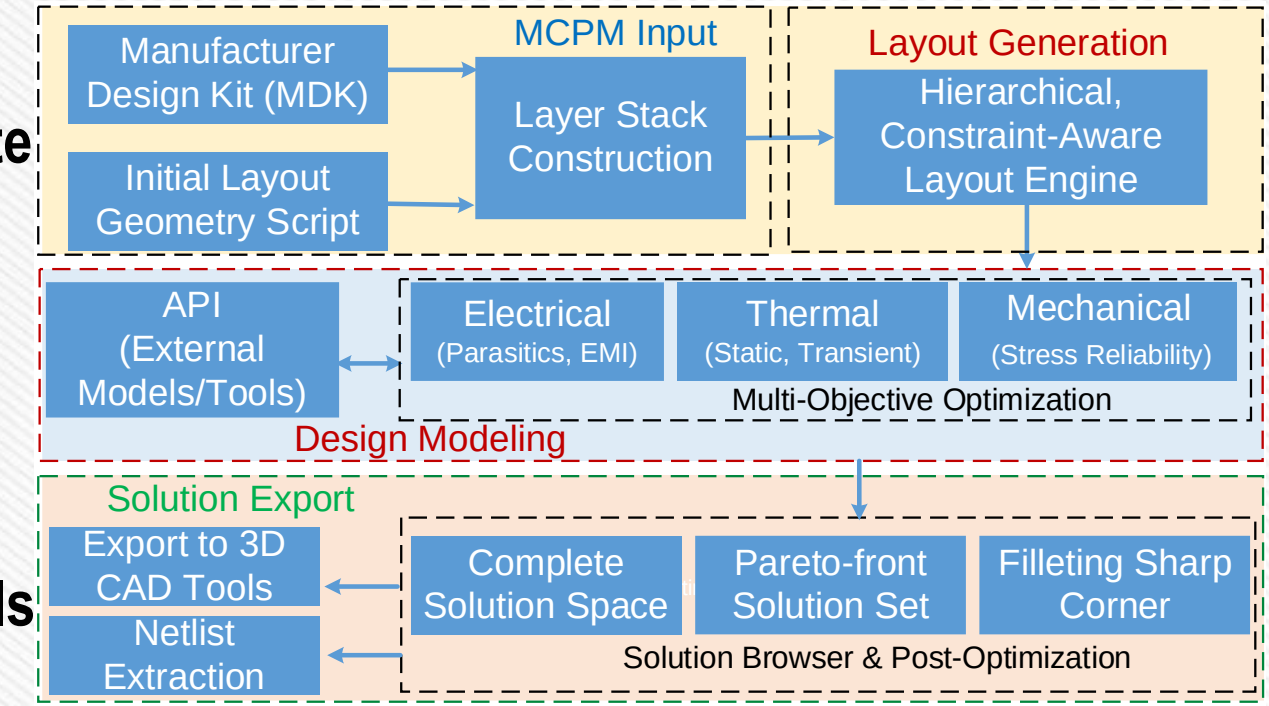
PowerSynth Features:

- MDK ensures manufacturability
- Layer stack parameterization
- Constraint-aware layout engine to generate DRC-clean layouts
- MCPM performance evaluation: fast, accurate and reduced-order electrical and thermal model.
- Electro-thermal reliability optimization
- Easily export design solutions to FEA tools

Release Website:

https://e3da.csce.uark.edu/release/PowerSynth/

- PS v1.x : 2D/2.5D MCPM Optimization
- PS v2+: 2D/2.5D/3D MCPM Optimization



PowerSynth architecture

Motivation and Our Contributions

❑ Motivation

- **Reliability optimization of MCPM is obvious before fabrication**
- **Existing methodologies:**
  - specific part/component failure mechanism/lifetime prediction
  - involves time-consuming FEA methodology
  - only layer stack material/thickness parameterization
  - limited solution space: placement and routing not considered

❑ Our Contributions:

- **Two-step electro-thermal reliability optimization methodology includes:**
  - layer stack optimization
  - placement and routing optimization
- **Fast, accurate transient thermal model for PowerSynth to predict thermal cycling behavior with phase change material (PCM)**
- **A comparative study of using PCM to reduce thermal cycling stress**

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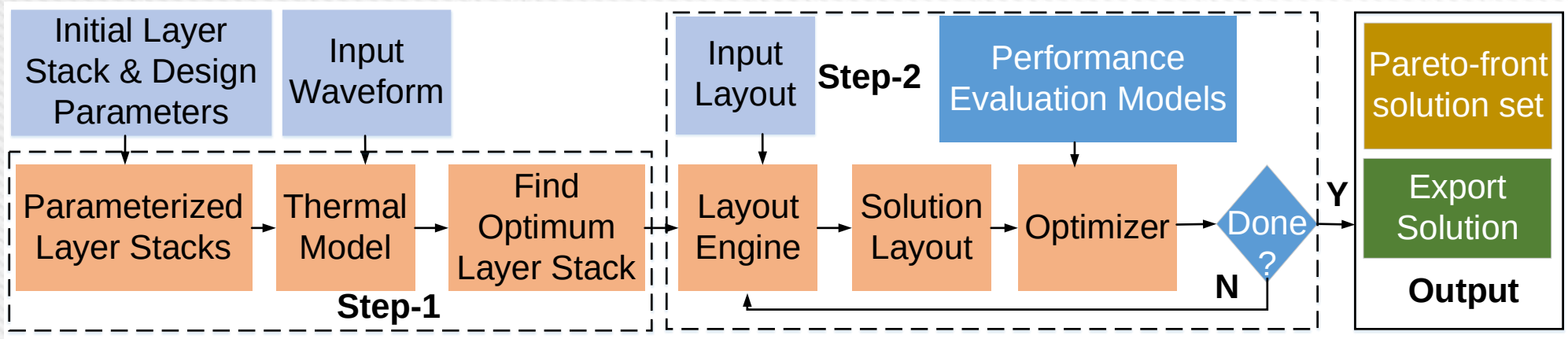
Our Approach

- **Goal: Optimization to reduce thermal cycling effects**
  - **Improve reliability of the whole module**
  - **Consider both layer stack and layout impact**
  - **Phase change material (PCM) usage:**
    - Optimizing location of PCM
    - Optimizing amount of PCM
    - reduce thermal stress due to fluctuations from the thermal cycling
- **Reliability Performance Metrics:**
  - **Electrical: Power loop inductance, High voltage/current operation**
  - **Thermal:**
    - Maximum transient temperature: thermal over-stress associated with material limits
    - Average temperature: thermal degradation modes
    - Peak-to-peak temperature: thermo-mechanical fatigue

Methodology

❑ Two-step optimization flow:

- **Step-1: Layer stack optimization**
  - Material, thickness variation
- **Step-2: Layout optimization**
  - Placement of devices & routing of traces
  - Variable floorplan sizes



- **Newly developed transient thermal model:**
  - Max, average, peak-to-peak temperature evaluation
  - Both static and transient thermal evaluation
  - Interaction among three tools

POWERSYNTH

ARL ParaPower

HSPICE

"ARL ParaPower": https://github.com/USArmyResearchLab/ParaPower

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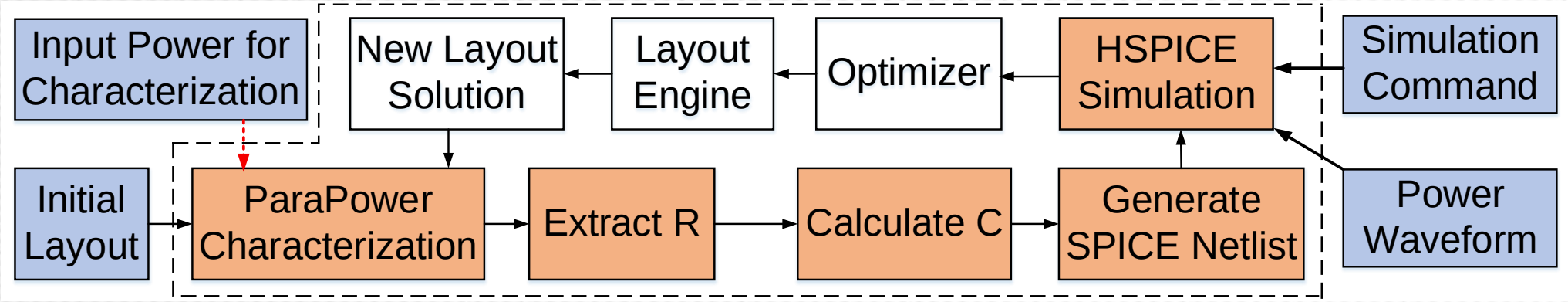
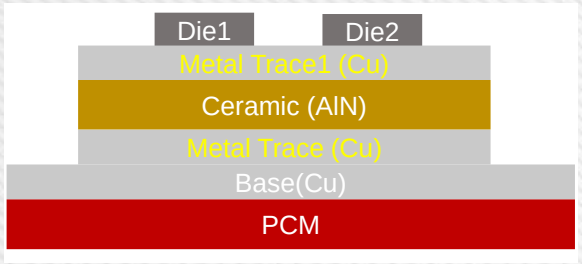
PowerSynth Transient Thermal Model

- **Newly developed transient thermal model:**
  - Generic layer stack handling with the latest layout engine of PowerSynth.
  - Represents MCPM structure as a cauer thermal RC network
  - Thermal resistance (R) extraction through ParaPower characterization
  - Thermal capacitance (C) value calculation using material properties.
  - PCM is modeled as voltage (temperature) dependent variable R and C.
  - HSPICE engine: solves RC-network to produce temperature metrics result
  - More capabilities:
    - Performance evaluation under input waveform parameters sweep
    - Find the optimum operating waveform for a given layer stack.

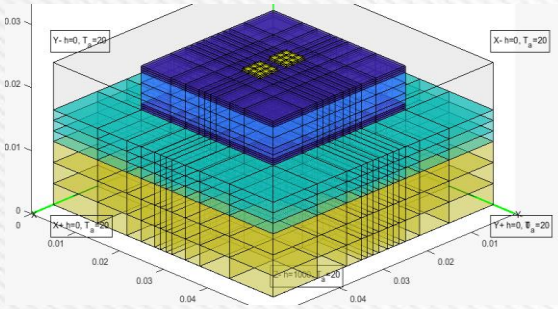


Model Validation

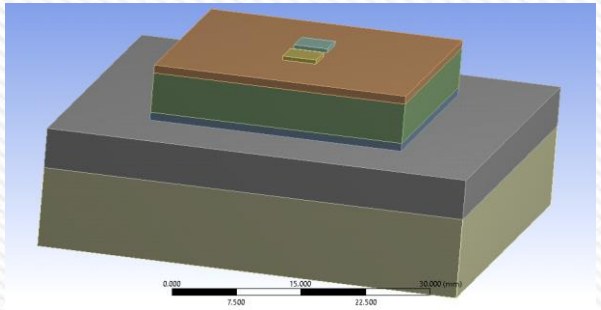
❑ An example layer stack and corresponding validation structure



Layer stack

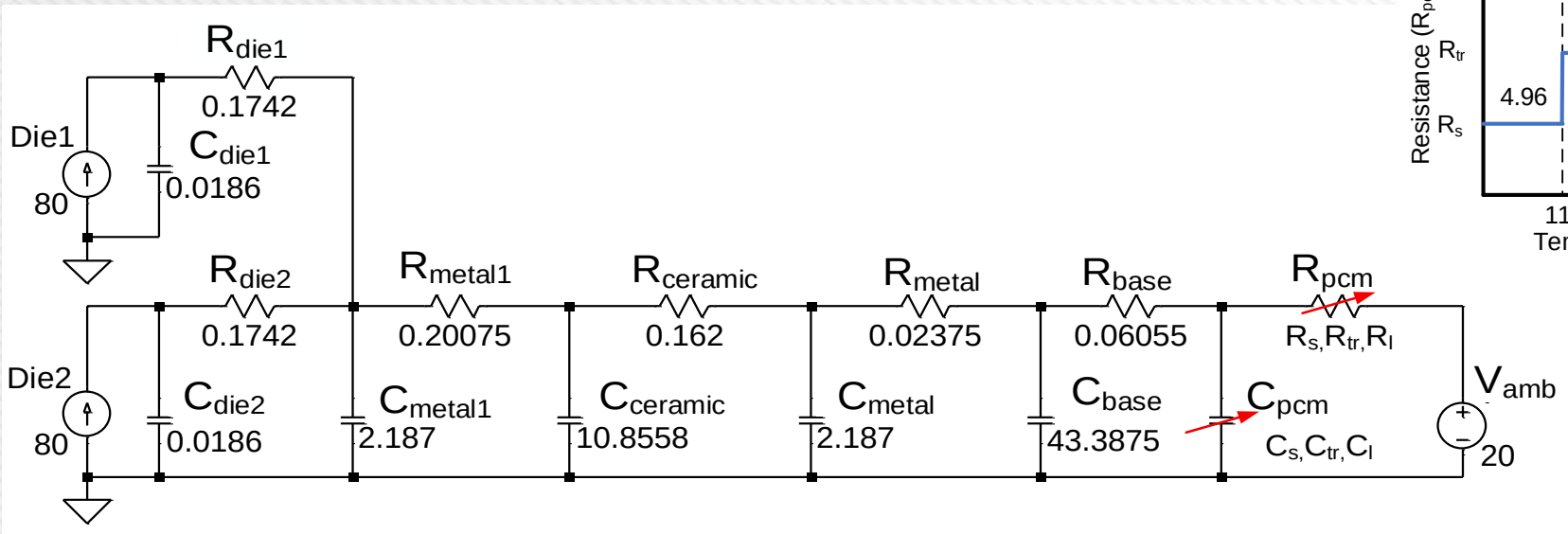


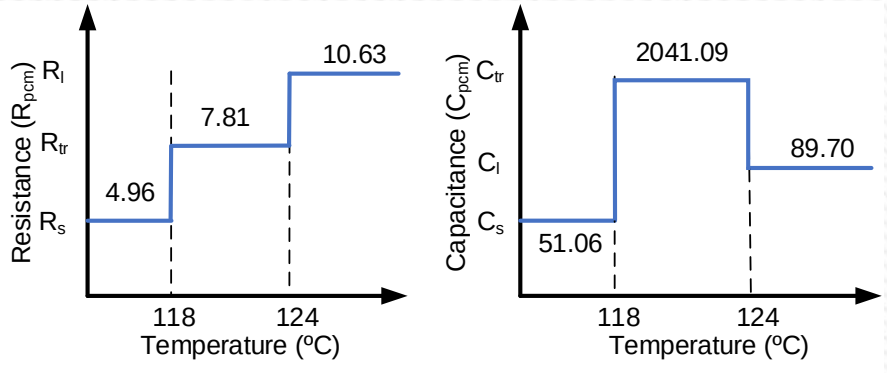
ParaPower structure



ANSYS structure

❑ Corresponding Cauer thermal network:

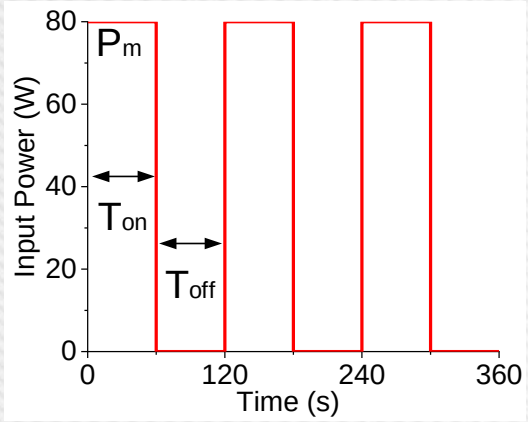




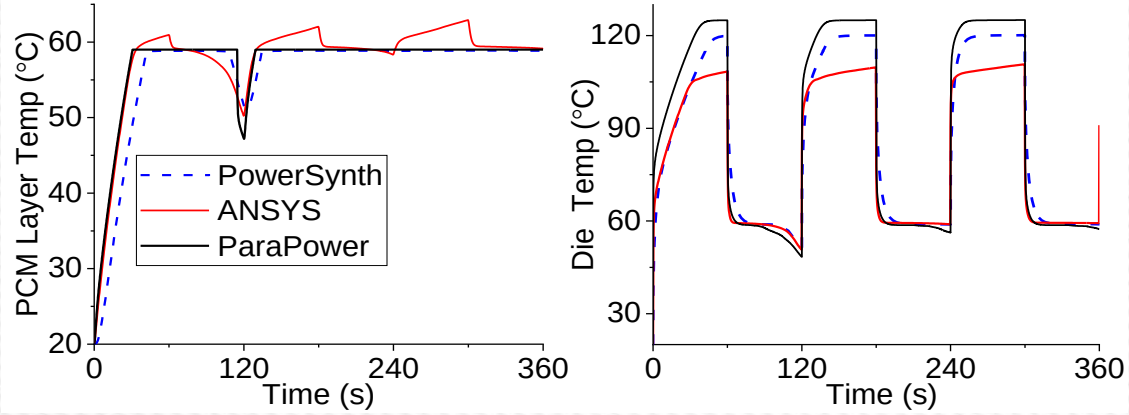
Variable R,C values for PCM

Validation Results

❑ Input waveform and Resultant PCM, die layer temperature:



Input Waveform



Resultant Waveform

❑ Performance comparison result:

Approach	Max Temp. (°C)	Avg. Temp. (°C)	P-to-P Temp. (°C)	Runtime (s)	Speedup	Memory (MB)
ANSYS	110.7	84.87	51.73	11165	1×	3373
ParaPower	125.0	90.64	68.67	35.27	316×	2361
PowerSynth	120.1	89.57	61.14	3.2	3489×	315

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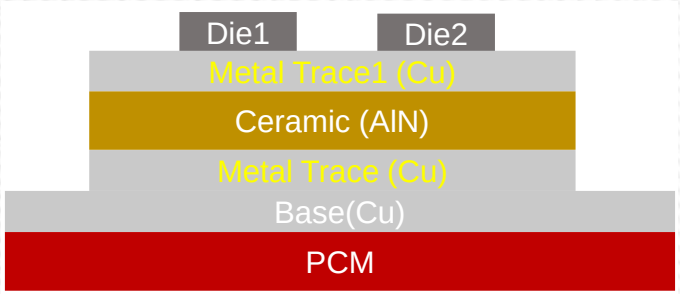
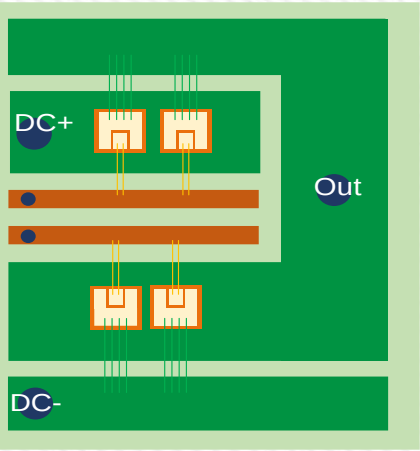
Reliability Optimization Case Study

- **MCPM layer stack and layout for case study:**
  - 2D half-bridge power module
  - PCM layer is considered

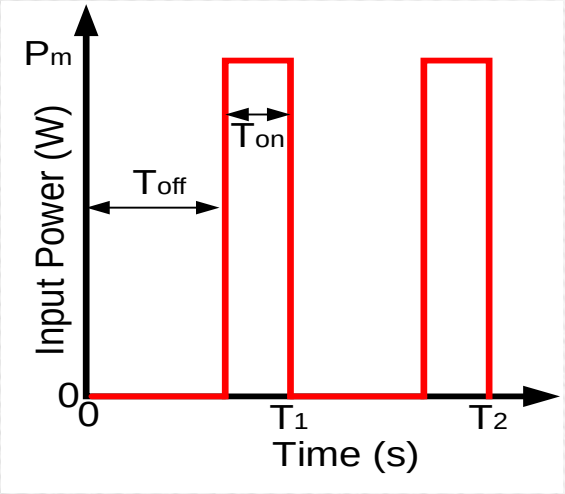


Layer stack

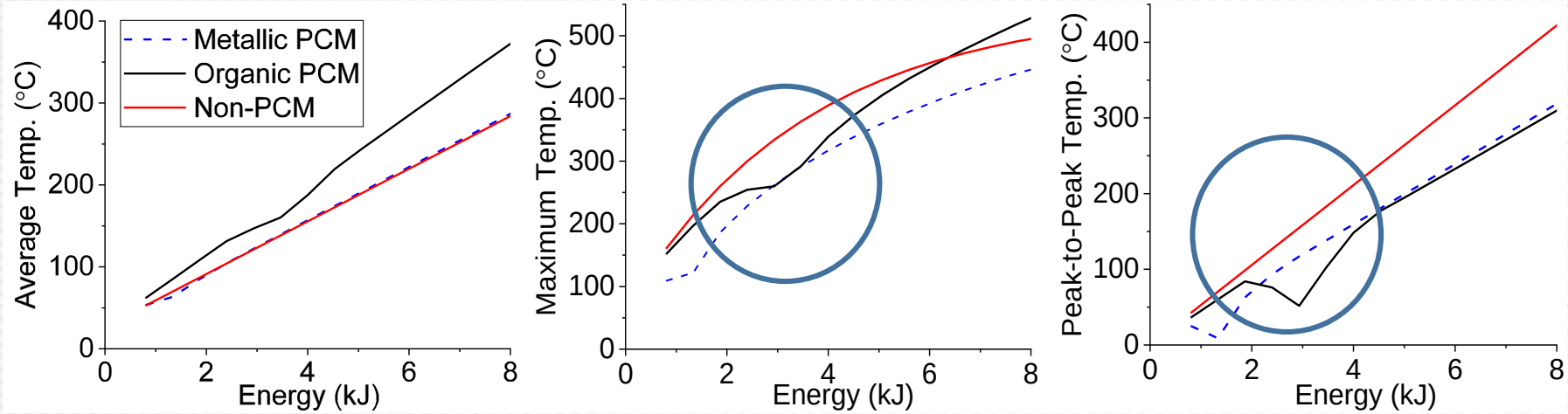


Half-Bridge MCPM Layout

- **Choosing thermal cycling waveform:**
  - Energy sweep: Varying Ton & Pm
  - Optimum waveform (Ton= 60 s, Pm= 40 W) is chosen based on the thermal metrics.



Sample Input Waveform



Energy sweep result

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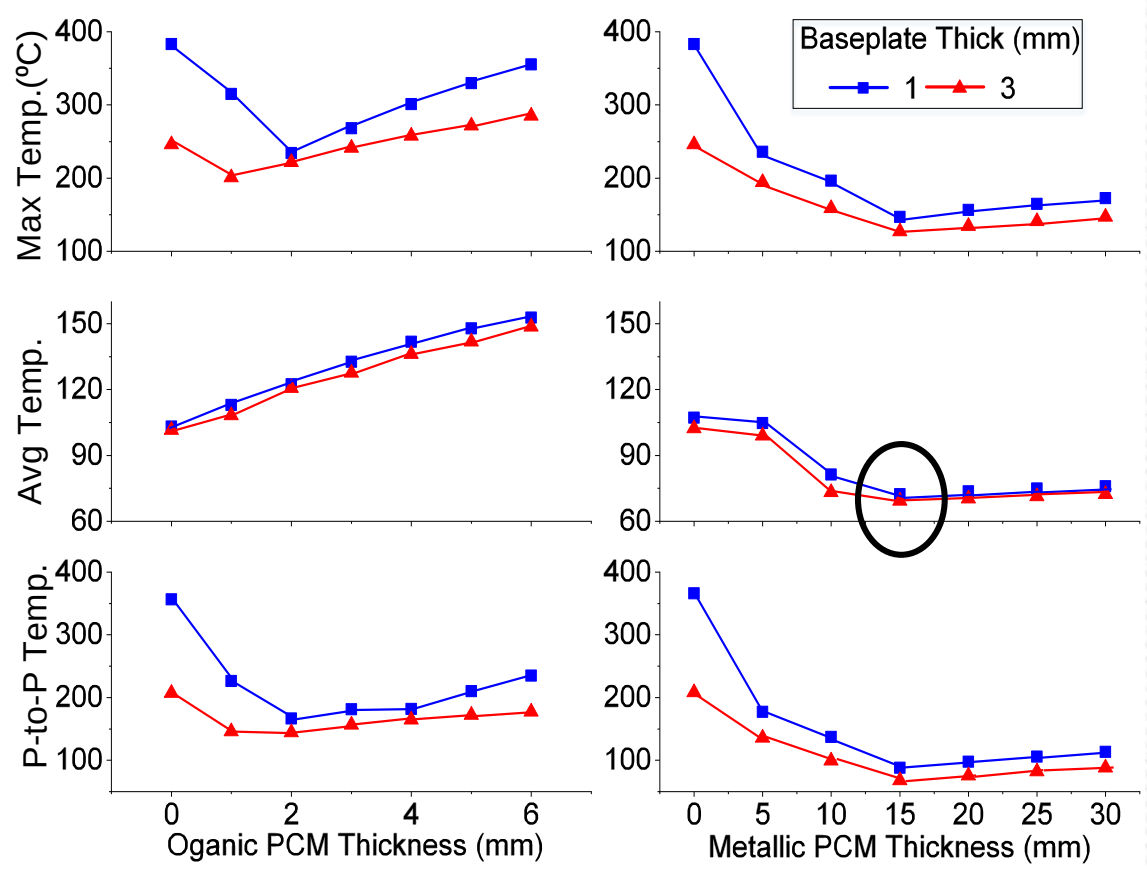
Layer Stack Optimization

❑ Step-1

- **Layer stack optimization**

Layer	Material	Thickness (mm)
Baseplate	Copper	1, 3
PCM	Fields' Metal (Metallic)	0, 5, 10, … 30
	Erythritol (Organic)	0, 1, 2, … 6

- **Optimum layer stack:**
  - 3 mm Copper baseplate
  - 15 mm Metallic PCM

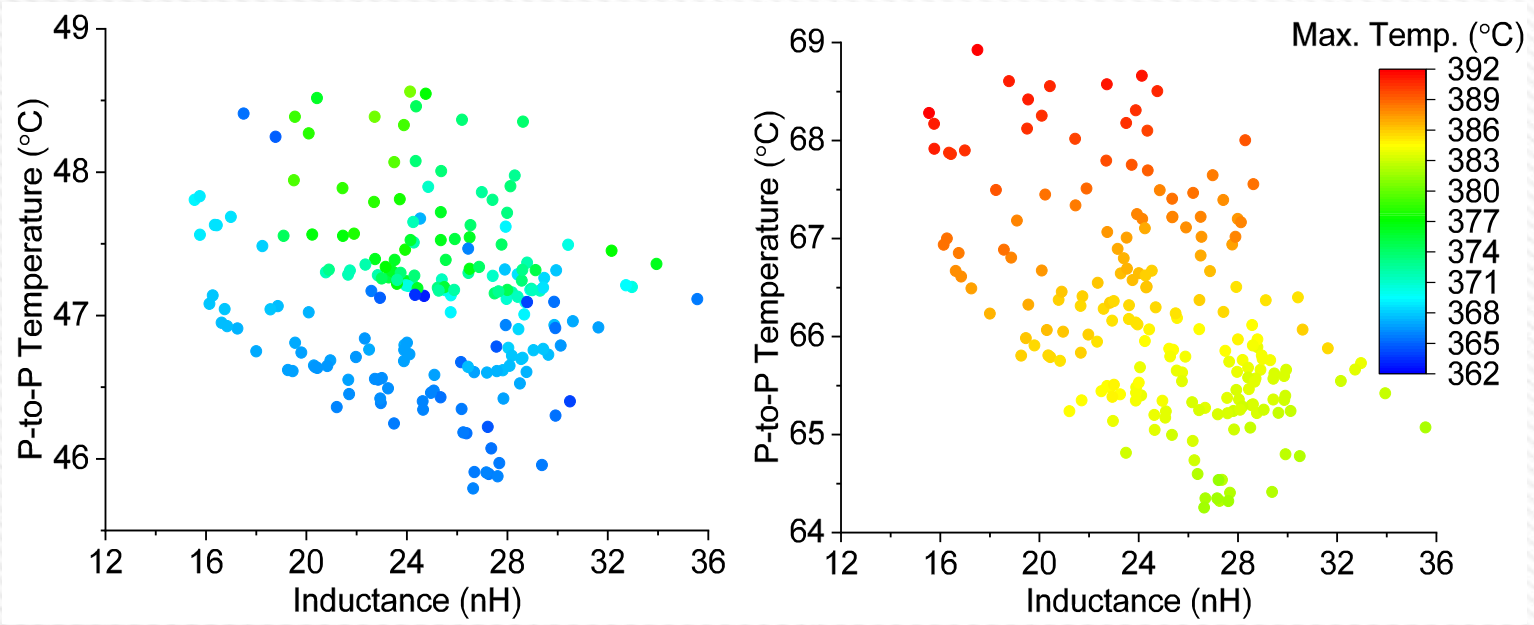


Temperature metrics vs. thickness variation

PCM vs Non-PCM Comparison

❑ Optimum layer stack vs. Non-PCM case

- **Layer stack choice:**
  - 3 mm Copper baseplate with no-PCM
  - 3 mm Copper baseplate with 15 mm metallic PCM (optimum layer stack)
- **Electro-thermal optimization**
  - 200 solutions for each
- **Input waveform:**
  - between 0 W to 40 W
  - 15% duty cycle
- **Total runtime:**
  - PCM→ ~815 s
  - Non-PCM→ ~147 s
- **PCM provides better thermal capacity over non-PCM**

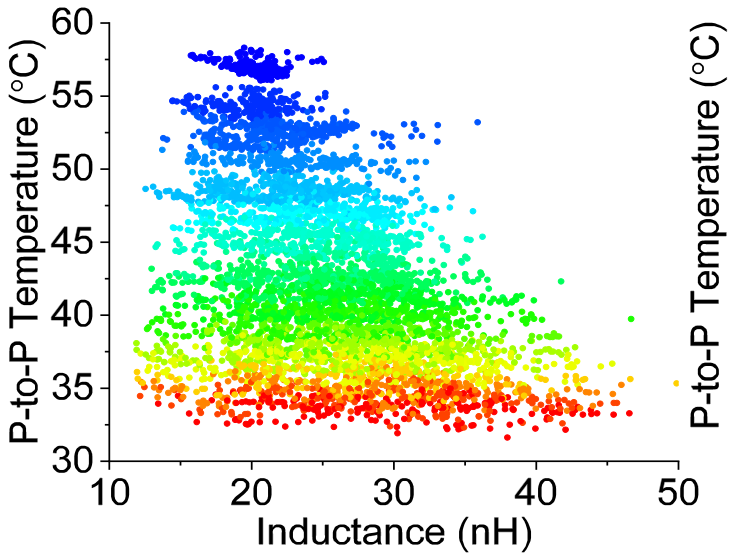


Fixed-floorplan size (46 mm × 36 mm) solution space

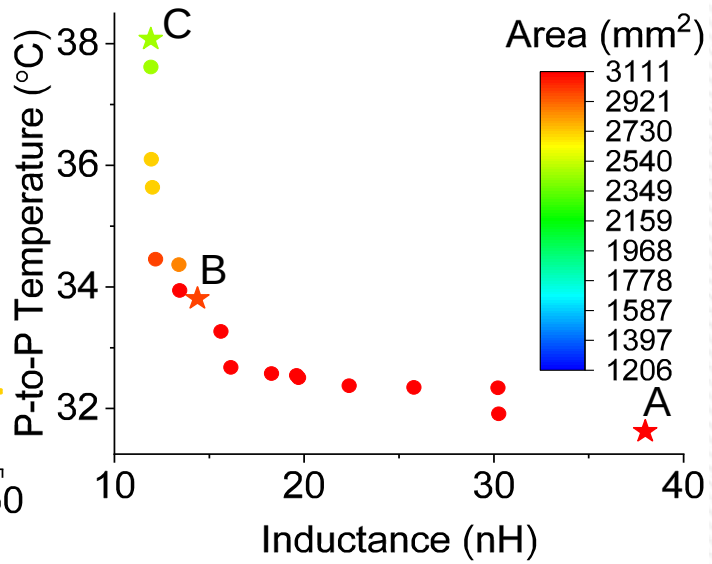
PowerSynth-Guided Layout Optimization

Step-2

- **Layout optimization**
  - Optimum layer stack is considered.
  - 6400 solutions with 32 different floorplan sizes.
  - For each size, 200 solutions are generated and evaluated (total runtime ~815 s)



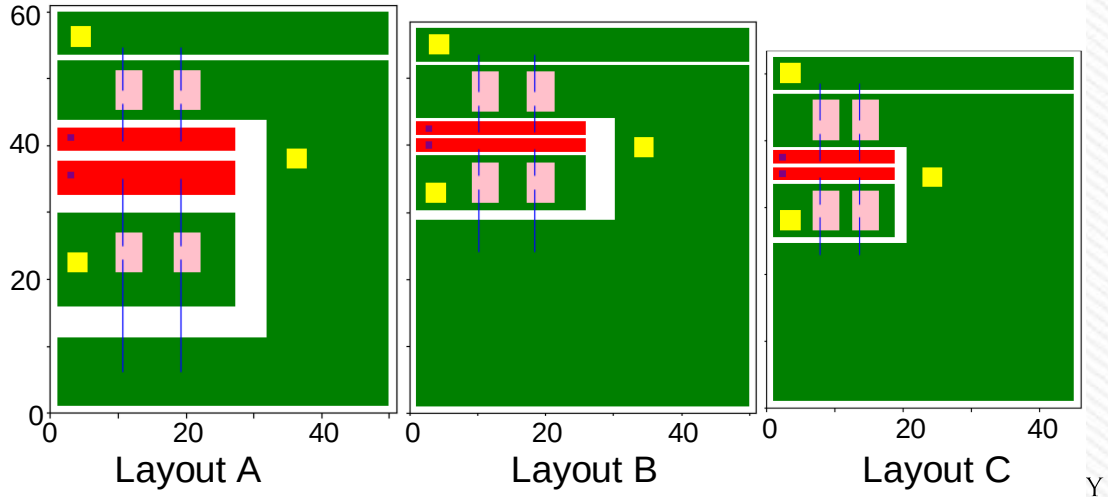
Complete solution space



Pareto-front solutions

Performance Table

ID	Floorplan Size (mm × mm)	Loop Inductance (nH)	P-to-P Temperature (ºC)
A	51 × 61	37.98	31.62
B	51 × 58.5	14.38	33.81
C	46 × 53.5	11.91	38.07



Selected Layouts

Conclusions and Future Work

Conclusions:

- Two-step methodology is efficient, scalable, and generic
- The transient thermal model has shown 3489 times speedup within 10% accuracy compared to ANSYS simulation results.
- Structure optimization is necessary for best results.
- From the case study, a combination of layout optimization and layer stack tuning can provide performant-yet-reliable solutions.
- A reliability-aware design automation tool can further reduce design efforts and engineering time.

Future Works:

- Mechanical stress will be considered as optimization objective.
- More exhaustive search in the layer stack parameterization will be performed.
- Methodology will be validated against physical measurements.

Thank You

Any Question?

For more information, please visit E3DA Lab Website:

https://e3da.csce.uark.edu