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Electronic Design Automation (EDA) Tools and Considerations for Electro-Thermo-Mechanical Co-Design of High Voltage Power Modules

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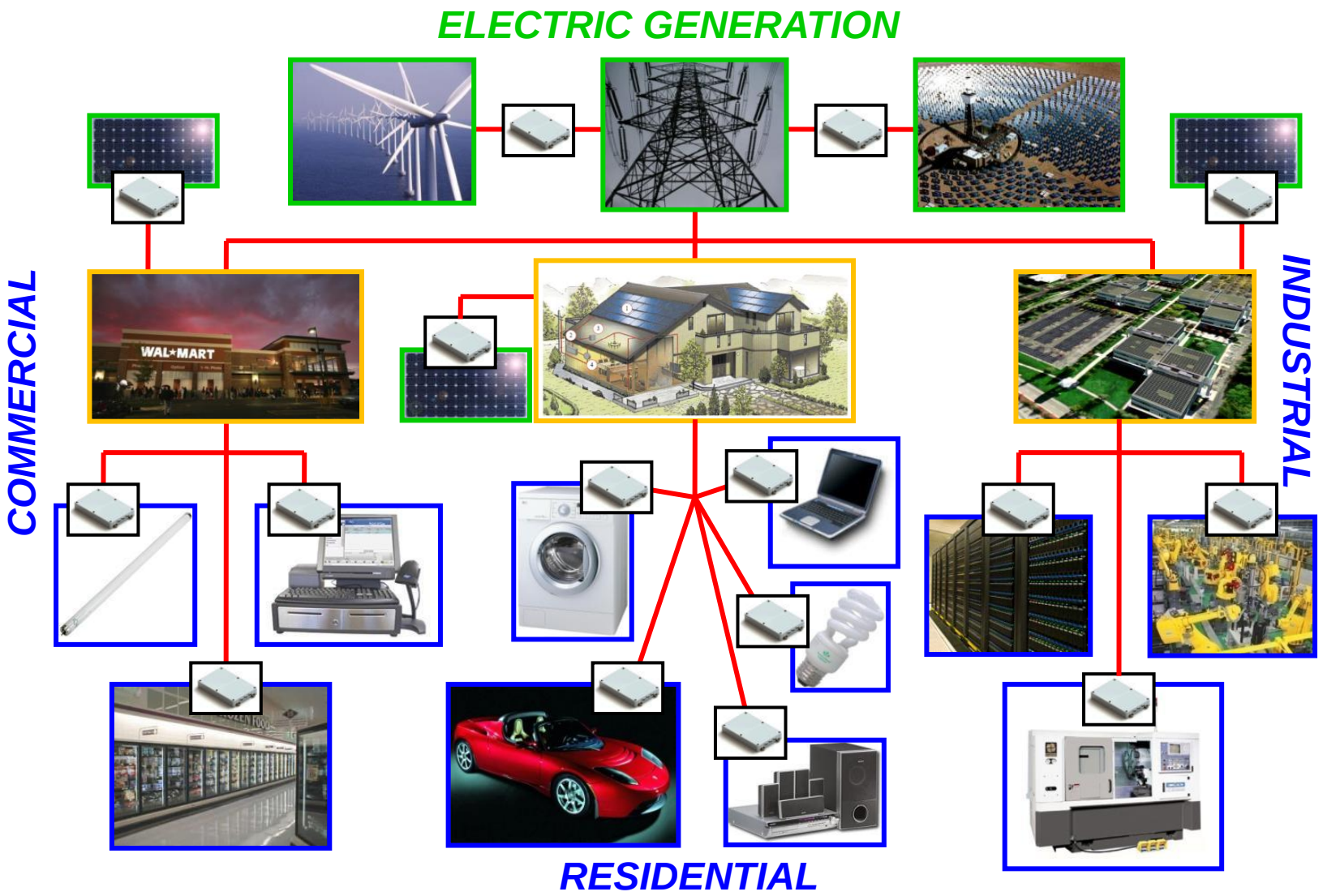
Outline

- Motivation
- PowerSynth Introduction
  - Overview
  - Models
  - High voltage reliability constraints
- ParaPower Introduction
- EDA tool integration
- Co-design example
- Summary

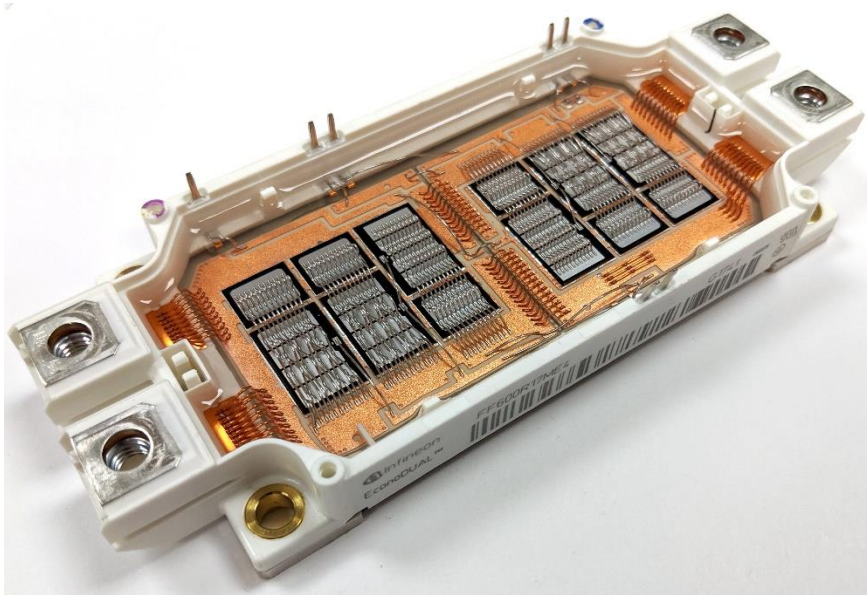
Power Electronics is Everywhere



MCPM Co-Design Challenges

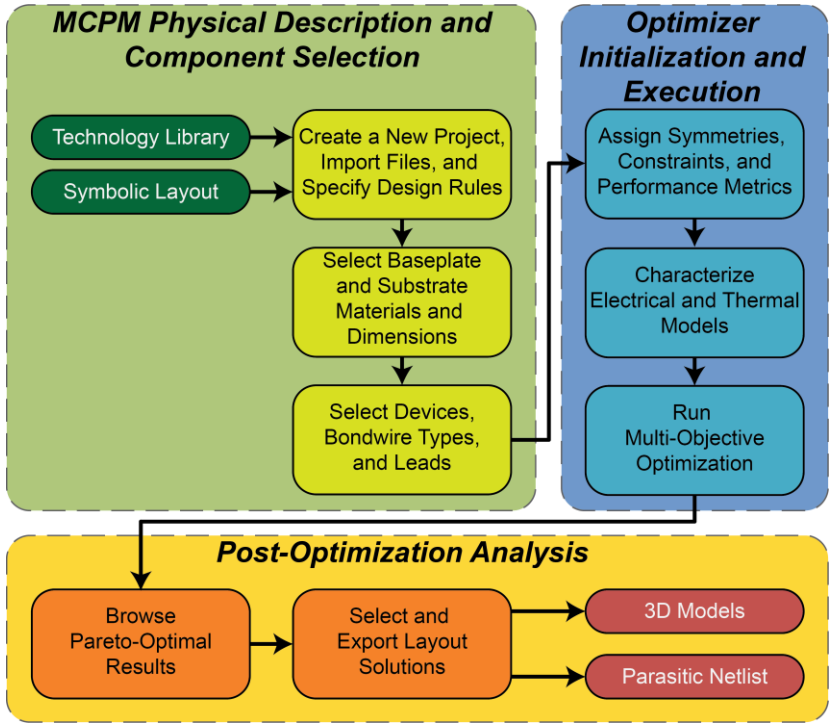
Physical design of multi-chip power modules (MCPM) is time consuming and poses several challenges:

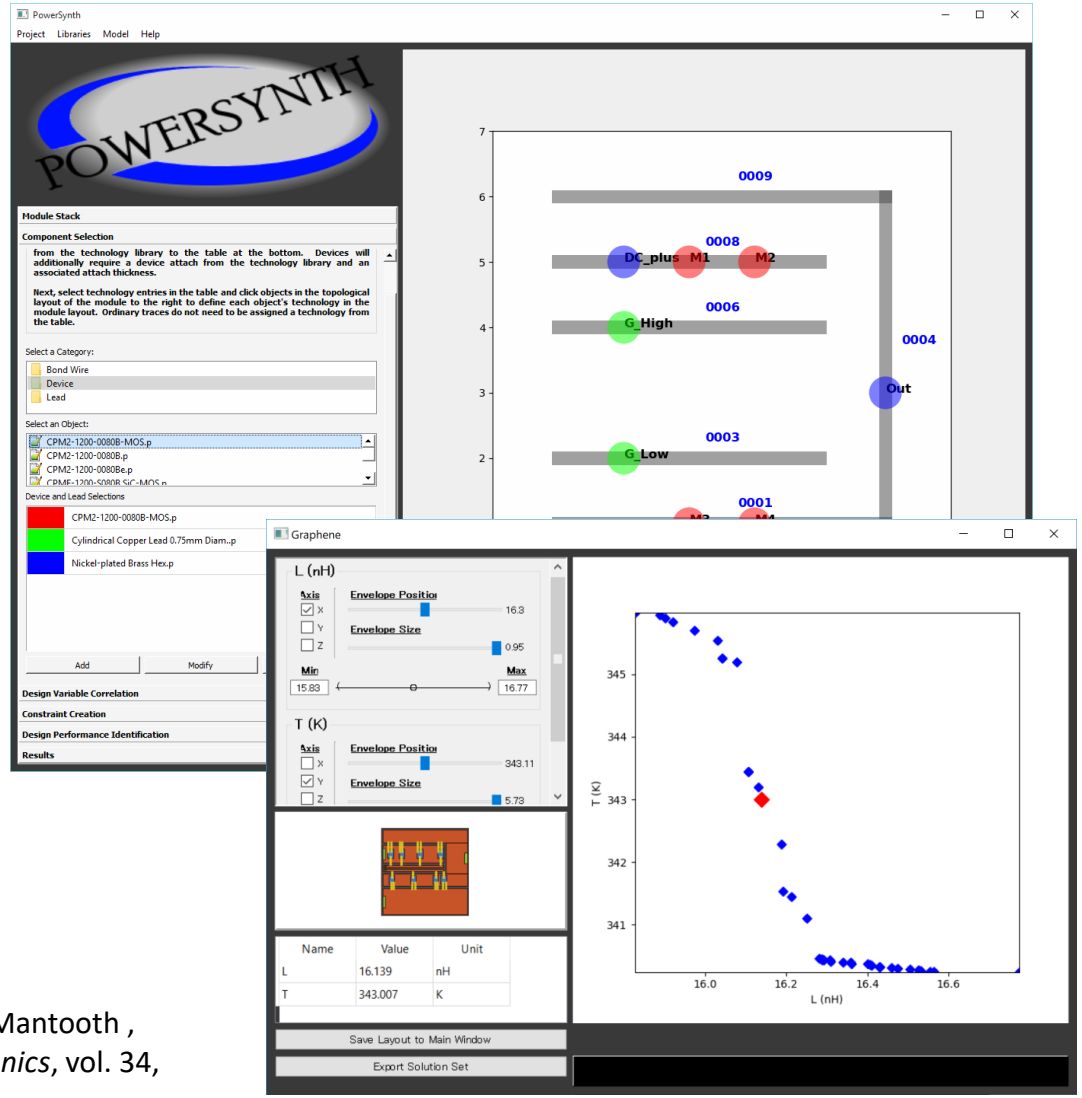
- Multi-domain nature of power electronic packaging necessitates consideration of materials and designs towards reduced:
  - Electrical parasitics for high performance devices
  - Temperature and mechanical stress for higher reliability
- Traditional design flows are iterative and require extensive use of computationally expensive finite element analysis (FEA)



PowerSynth Overview

- EDA tool for multi-chip power modules (MCPM)
- Multi-objective layout optimization
- Reduced order models
- Pareto-front of tradeoffs
- Design export





Tristan M. Evans, Quang Le, Shilpi Mukherjee, Imam Al Razi, Tom Vrotsos, Yarui Peng, H. Alan Mantooth , "PowerSynth: A Power Module Layout Generation Tool," in *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5063-5078, June 2019. doi: 10.1109/TPEL.2018.2870346 **Highlighted Paper**

PowerSynth Manufacturer Design Kit (MDK) and Technology Library

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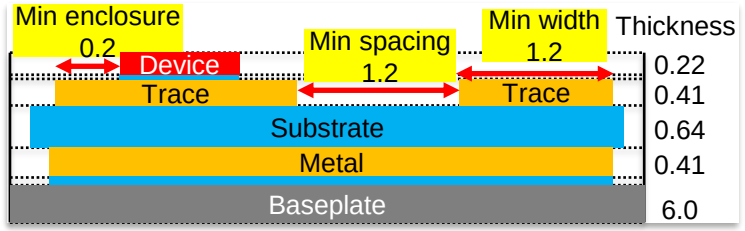
Layer Stack

- Input file describing layers and technologies
- Holds information pertaining to
  - Layer width, length, and thickness
  - Layer material properties

MDK and Design Rules and Checker (DRC)

- Input file containing technology-dependent design and processing rules
- Ensures feature sizing and component placement are within processing tolerance



MCPM layer stack

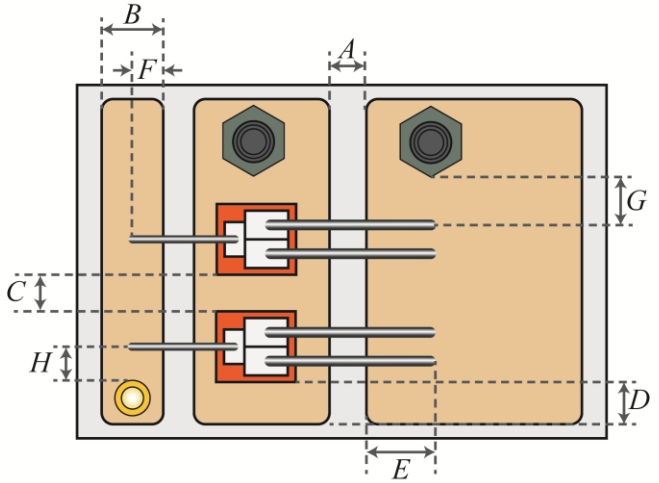
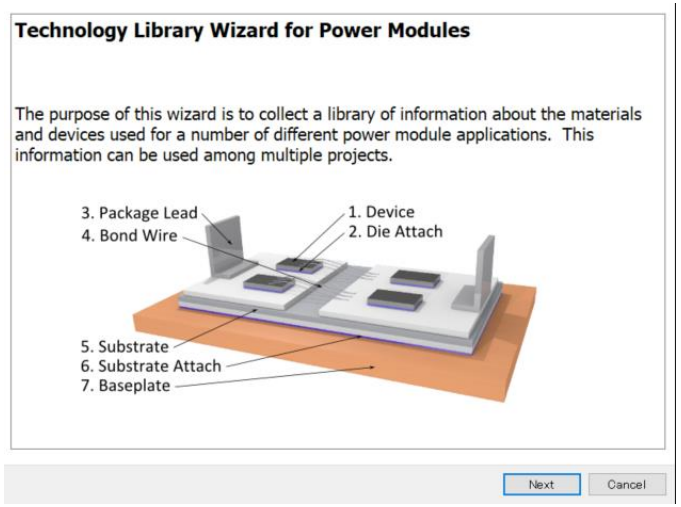


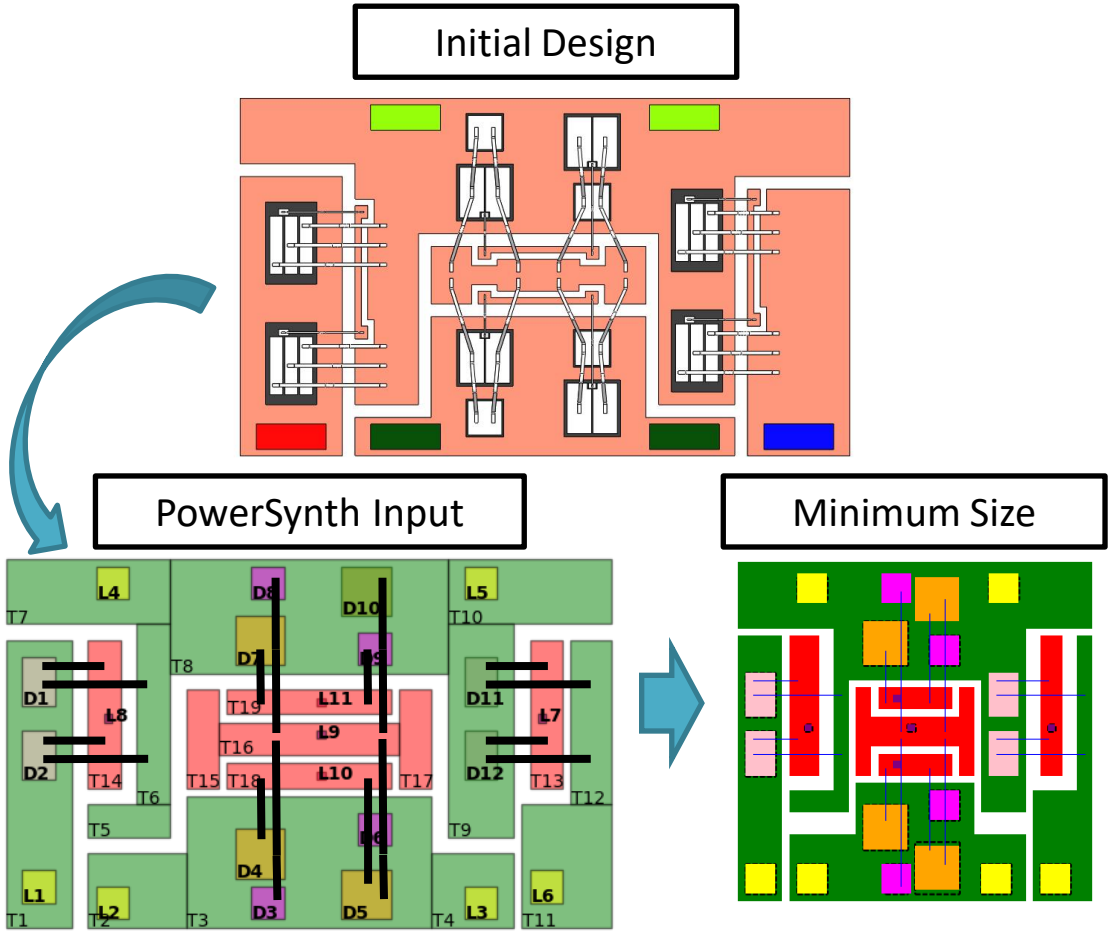
Illustration of design rules pertaining to feature placement and minimum spacing



PowerSynth technology library wizard

PowerSynth Layout Engine

- Constraint aware, hierarchical layout engine
- Minimum trace gaps set by trace-to-trace potential difference
- Heterogeneous component support
- Fixed or minimum layout size capabilities



I. Al Razi, Q. Le, H. A. Mantooth, and Y. Peng, "Constraint-Aware Algorithms for Heterogeneous Power Module Layout Synthesis and Reliability Optimization." in *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2018, pp. 323-330.

PowerSynth Thermal Model

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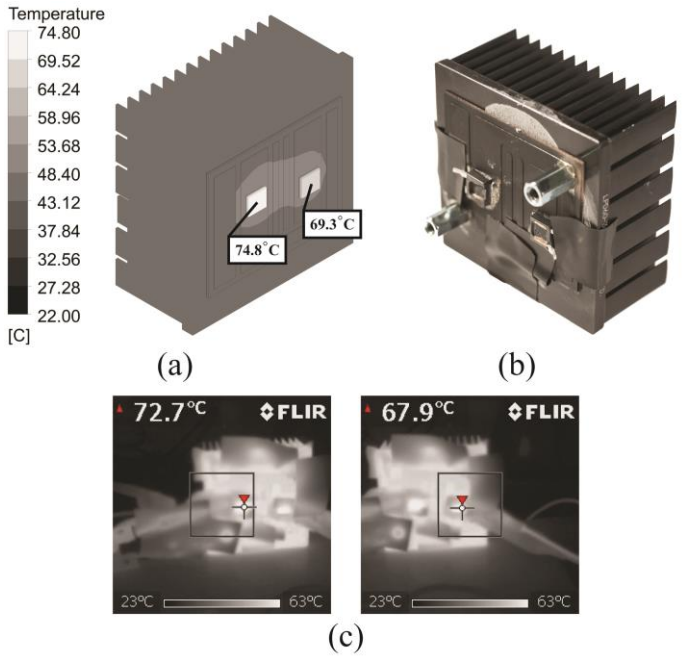
Fast Thermal Model

- Lumped element heat transfer system composed of thermal resistances
- Single FEA sim for characterization
- Includes mutual heating and proximity effects

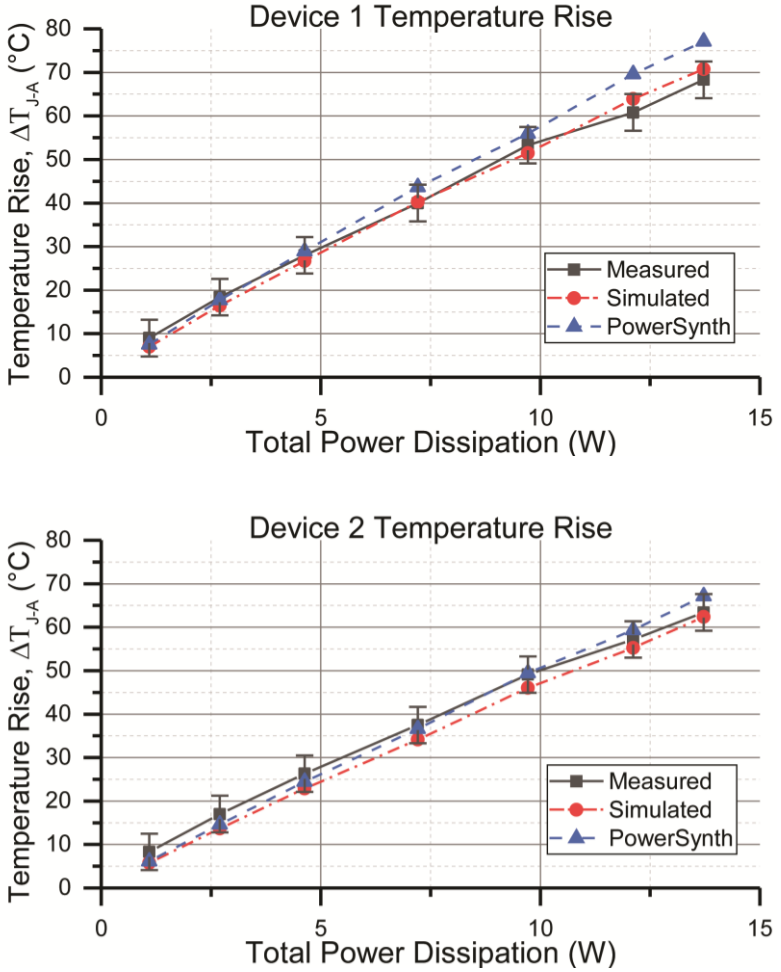
Device temperature rise results

- PowerSynth thermal model, Icepak, and thermal camera measurement comparison
- Average error of 4% when compared to simulation or measurement

PowerSynth accuracy within 10% but 8000x faster than FEA



Icepack simulation (a), test vehicle (b), IR measurement (c).



Thermal model validation results for device 1 (above) and device 2 (below) of the test vehicle over a range of power dissipation levels

PowerSynth Electrical Model

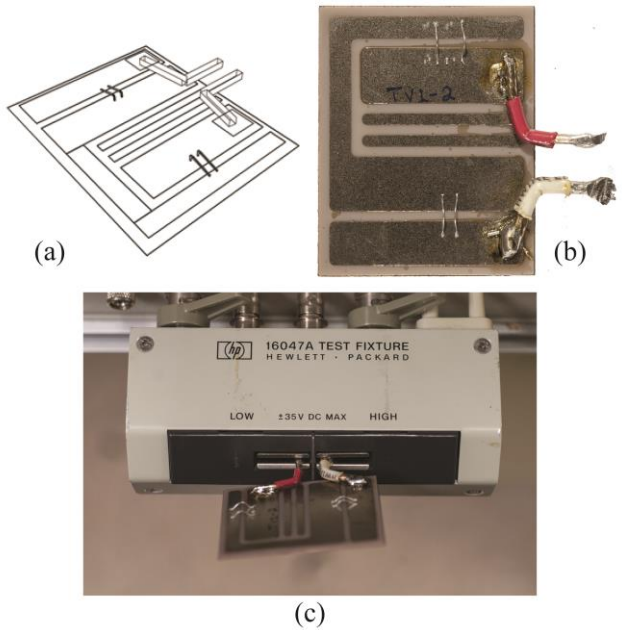
Response surface model (RSM) for parasitics

- Based on partial element equivalent circuit method (PEEC)
- Uses FastHenry to run parametric simulations for a given substrate technology
- Maps trace dimensions and vertical separation to resistance and inductance values

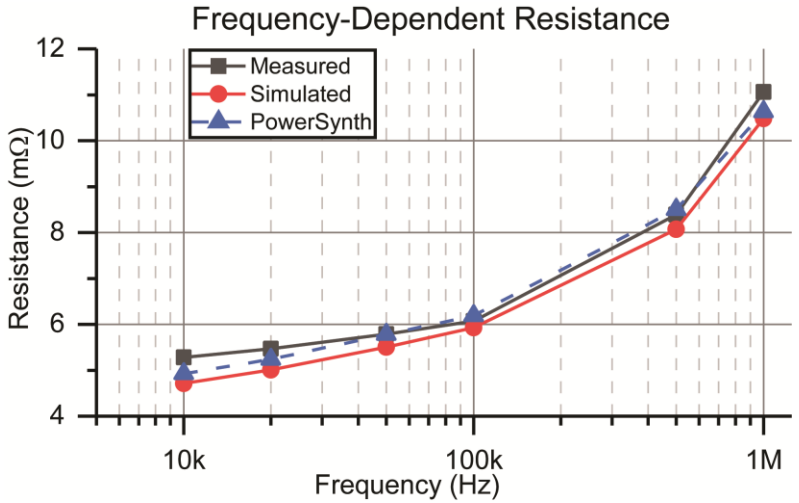
Resistance and inductance results

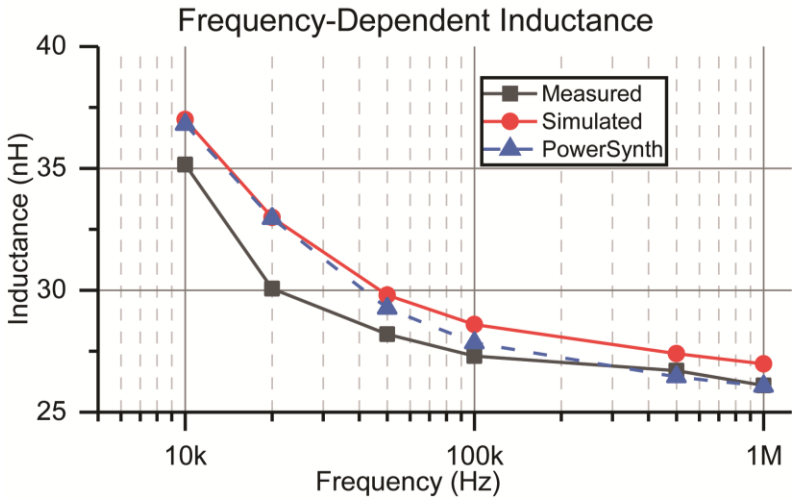
- Test vehicle layout parasitics compared among PowerSynth, FastHenry, and LCR meter measurement
- PowerSynth model error <10% with both simulation and measurement

RSM parasitics calculation is accurate and up to 6000 times faster than simulation



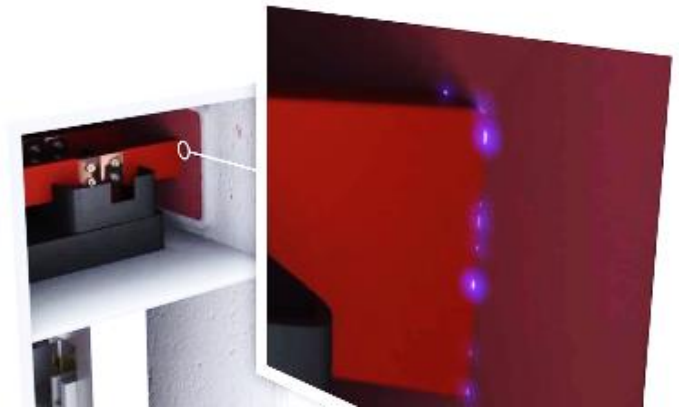
Simulation structure(a), test vehicle (b), LCR measurement (c).

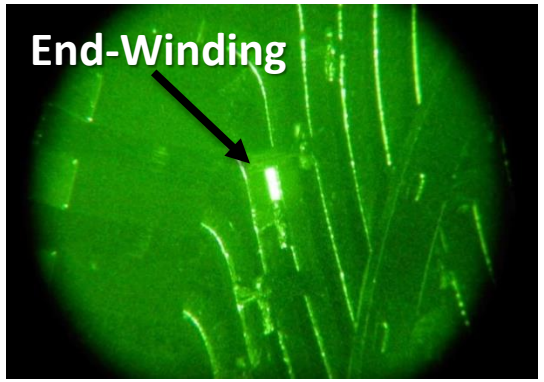


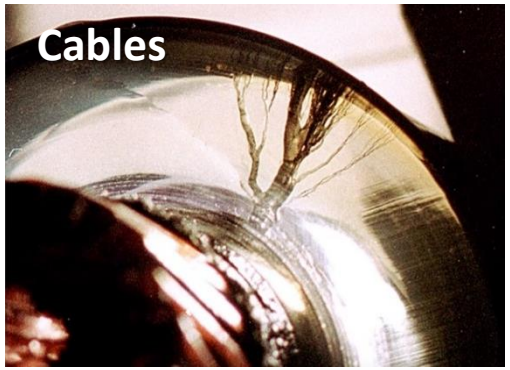


Electrical model validation results for resistance (above) and inductance (below)

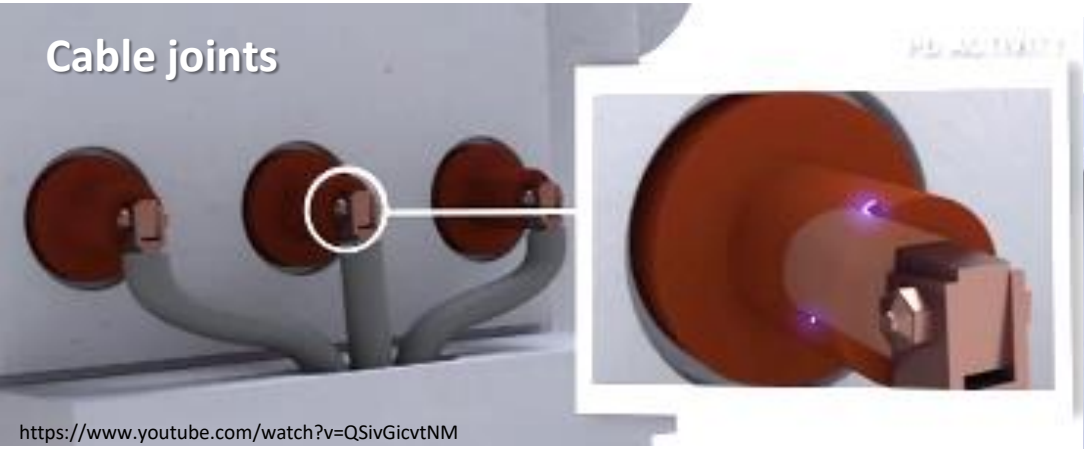
Partial Discharge (PD) and High Voltage Reliability

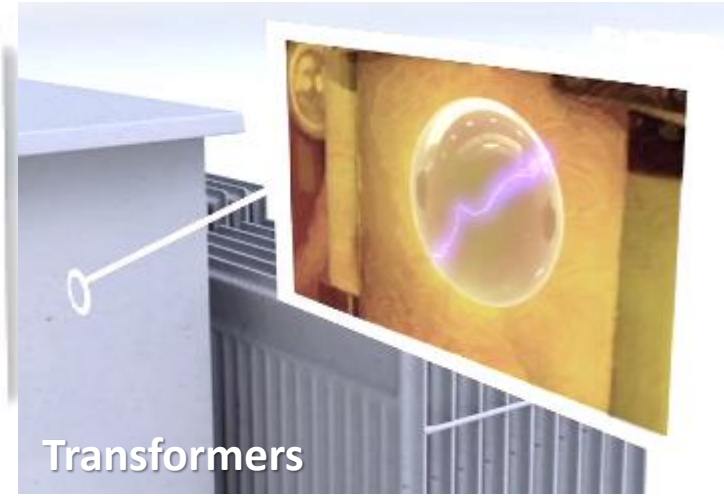


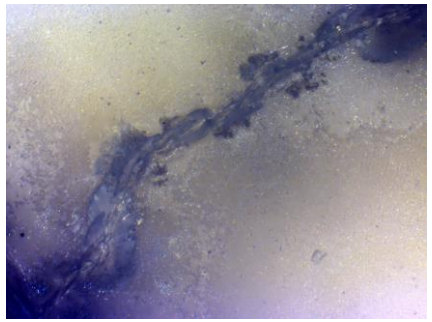


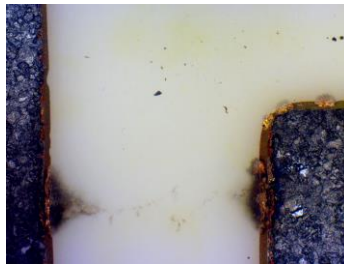


DBC test coupon



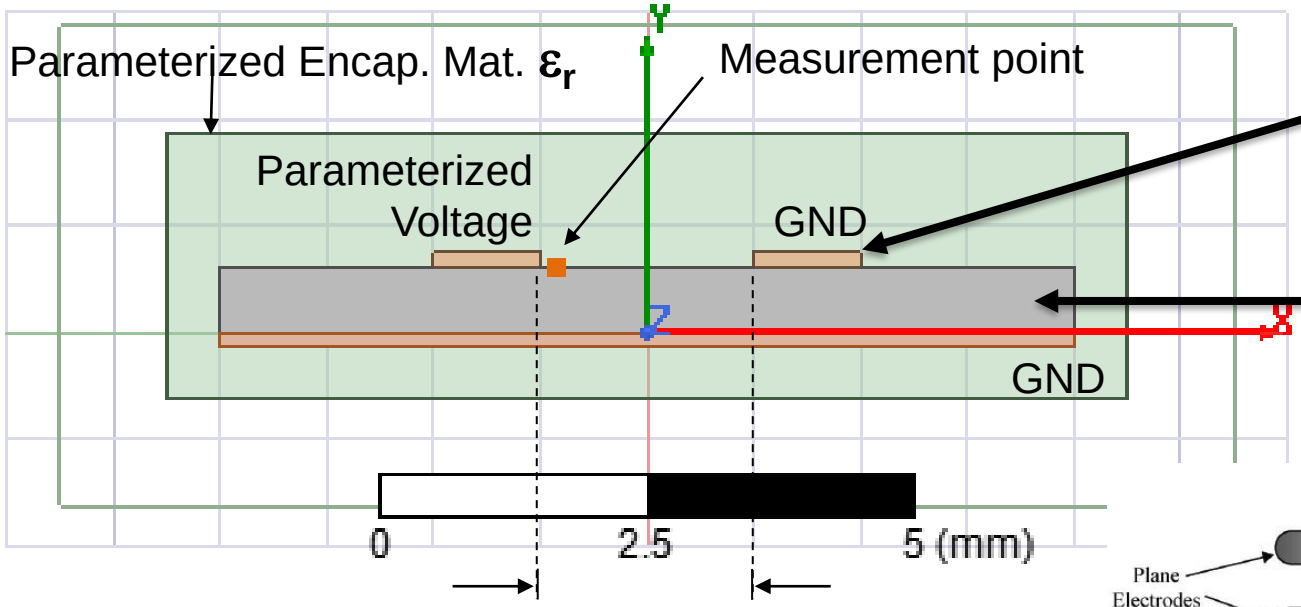




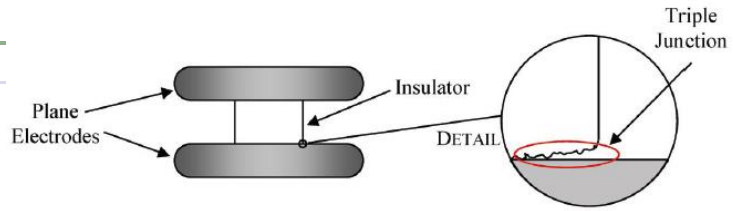


2D Electric Field Simulation Setup

Model geometry



TRACE GAP parameterized



Triple point detail

Parameter range:

Trace gap: 0.5mm to 5.0mm ε_r : 1 to 10 Voltage: 5kV to 30kV

2D Electric Field Simulations

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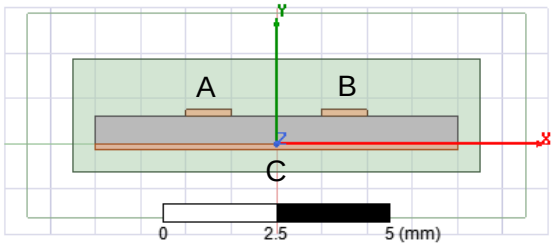
Model geometry

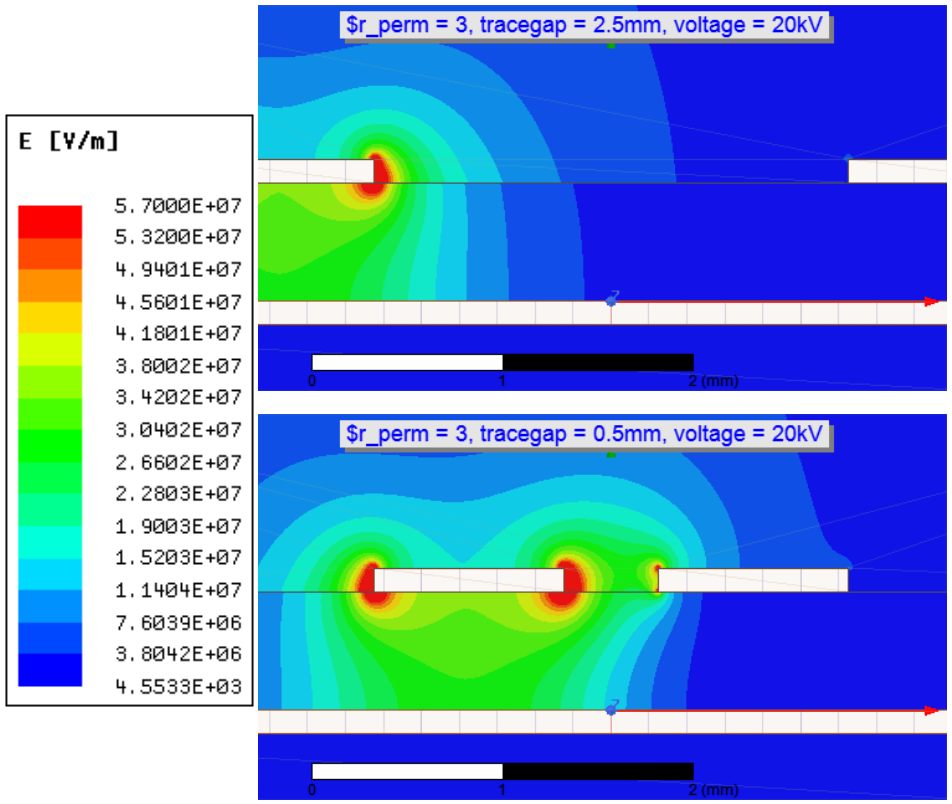


Parameter range:

Trace gap: 0.5mm to 5.0mm
step size: 0.5mm

ε_r : 1 to 10
step size: 1

Voltage: 5kV to 30kV
step size: 5kV



2D Electric Field Simulation Results

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General form of equation

$$E = f(v, \varepsilon_r)\, x^{-g(v, \varepsilon_r)}$$

Where

E is the electric field in kV/mm,

v is the voltage in kV,

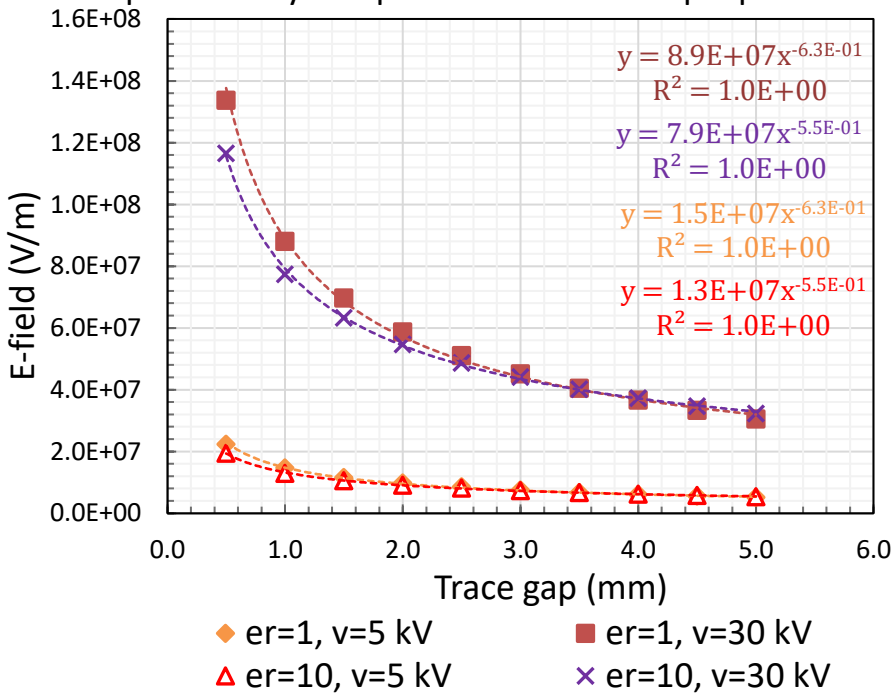
x is the gap between traces A and B in mm,

ε_r is the relative permittivity of the encapsulating material

f and g are functions of v and ε_r.

Power curves

E-field vs. trace gap for corner cases of the parametric sweep of voltage and relative permittivity at a point close to the triple point



Implementation in PowerSynth

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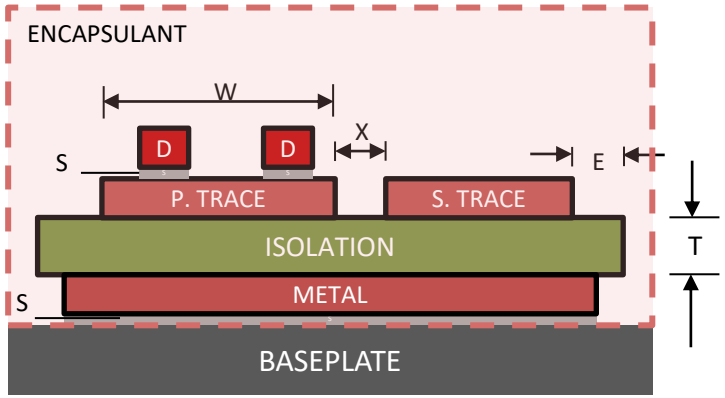
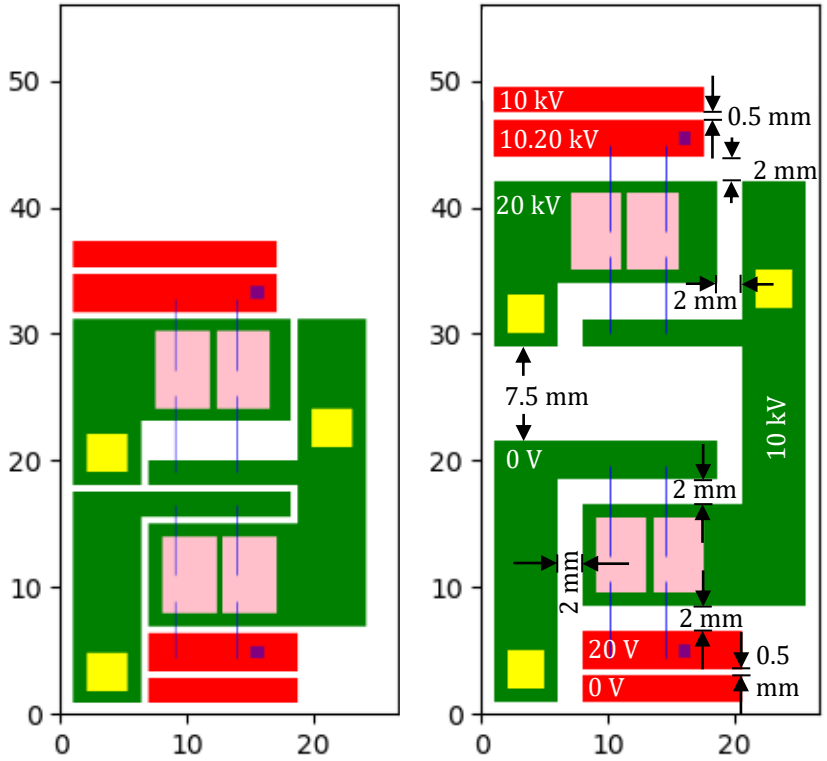
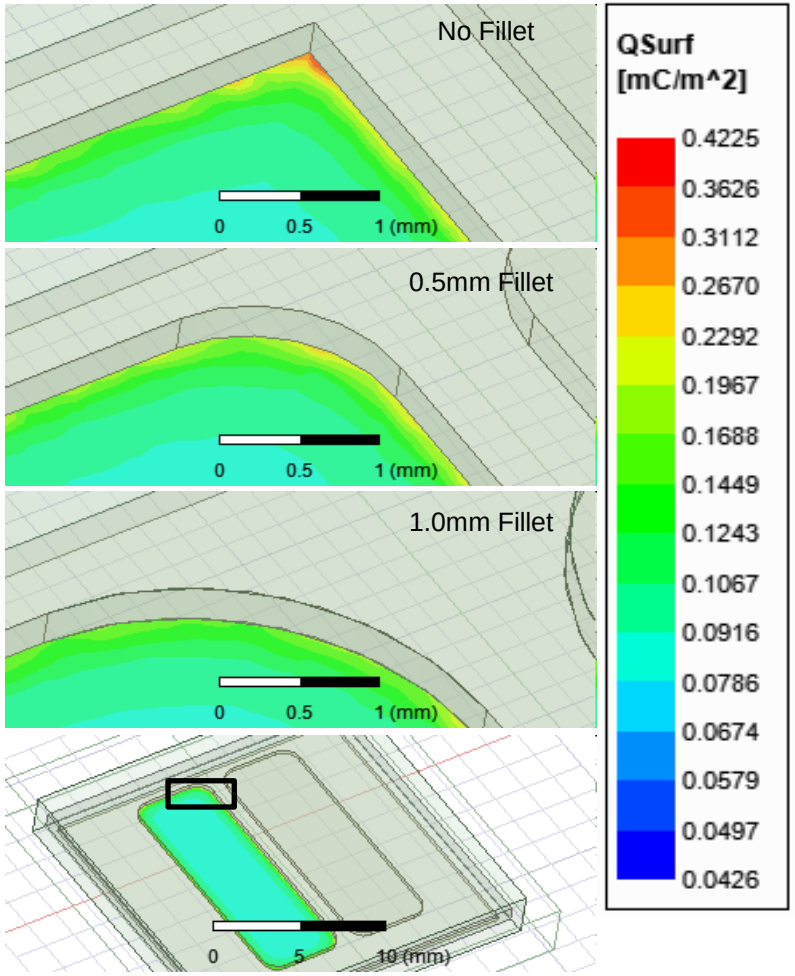


W: lateral width of trace
X: lateral trace gap
E: minimum enclosure
T: vertical thickness of a layer
D: device
P. trace: power trace; S. trace: signal trace
S: substrate attach or die attach

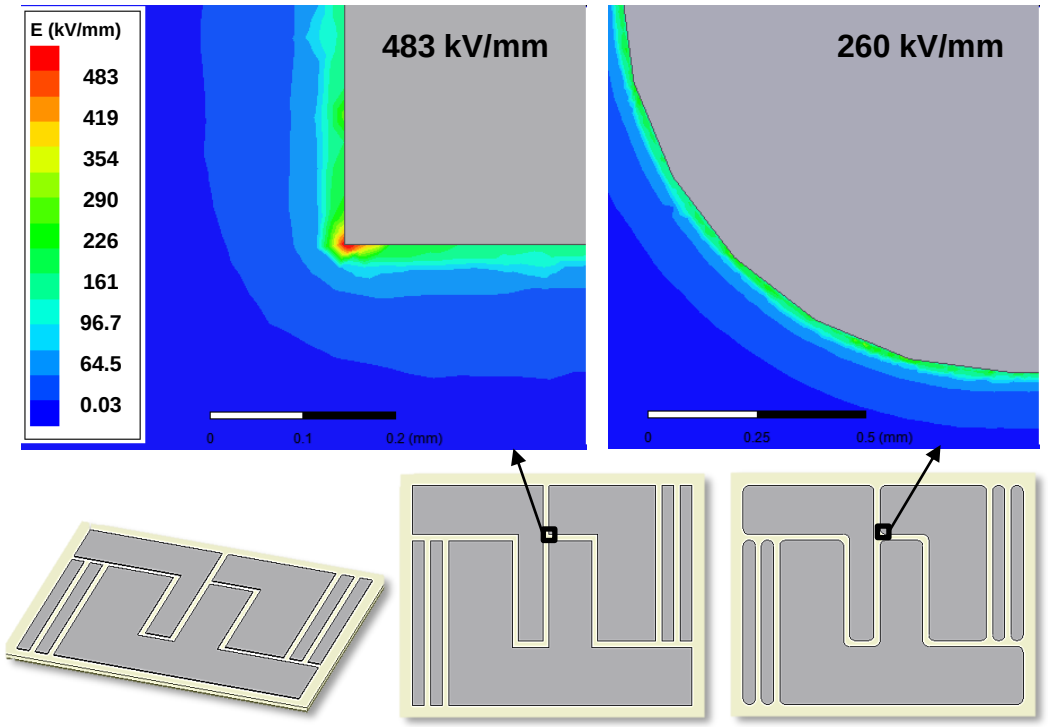
Default layout vs.
Layout with design rules applied



Effect of Filleting Sharp Corners



E-field and Q_s are almost halved



Filleting Reduces Mechanical Stress

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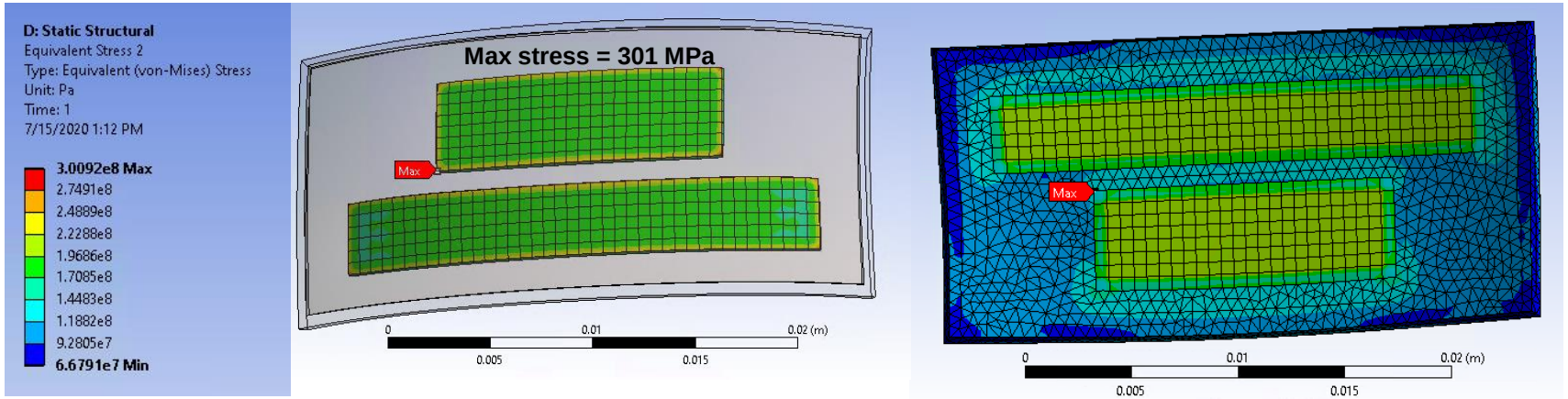
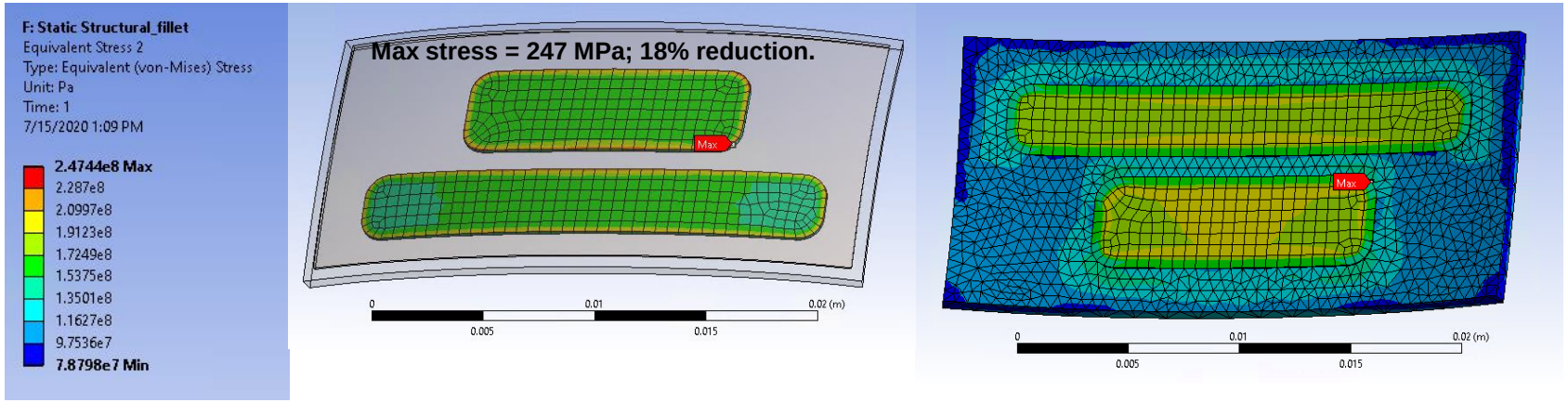
Bottom view

Top view

Sharp



Fillet



Effect of Filleting Sharp Corners with PowerSynth

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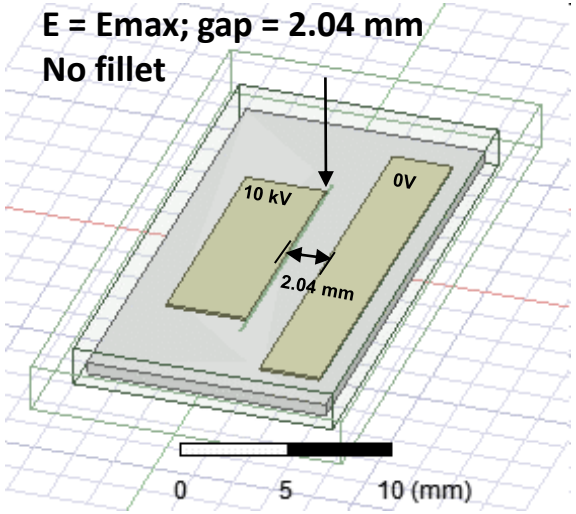
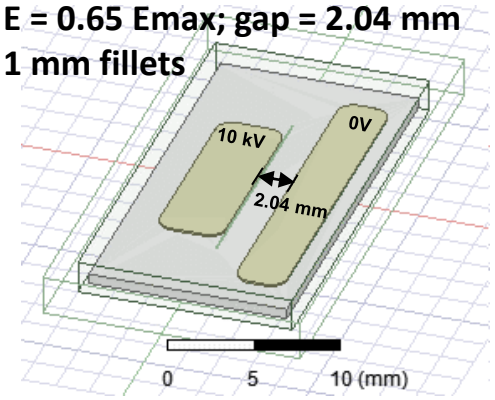
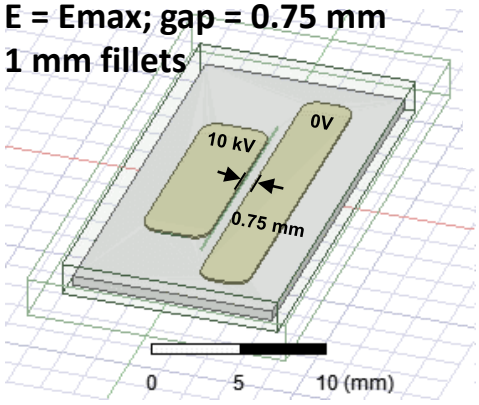
E = Emax; gap = 2.04 mm
No fillet



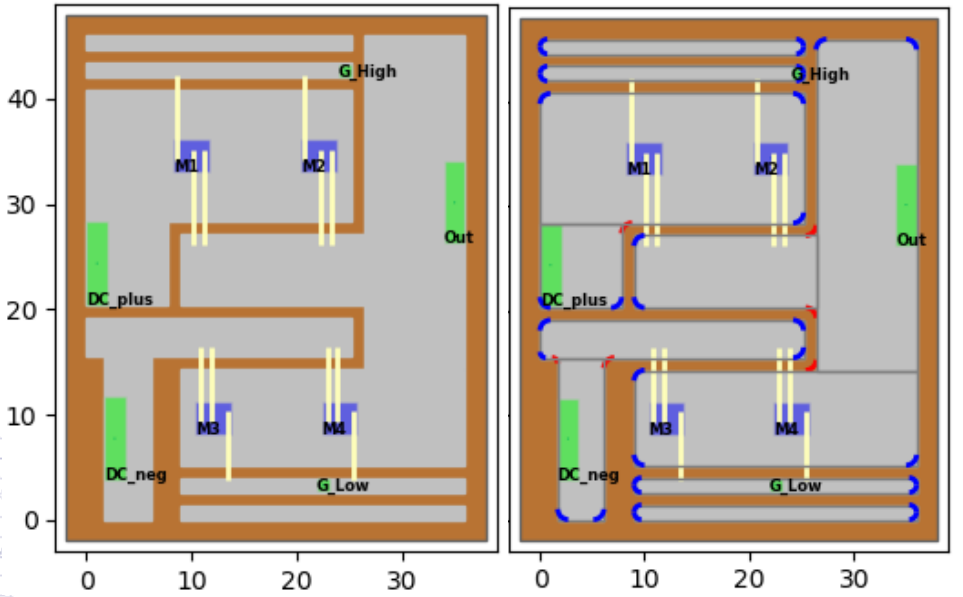
E = 0.65 Emax; gap = 2.04 mm
1 mm fillets



E = Emax; gap = 0.75 mm
1 mm fillets



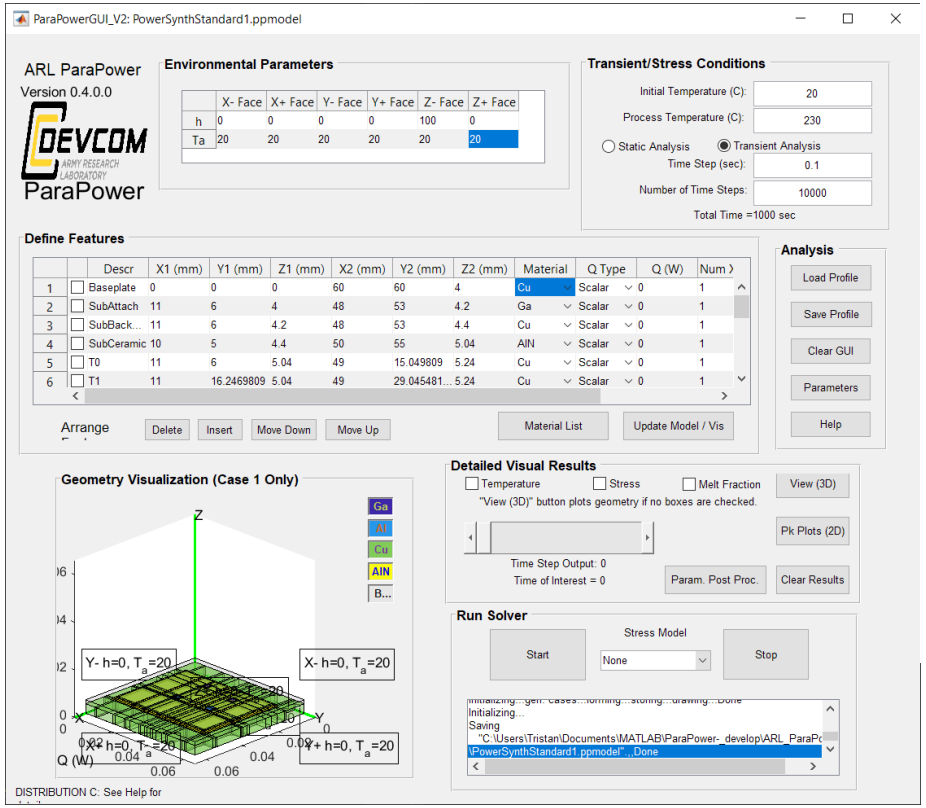
Application of fillets in PowerSynth

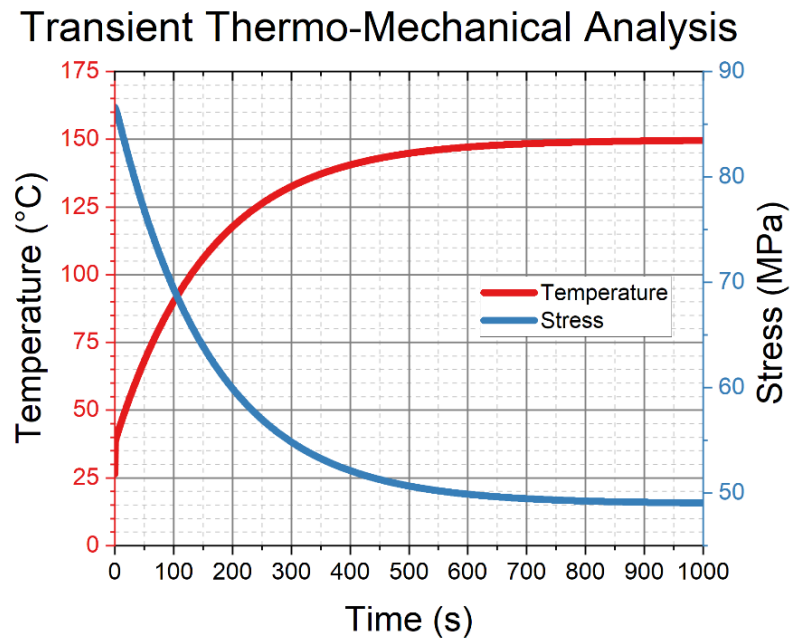


← Gap can be reduced to about 40% of the original gap if fillets are applied.

ParaPower Overview

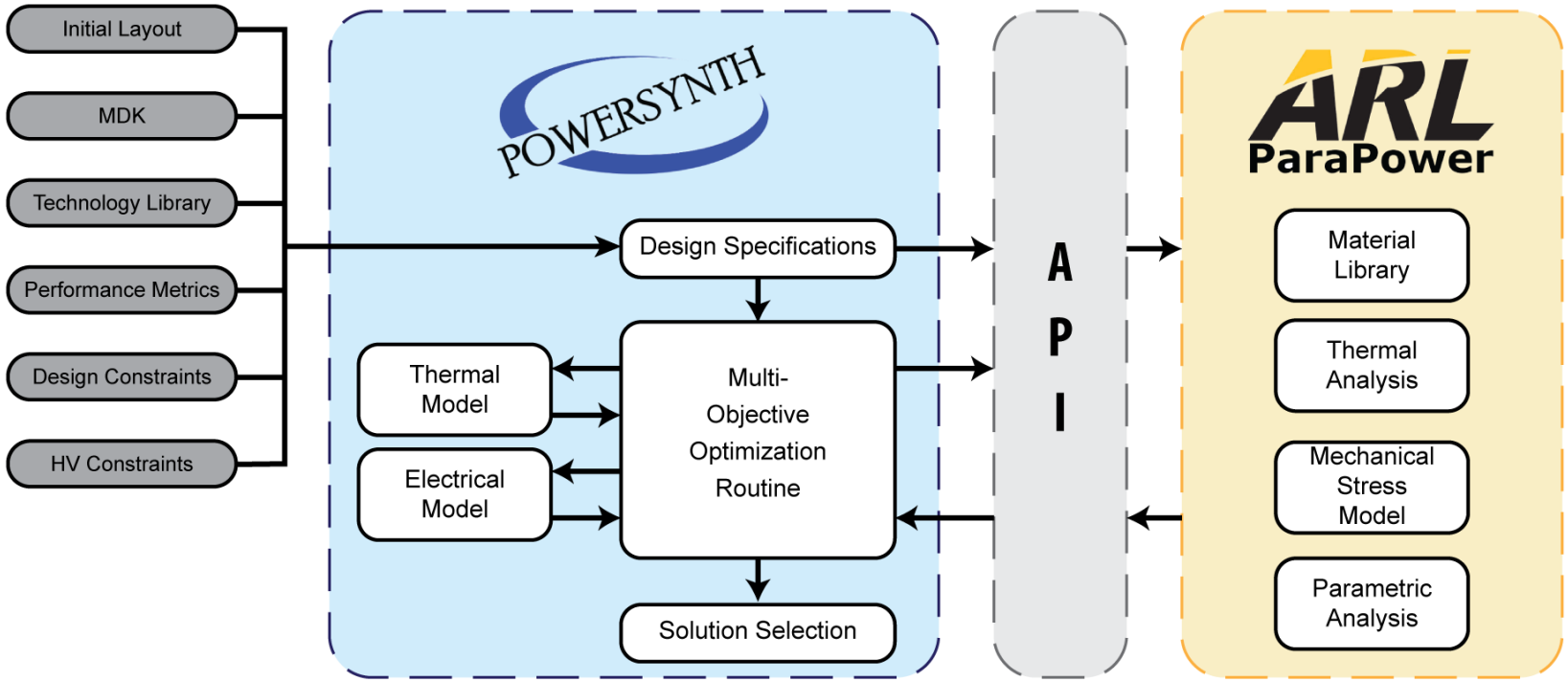
- Open source co-design tool by US Army Research Lab
- Fast, thermo-mechanical analysis of power electronics modules
- Parametric analysis tools
- Support for phase change materials





https://github.com/USArmyResearchLab/ParaPower

PowerSynth⇄ParaPower Integration

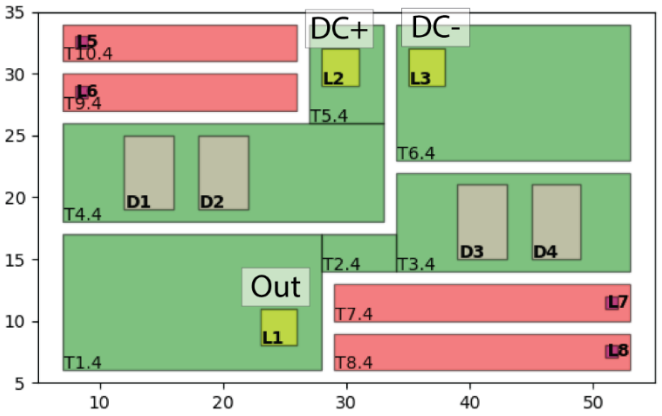


API to leverage:

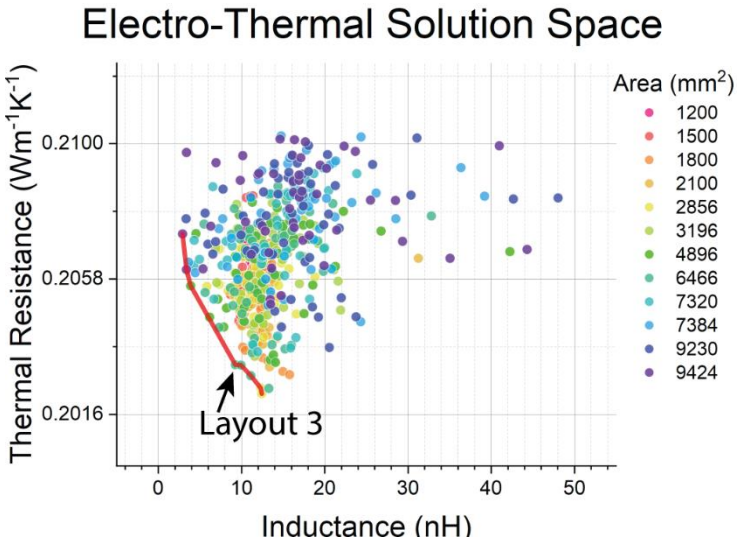
- PowerSynth layout generation and electrical parasitics extraction
- ParaPower 3D thermo-mechanical analysis

Co-Design Example (1/2)

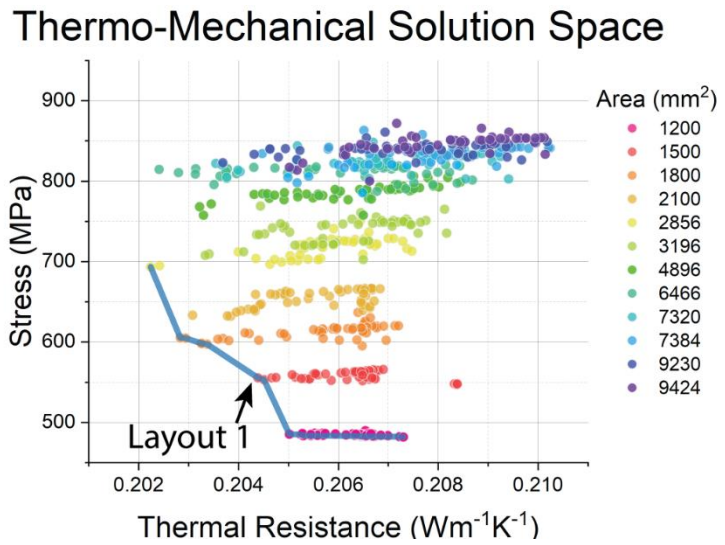
- Half bridge layout
- Loop inductance from DC+ to DC-
- 10 W power dissipation/die, 25°C backside temperature
- 230°C process temperature, -40°C minimum ambient temperature

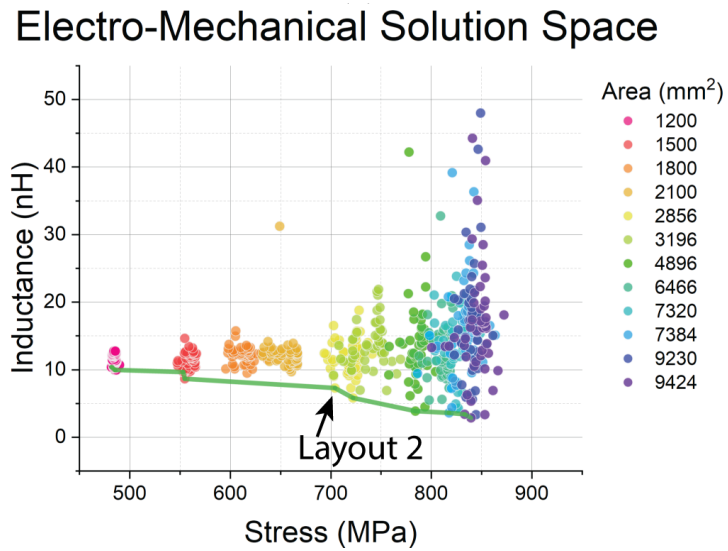


Initial Layout

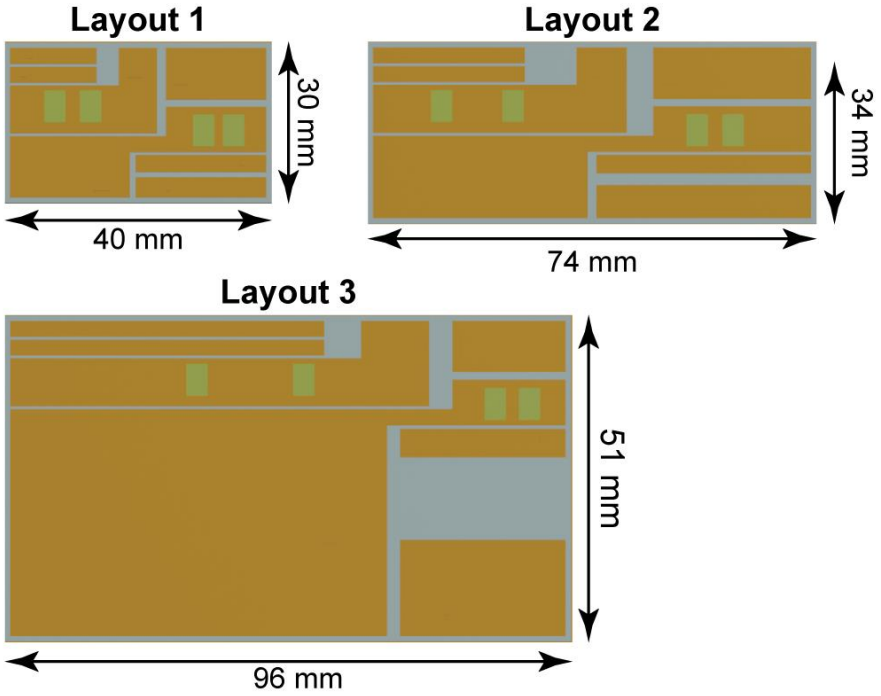


Pareto frontier results for different solution spaces





Co-Design Example (2/2)



Layouts selected from solution space

Layouts performance metrics

	Dimensions (mm)	Inductance (nH)	R_{TH} ($Wm^{-1}K^{-1}$)	Stress (MPa)
Layout 1	40x30	9.93	0.204	556
Layout 2	74x34	7.23	0.206	704
Layout 3	96x51	9.26	0.203	816

Summary and Future Work

- EDA tools for power electronics gaining momentum
- Integration of PowerSynth and ParaPower enhances capabilities of both
- Layout engine updated with high voltage reliability constraints
- Co-design methods being used to rapidly explore design space tradeoffs
- Continued development:
  - Enhance models
  - Toward 3D and heterogeneous layout
  - Reliability assessment

Acknowledgements

Power Optimization of Electro Thermal Systems (POETS) An NSF ERC

US Army Research Laboratory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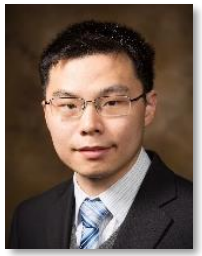
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