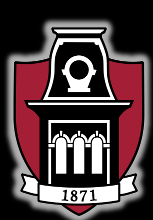

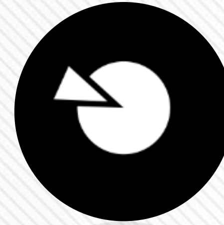

Holistic 2.5D Chiplet Design Flow: A 65nm Shared-Block Microcontroller Case Study

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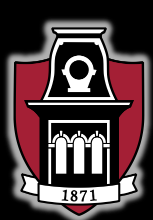

Introduction

- **Package becomes increasingly critical in post-Moore's Law era**
  - Sizes of modern chips (GPU, FPGA, TPU, etc.) are reaching reticle limit.
  - 2.5D and 3D packages provide high bandwidth and compact size.
- **2.5D packaging opens a new door of opportunities**
  - Novel design techniques like plug-and-play, Drop-in, Hardware security
  - Heterogenous integration capabilities (AMD EPYC2, Intel Lakefield)
- **Need for a cross-boundary package-aware design strategy**
  - Interactions between the package and chiplets are significant
  - Optimization goals for 2.5D system are different: inductance, signal integrity, thermal, reliability, cost, turnaround time, flexibility, etc
- **Objectives**
  - Application of our holistic design flow in commercial technologies.
  - Design and study of a system designed in our flow in 65nm technology.

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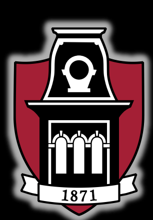

Traditional vs. Our Holistic Flow

- **Traditional die-by-die design flow can achieve the shortest possible 2.5D system design time using off-the-shelf chiplets.**
  - Cannot ensure the maximum performance and highest reliability
  - Package routing can get complicated due to its pin-dominated nature
- **Need for a cross-boundary package-aware design strategy:**
  - Timing optimization needs to be accounted in a holistic way
  - Partition tool needs to be aware of the delay introduced by redistribution layers (RDLs) with detailed parasitic extraction
  - Package planning tool may need to modify chiplet pin arrangement to optimize RDL routing and package flooplan
  - Chiplet timing optimization steps need to be aware of package wires.
  - The analysis tool needs to consider the chiplets and package interactions altogether.

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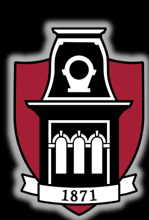
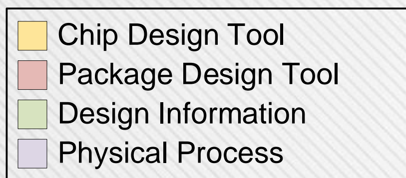
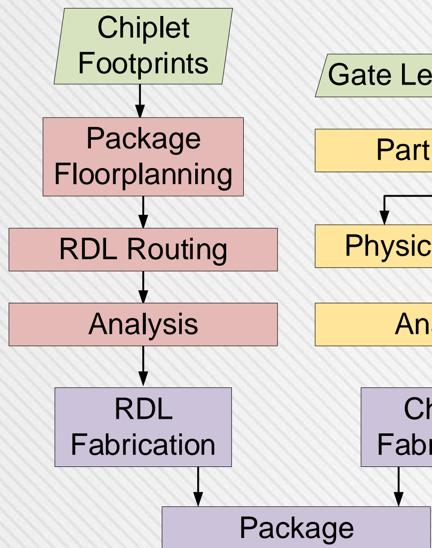
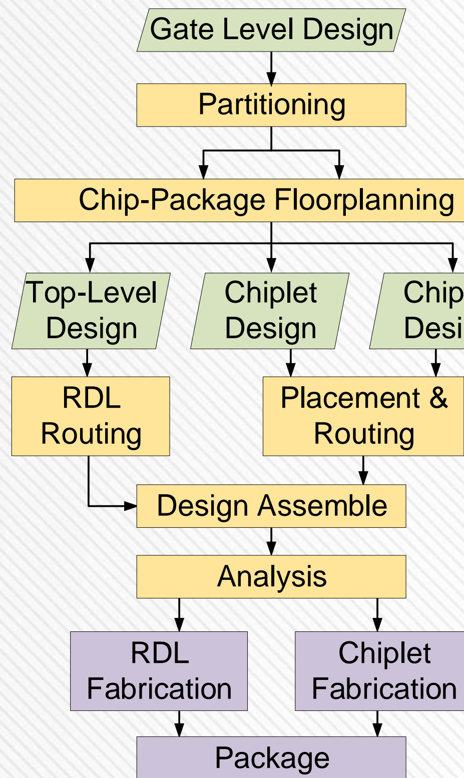


Traditional vs. Our Holistic Flow

- We incorporate the missing necessary interactions between package and chiplets during design, optimization and analysis steps.







Holistic top-level planning of the entire system

Maintaining parallelism in implementation of individual component

Capturing interactions among all the components of the system in optimization and analysis

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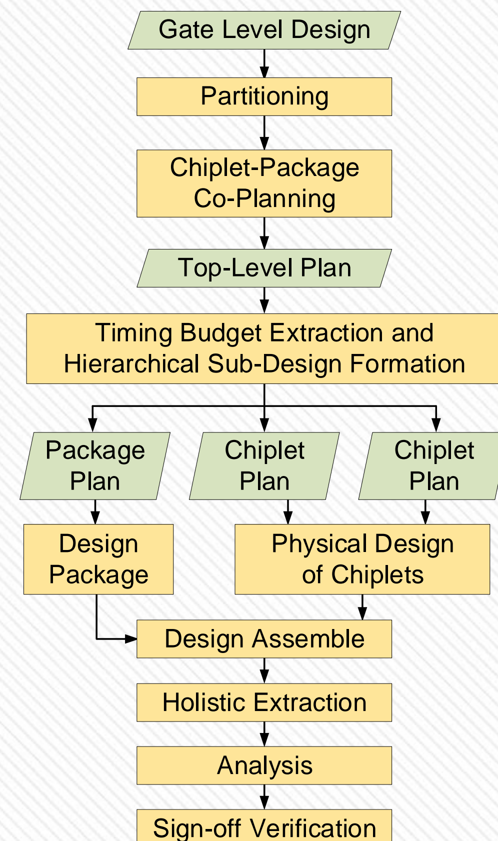
Overall Flow

- **Our flow consists of partitioning, top level planning, individual implementation of components, design assembly and analysis.**
  - Gate-level netlist is generated by synthesis tool.
  - The system is partitioned into chiplets.
  - Chiplet-Package co-planning determines the package floorplan and chiplet pin configurations.
  - Top-Level plan consists of package floorplan, RDL routing, chiplet pin configurations.
  - Chiplets and package are implemented independently with top-level constraints
  - Everything is assembled for overall optimization and verification



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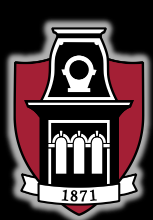

MCU Architecture and Partitions

- **System architecture of proof-of-concept design**
  - **Microcontroller system based on ARM Cortex-M0 core**
  - **16KB RAM with some common peripheral devices**

System architecture

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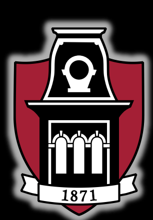
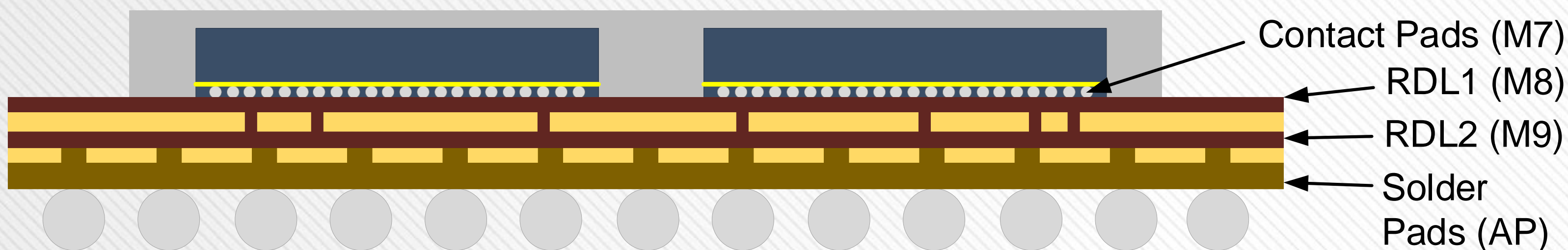


Technology Settings

- We use TSMC 65nm as our PDK and ARM IP for implementation
  - M1-M6 used for chiplet internal routing
  - Standard Cells and Memory compiler from ARM
- We modify the top three layers to include 2.5D package RDLs
  - Dimensions are similar to the TSMC 2.5D InFO technology

Layer	Purpose	Width	Spacing
M1-M6	Intra-Chiplet routing	Original	Original
M7	AP	5 µm	5 µm
M8	RDL1	5 µm	5 µm
M9	RDL2	5 µm	5 µm
AP	Solder Pads	Original	Original



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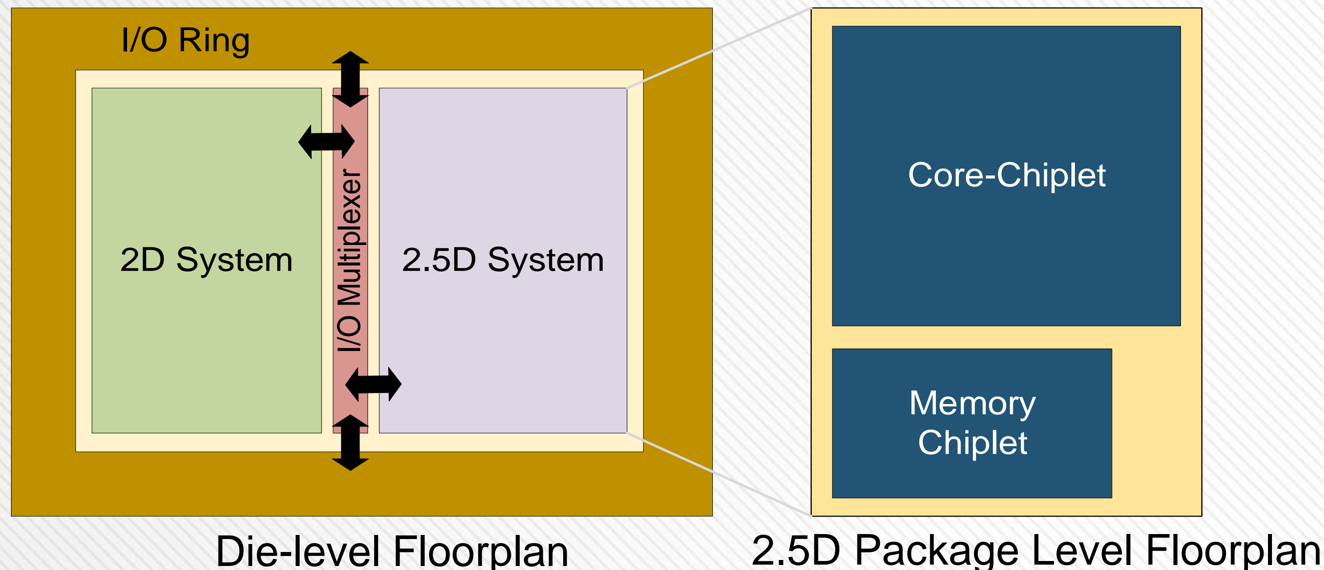
Shared Die Tape-Out Plan

- **2.5D system and the reference 2D system are designed to be taped out in a single die**
  - Shared die tape-out is performed to save pin area and fulfill minimum area requirement of the foundry.
  - Two systems share the same I/O ring.
  - An I/O multiplexer module controlled from outside decides which system can communicate to the I/O ring.



Die-level Floorplan

2.5D Package Level Floorplan

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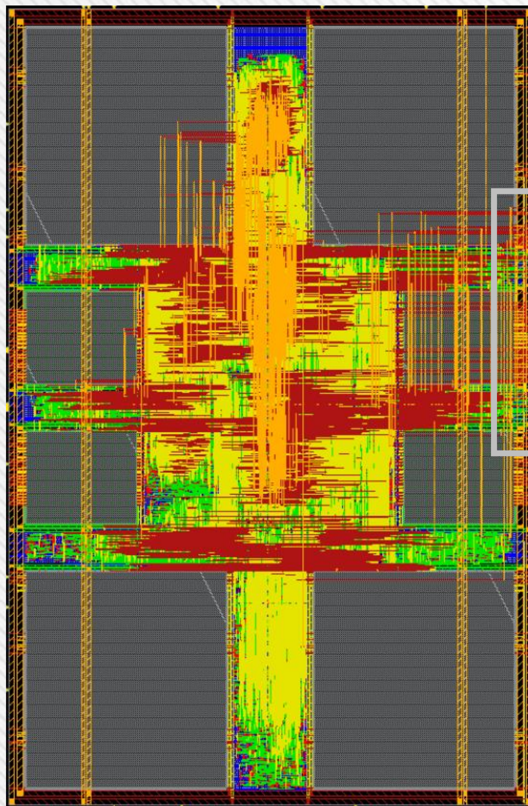
Reference 2D Design

- **For comparative study, we implemented the microcontroller as a 2D system using conventional 2D chip design flow**
  - Only with 16KB mem flavor



External I/Os connected to the I/O muxing module

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Chiplet Partitions

- **The partition tool needs to account for package RDL wires while exploring solutions.**
- **We partition the system into two chiplets.**
  - We tested different partition schemes and settled with an architecture-aware partition scheme.
  - We selected this custom partition scheme to meet the area required to accommodate the pins of both chiplets.

Parameter	Core-Chiplet	Mem-Chiplet
Logic Cell #	20,206	0
Macros	6	2
Area (μm^2)	179,655	72,826
Area Balance	71.16%	28.84%
Pin Count	141	101

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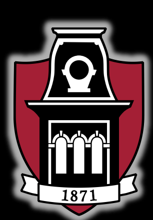
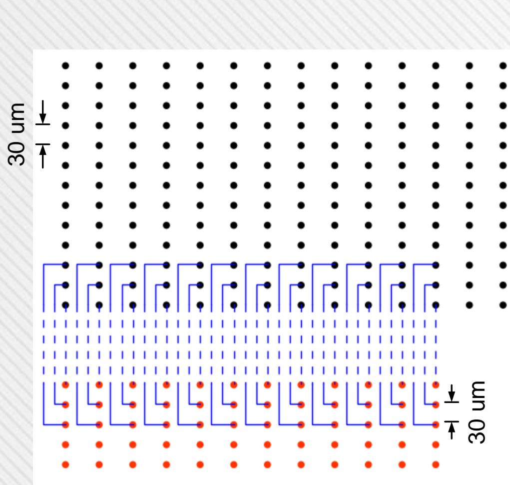
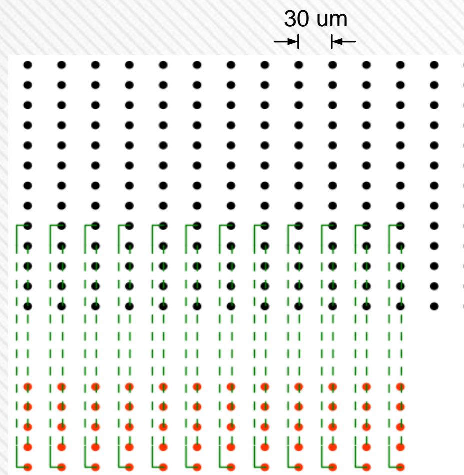


Co-Planning Strategy

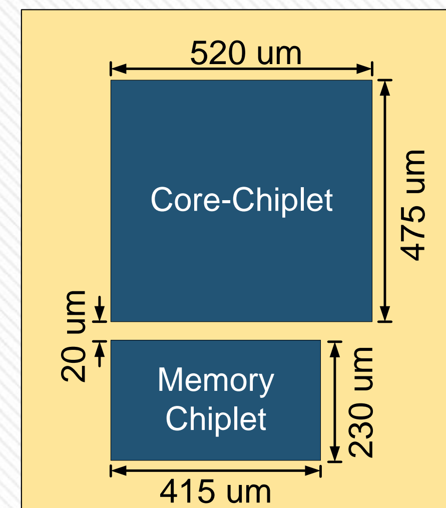
- **In-house RDL planning tool implements our planning strategy.**
- **Our planning strategy,**
  - Package floorplan and routing are determined before signal assignment
  - Use of short & straight wires to route the chiplet pins
  - Signal assignments of pins are determined from package routing and timing report from synthesis tools



RDL1 Routing



RDL2 Routing



Package Floorplan

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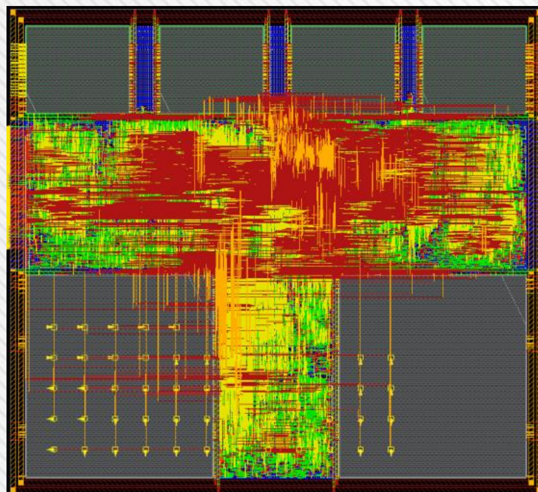
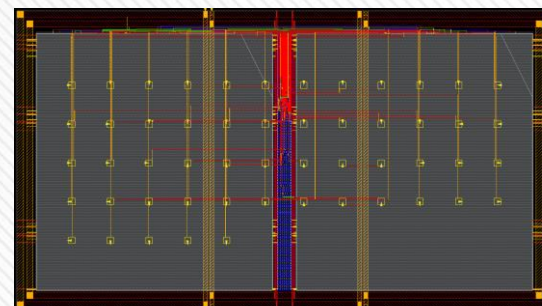
Placement & Routing

- **After top level planning, chiplets and package are implemented independently with constraints propagated from top-level**
  - Top level design is divided into hierarchical sub-designs.
  - Chiplet floorplan and PDN are finalized.
  - Chiplet implementation is the same as conventional 2D chip that includes power planning, placement, time design, routing and post routing optimizations.



Core-Chiplet



Mem-Chiplet

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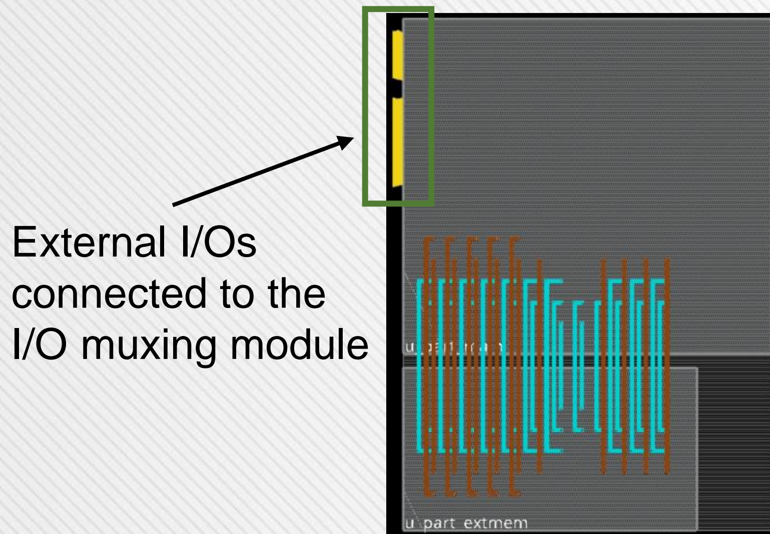
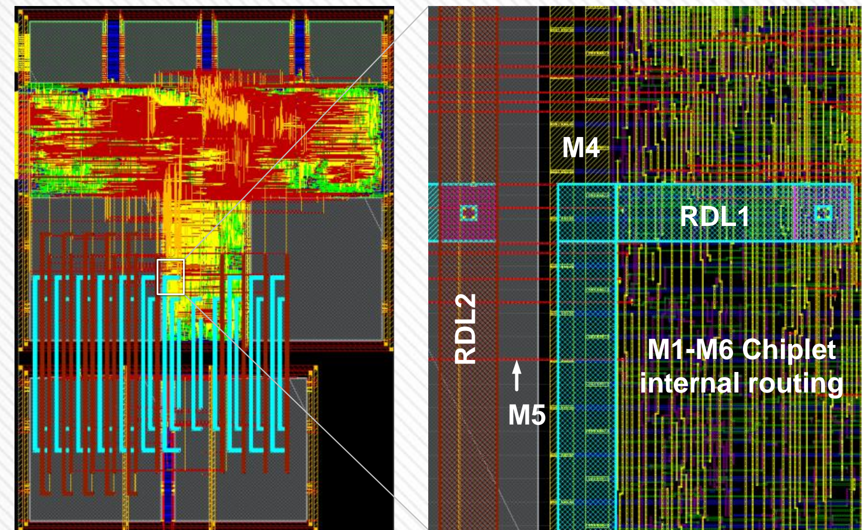
Package Design and Assembly

- **Package is implemented according to the top-level plan and assembled with chiplet desigs for holistic extraction.**
  - Only inter-chiplet signals are routed on the RDLs. Due to shared-die design, the external I/O are routed to the I/O multiplexing module and are routed separately on M7.
  - As the design environment has everything together, holistic extraction can capture all the interactions between chiplets and package.



Package Design



Assembled System

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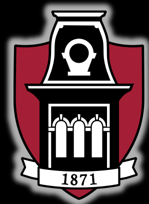

Chiplet-Package Interactions

❑ Chiplet-Package coupling capacitance

- The columns for RDL1 and RDL2 show the coupling capacitance between package layers and chiplet layers (in fF).
- M6 and RDL1 are extracted with considerations from the other side
- RDL1 has greater coupling with M5 compared to M6
- This extraction result can be utilized to optimize signal integrity

	M1-M3	M4	M5	M6	AP	RDL1	RDL2
M1-M3	7505.6	2494.7	1389.3	38.0	0.3	13.3	0.8
M4	2494.7	2445.3	648.8	150.7	1.5	12.8	0.4
M5	1389.3	648.8	2756.7	90.0	1.3	40.8	4.9
M6	38.0	150.7	90.0	190.6	8.6	31.1	6.8
AP	0.3	1.5	1.3	8.6	0.0	0.6	0.1
RDL1	13.3	12.8	40.8	31.1	0.6	10.8	146.2
RDL2	0.8	0.4	4.9	6.8	0.1	146.2	33.8

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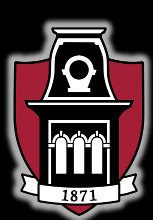

2D vs 2.5D Systems Comparison

❑ Chiplet analysis results

- Analysis captures the impact of RDLs on system performance.
- Maximum system frequency of 2D system is 125 MHz
- For the 2.5D system the highest system frequency achieved is 100 MHz
- P&R tool inserted buffers to drive package wires
- The 27 cells in Mem-Chiplet are buffers driving the package wires.

Chip Design	2D System	Core Chiplet	Mem Chiplet
Standard Cells #	20,061	20,096	27
Total Chip WL	544.70	478.57	12.96
Die Size (µm x µm)	475 x 725	520 x 475	415 x 230
Frequency	125 MHz	100 MHz	
Chip Power	7.0 mW	5.12 mW	0.718 mW

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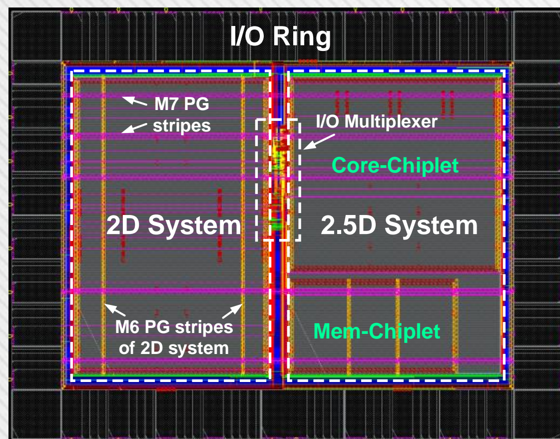
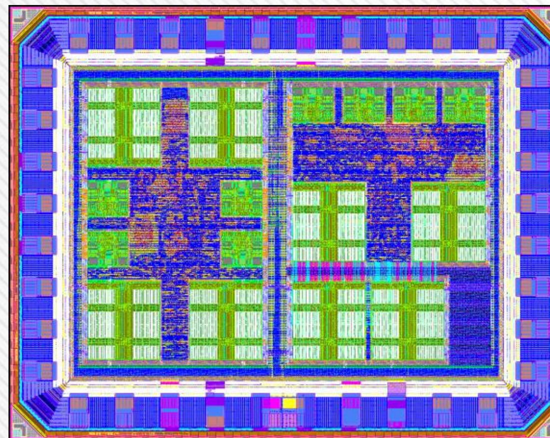
Die Level Design

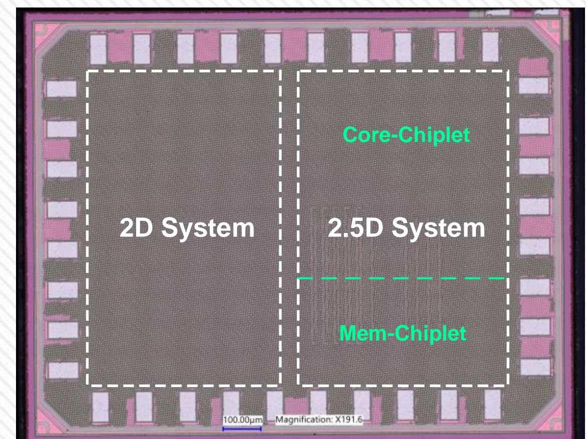
- For fabrication, we combined the 2D system and the 2.5D system containing both chiplets into a single GDS and performed sign-off verifications.
  - Had adjust the wide top wires (RDL) for antenna rules
  - Had to use special filler cells in the empty space between the systems and chiplets to satisfy some density requirements.



Die-level design



GDS for tapeout



Microscopic die-shot

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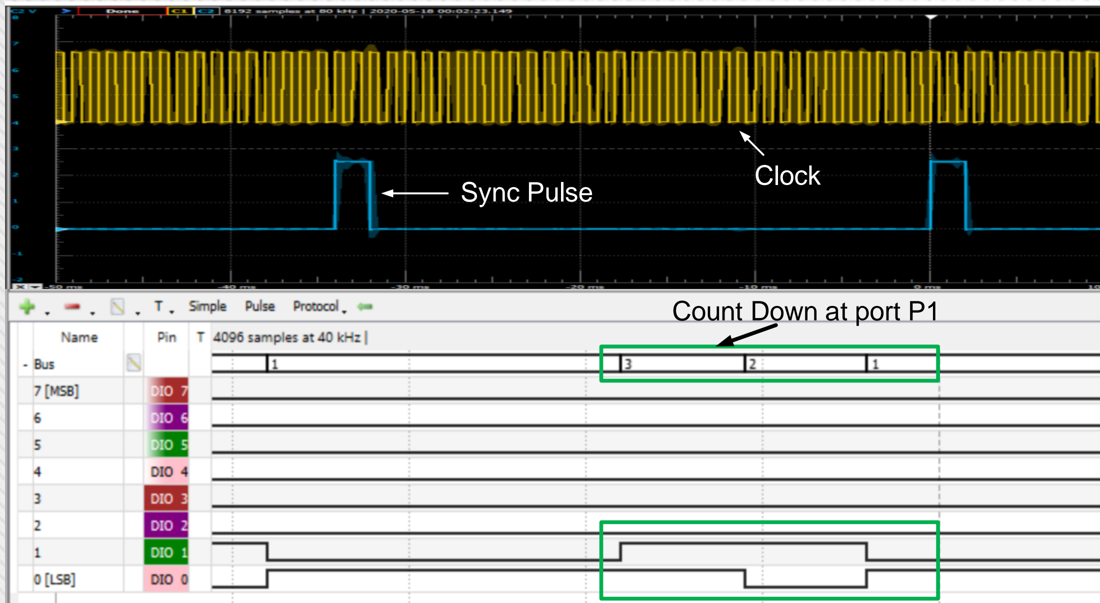
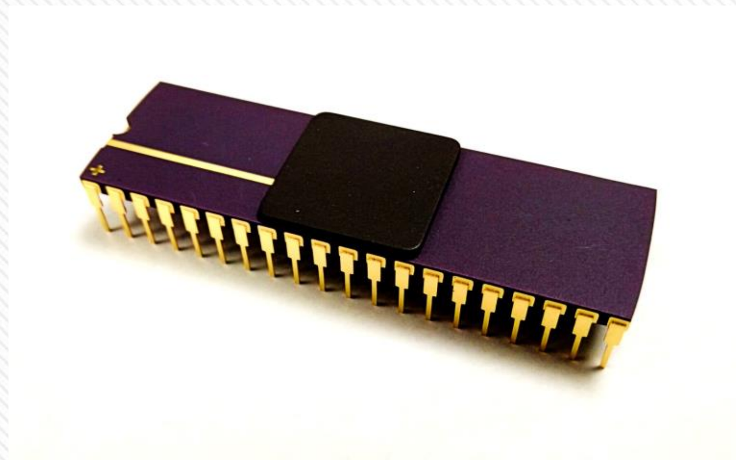
Chip Testing and Validation

- **Functionality test was performed on the fabricated chip**
  - Test vectors were generated and the chip responses were captured using a logic analyzer.
  - Both systems passed the verification tests.



Chip testing waveforms



Packaged Chip

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Conclusions & Future Work

❑ Conclusions

- Chiplet-Package interactions need to be considered in 2.5D systems
- Our flow effectively captures the impact of RDLs in optimization and analysis steps.
- It incorporates necessary interactions between package and chiplet designs for holistic planning and optimization.
- The flow is suitable for homogeneous designs with existing commercial chip design technolgies.

❑ Future Works

- Extending the flow to include design optimization steps that utilizes the holistic extraction results.
- New tools/techniques based on in-context design strategy need to be developed to support heterogeneous designs.
- Chiplet-Package inductance impact on PPA and noise

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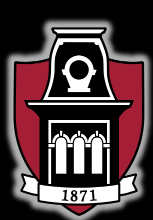

Thank You

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