Physical Design Automation for High-Density 3D Power Module Layout Synthesis and Optimization

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Manual Design Flow

- Tedious and computationally expensive design flow

Our Approach: PowerSynth

- A software tool for the layout synthesis and optimization of multi-chip power modules [1].

Already demonstrated:
- 2D and 2.5D heterogeneous power module optimization capability.

To increase the power density:
- 3D heterogeneous power modules optimization are obvious.

Feature Update:
- 3D power module layout generation and optimization.

Three types of layouts handled by PowerSynth:
- 2D layout: One device layer with routing layers on the same substrate
- 2.5D layout: Multiple 2D designs connected on a supporting 2D plane
- 3D layout: Multiple device layers stacked vertically on the same substrate
PowerSynth 2 Methodology

- **Layout Representation:**
  - Multiple 2D layers connected with vertical vias

- **Data Structure and Algorithms:**
  - Hierarchical tree structure of corner-stitched planes

- **Layout Generation:**
  - Hierarchical constraint graphs
    - Guarantee DRC-clean solutions

- **Layout Optimization:**
  - Efficient models
    - Electrical/thermal/mechanical
  - Optimization algorithms
    - Tradeoff among multi-objectives

**High-level pseudocode:**

```
Read Input Script
Create a root node
Create group of layers connected with same via

For each group
  Create a sub-root in the tree containing via location
  For each layer
    Create HCS, VCS
    Create and Evaluate HCG, VCG

For each ancestor from leaf to root
  Perform bottom-up constraint propagation
  Evaluate root node and compute available space

For each sub-tree from root to leaf
  Perform top-down location propagation

Evaluate independent nodes

HCS/VCS: Horizontal/Vertical Corner Stitch
HCG/VCG: Horizontal/Vertical Constraint Graph
```
3D Layout Generation Results

2D vs. 3D Performance Comparison:

- Initial layout:
  - Half-bridge MCPM: 2D structure (left), 3D structure (right)

<table>
<thead>
<tr>
<th>Performance Metric</th>
<th>2D</th>
<th>3D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Loop Inductance (@100 KHz)</td>
<td>15.93 nH</td>
<td>6.104 nH</td>
</tr>
<tr>
<td>Max Temperature</td>
<td>332.15 K</td>
<td>370.29 K (single-side cooling)</td>
</tr>
</tbody>
</table>

(a) 2D layout (b) 3D power loop, (c) high-side (Layer 1) and low-side (Layer 2) layers of 3D layout
3D Layout Optimization Results

3D Layout Optimization:
- Initial Layout:
- Electro-thermal evaluation:
  - ParaPower [2] thermal model
  - FastHenry electrical model
- Optimization:
  - 2400 solutions are generated
  - 0.08s per solution generated

Solution Space:

<table>
<thead>
<tr>
<th>ID</th>
<th>L (nH)</th>
<th>T (K)</th>
<th>Size (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.44</td>
<td>334.11</td>
<td>34.5 × 16.5</td>
</tr>
<tr>
<td>B</td>
<td>1.22</td>
<td>328.13</td>
<td>37.0 × 24.0</td>
</tr>
<tr>
<td>C</td>
<td>2.43</td>
<td>324.62</td>
<td>42.0 × 26.5</td>
</tr>
</tbody>
</table>

Conclusions:

- Generic and efficient algorithms to handle both intra-layer and inter-layer connections.
- Able to handle arbitrary number of layers in an efficient manner.
- This methodology is generic and can be extended towards cabinet-level optimization.

Future Work:

- Update the algorithm for generic 3D layout cases and validate through measurements.
- Customized optimization algorithm to find a better tradeoff among multiple objectives.
- PowerSynth v2.0 release.