Physical Design Automation for High-Density 3D Power Module Layout Synthesis and Optimization

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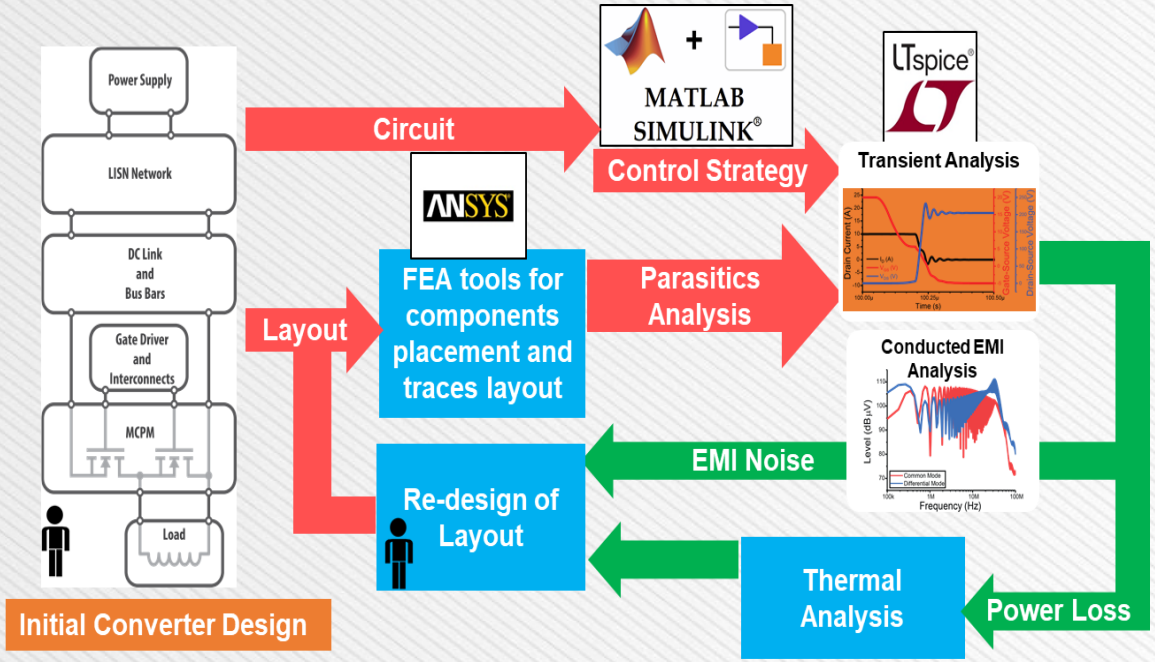
Traditional vs. Automatic Design Flow

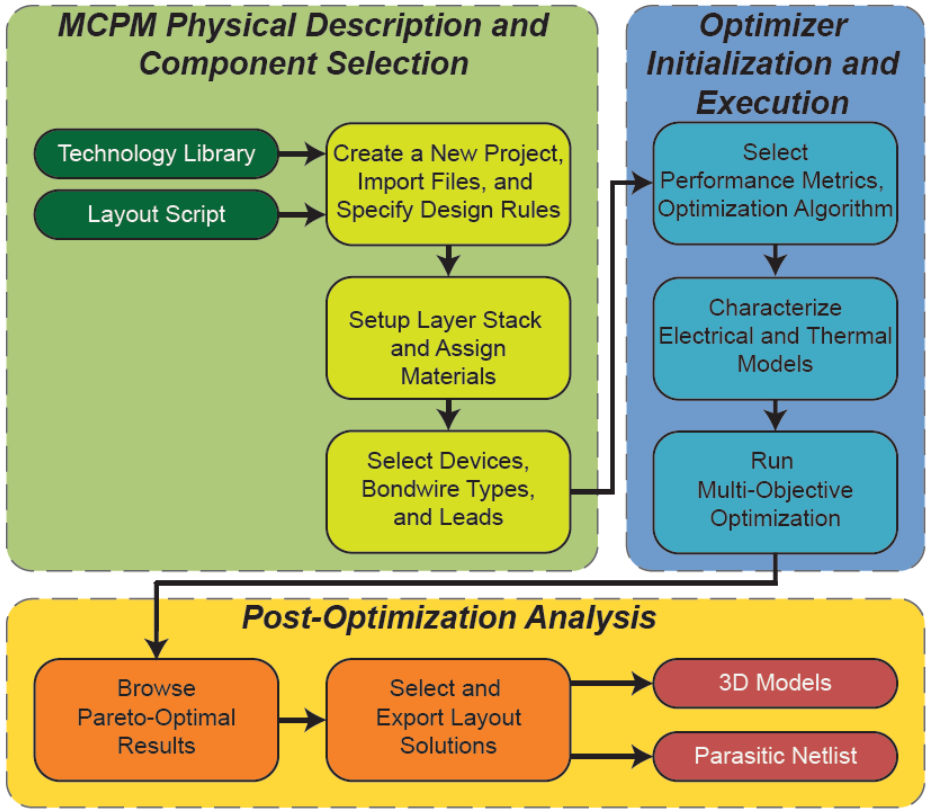
❑ Manual Design Flow

- Tedious and computationally expensive design flow



❑ Our Approach: PowerSynth

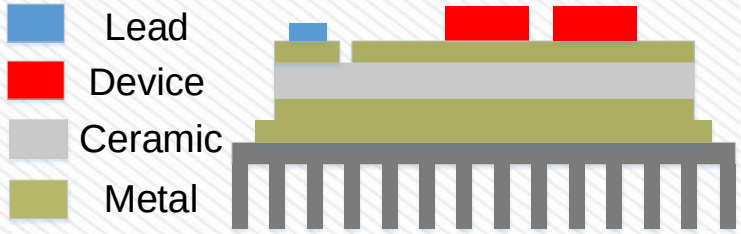
- A software tool for the layout synthesis and optimization of multi-chip power modules [1].



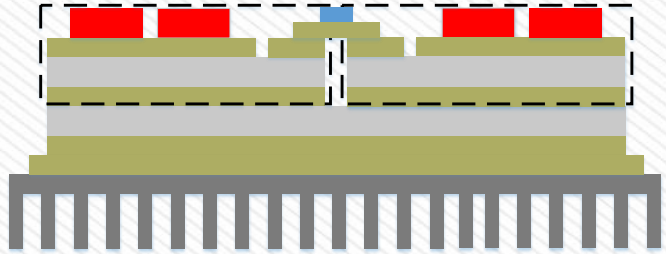
[1] T. M. Evans *et al.*, "PowerSynth: A Power Module Layout Generation Tool," in *IEEE Transactions on Power Electronics,2019*.

PowerSynth 2 Introduction

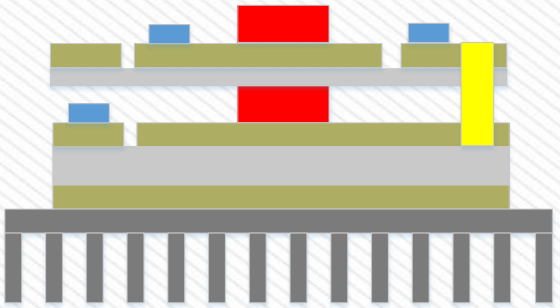
- **Already demonstrated:**
  - 2D and 2.5D heterogeneous power module optimization capability.
- **To increase the power density :**
  - 3D heterogeneous power modules optimization are obvious.
- **Feature Update:**
  - 3D power module layout generation and optimization.



2D Half-Bridge Power Module


2.5D Full-Bridge Power Module

- **Three types of layouts handled by PowerSynth:**
  - 2D layout: One device layer with routing layers on the same substrate
  - 2.5D layout: Multiple 2D designs connected on a supporting 2D plane
  - 3D layout: Multiple device layers stacked vertically on the same substrate


3D Half-Bridge Power Module

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PowerSynth 2 Methodology

❑ Layout Representation:

- Multiple 2D layers connected with vertical vias

❑ Data Structure and Algorithms:

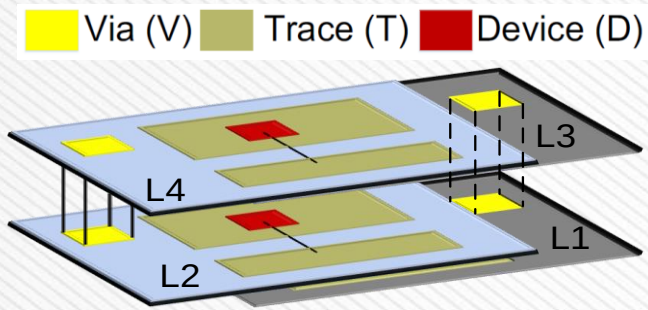
- Hierarchical tree structure of corner-stitched planes

❑ Layout Generation:

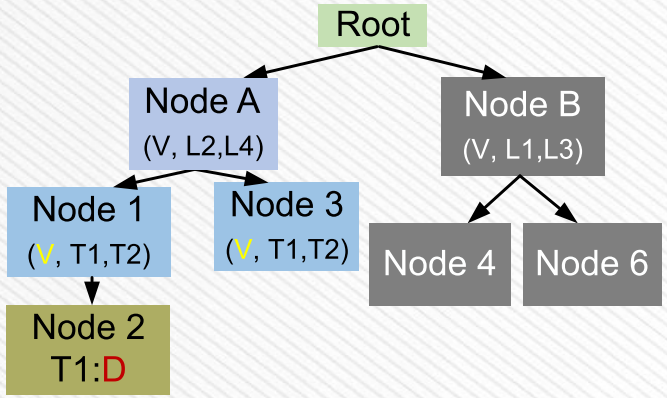
- Hierarchical constraint graphs
  - Guarantee DRC-clean solutions

❑ Layout Optimization:

- Efficient models
  - Electrical/thermal/mechanical
- Optimization algorithms
  - Tradeoff among multi-objectives



Sample 3D structure



Tree representation

❑ High-level pseudocode:

Read Input Script
Create a root node
Create group of layers connected with same via

For each group
  Create a sub-root in the tree containing via location
  For each layer
    Create HCS, VCS
    Create and Evaluate HCG, VCG

For each ancestor from leaf to root
    Perform bottom-up constraint propagation
Evaluate root node and compute available space

For each sub-tree from root to leaf
    Perform top-down location propagation

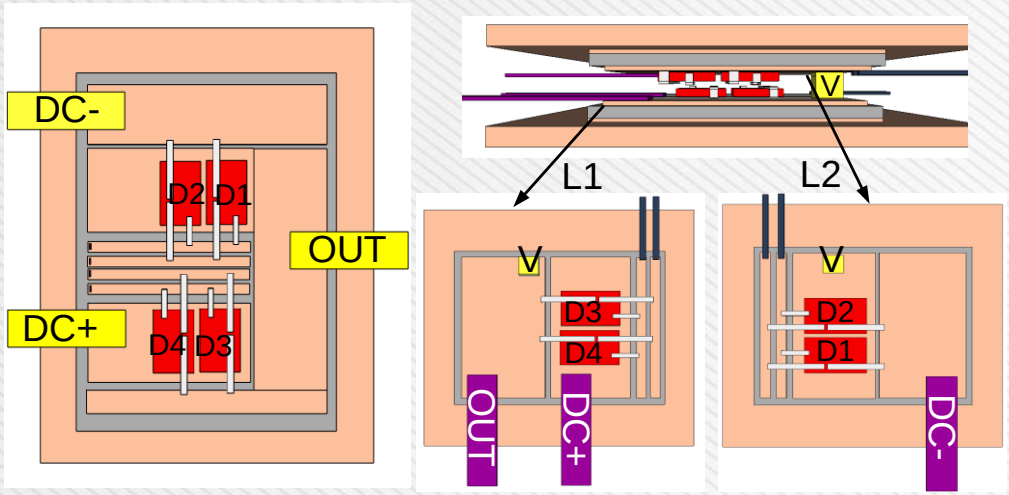
Evaluate independent nodes

HCS/VCS: Horizontal/Vertical Corner Stitch
HCG/VCG: Horizontal/Vertical Constraint Graph

3D Layout Generation Results

❑ 2D vs. 3D Performance Comparison:

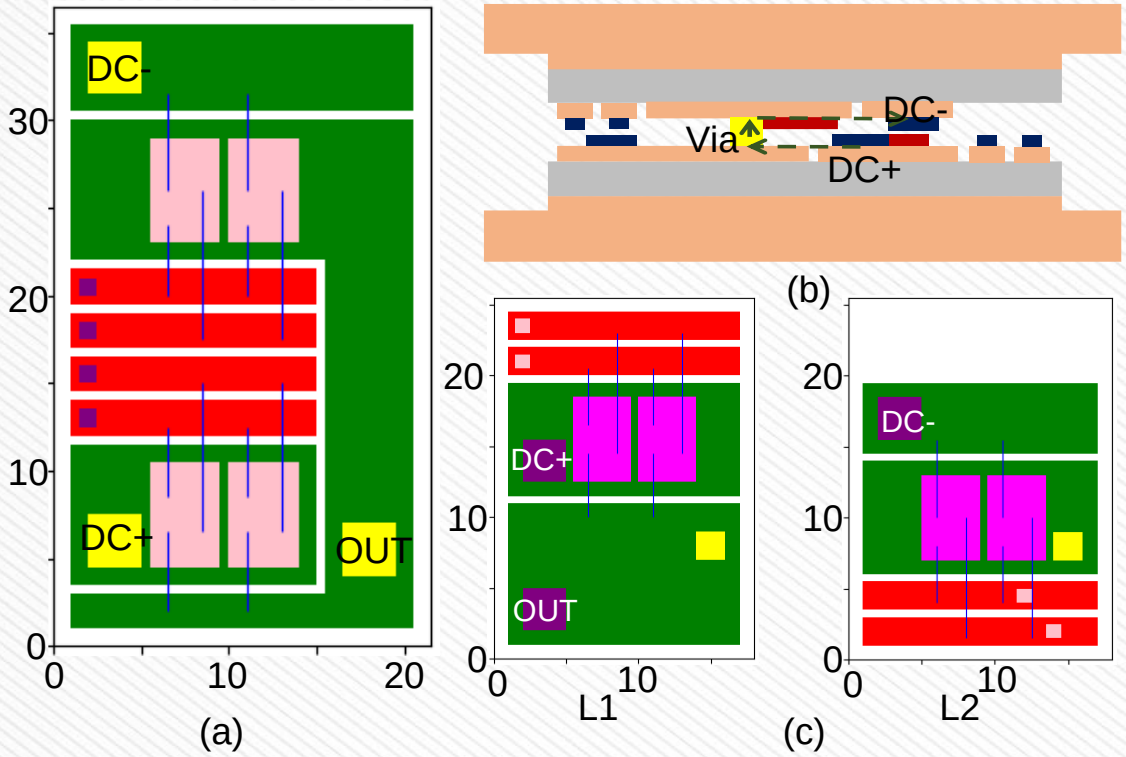
- Initial layout:



Half-bridge MCPM: 2D structure (left), 3D structure (right)

Performance Metric	2D	3D
Loop Inductance (@100 KHz)	15.93 nH	6.104 nH
Max Temperature	332.15 K	370.29 K (single-side cooling)
		328.38 K (dual-side cooling)

- Min-sized Result:

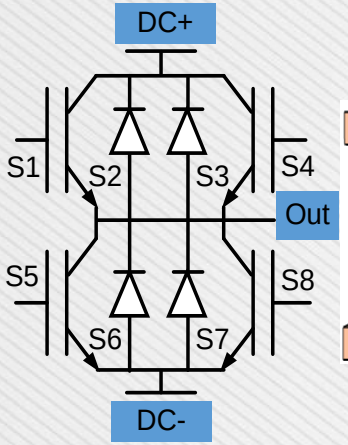


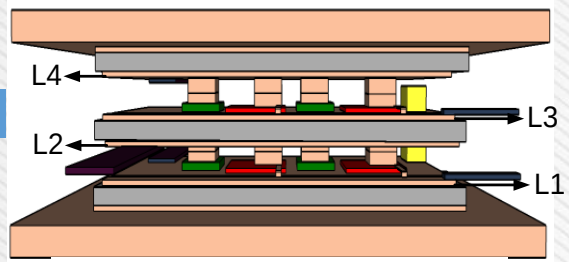
(a) 2D layout (b) 3D power loop, (c) high-side (Layer 1) and low-side (Layer 2) layers of 3D layout

3D Layout Optimization Results

3D Layout Optimization:

- **Initial Layout:**



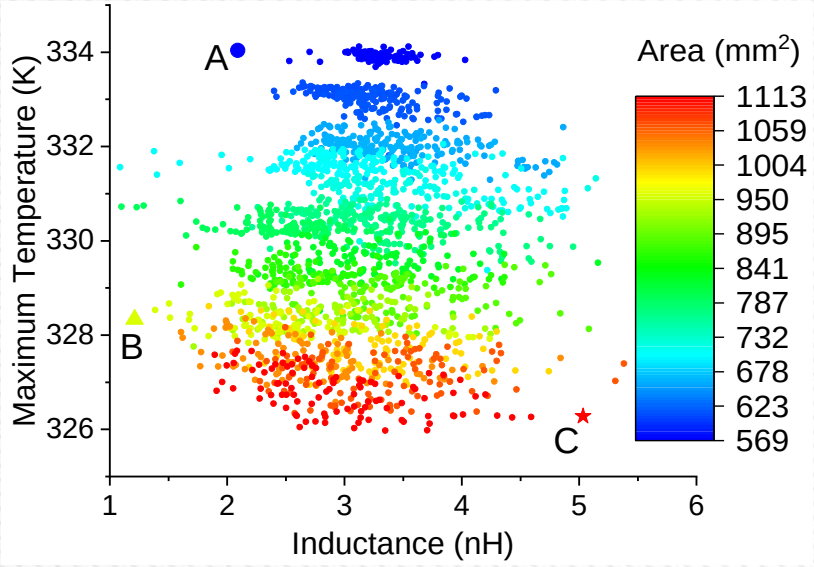


3D Structure

- **Electro-thermal evaluation:**
  - ParaPower [2] thermal model
  - FastHenry electrical model
- **Optimization:**
  - 2400 solutions are generated
  - 0.08s per solution generated

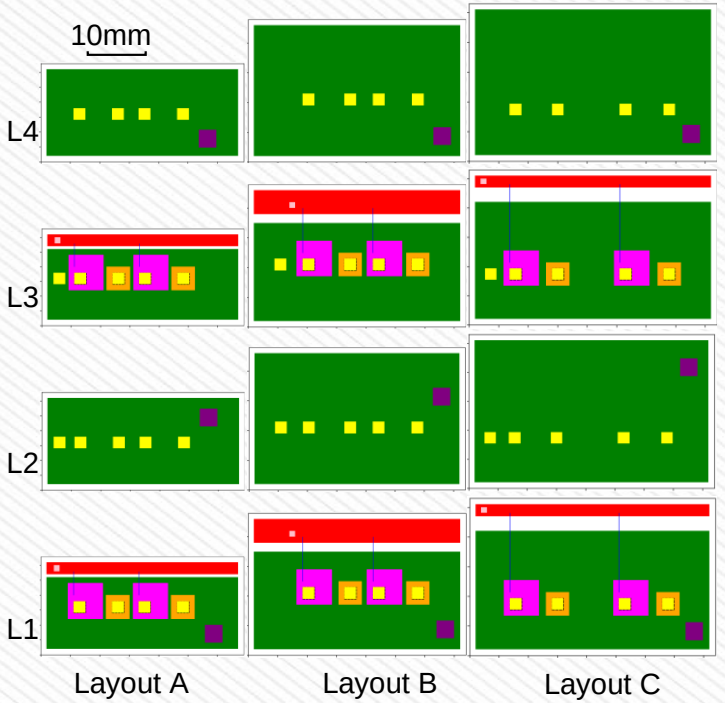
[2] "ARL ParaPower" :https://github.com/USArmyResearchLab/ParaPower

- **Solution Space:**



Performance values

ID	L (nH)	T (K)	Size (mm²)
A	1.44	334.11	34.5 × 16.5
B	1.22	328.13	37.0 × 24.0
C	2.43	324.62	42.0 × 26.5



Three selected layouts

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Conclusions and Future Works

❑ Conclusions:

- Generic and efficient algorithms to handle both intra-layer and inter-layer connections
- Able to handle arbitrary number of layers in an efficient manner.
- This methodology is generic and can be extended towards cabinet-level optimization.

❑ Future Work:

- Update the algorithm for generic 3D layout cases and validate through measurements.
- Customized optimization algorithm to find a better tradeoff among multiple objectives.
- PowerSynth v2.0 release