DEVELOPMENT OF EDA TECHNIQUES FOR POWER MODULE EMI MODELING AND LAYOUT OPTIMIZATION

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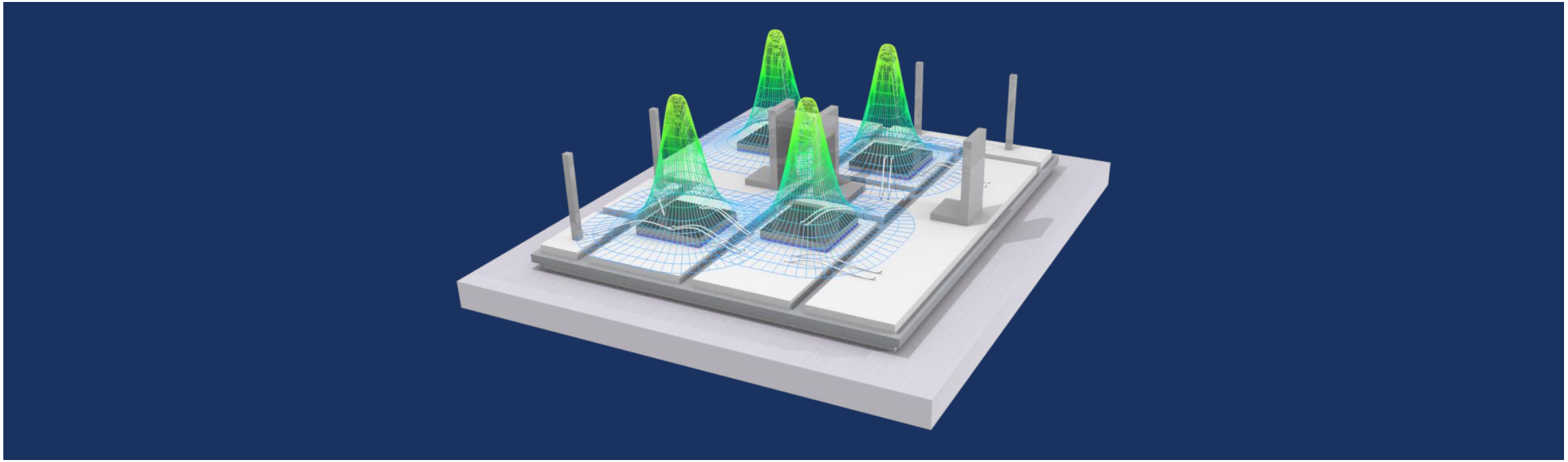


OUTLINE

- PowerSynth: an EDA tool for rapid power module layout optimization
  - Significance, applications, and challenges
  - Software overview
- Conducted EMI modeling in PowerSynth
  - High frequency equivalent circuits
  - Differential and common mode modeling
- Test Case and Comparison
  - DM and CM layout optimization
  - Comparison using simulated EMI testbench
- Conclusions

POWERSYNTH

MULTICHIP POWER MODULES (MCPM)

Applications

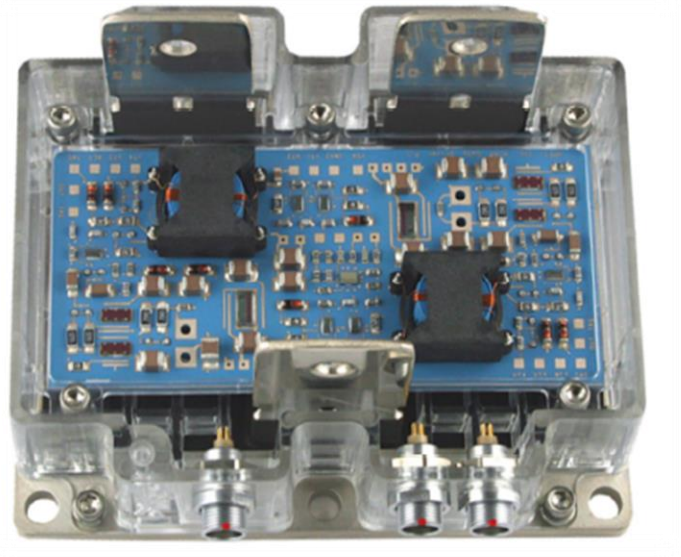
- Renewable energy
- Electric vehicles and traction
- Aerospace
- Industry

Advantages

- Integration of power and control circuitry
- Increased power density

Challenges

- Multidomain: electrical, thermal, mechanical
- Integration and EMC
- Design iteration



R&D 100 Award-Winning MCPM Design by UA and APEI

STATE OF THE ART AND CHALLENGES

Commercial Solutions

- Tools used to simulate electrical/thermal/mechanical/EMI
  - ICEPAK
  - Q3D
  - HFSS
  - COMSOL
  - SolidWorks
  - MATLAB & Simulink
  - FastHenry
- Common Methodologies
  - Finite Element Analysis (FEA)
  - Circuit Simulation
- Advantages
  - Increased accuracy for finer meshes
  - CAD import, data and image export

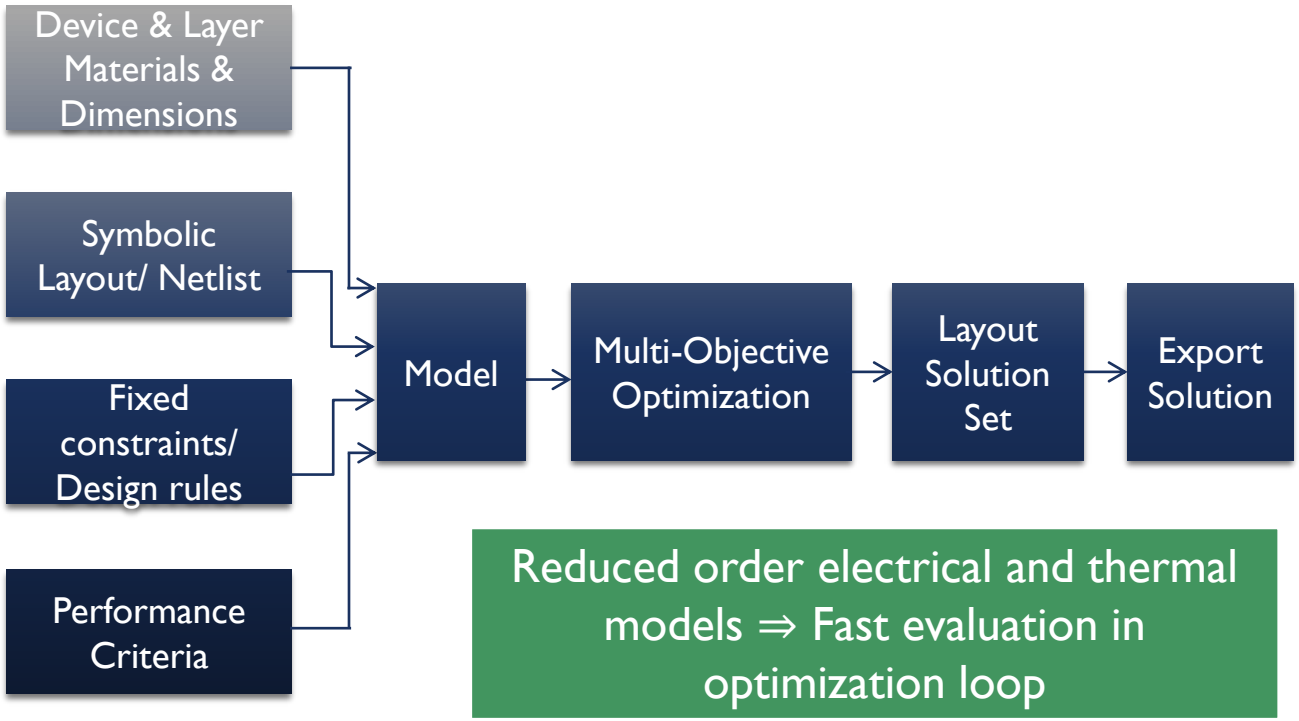
Challenges

- Long simulation times
  - To solve closed form higher order differential equations
  - To build finer mesh
  - To analyze all parameters on finer mesh
- Single solution at a time
- User attention/input required (to modify/optimize geometry/mesh if one option doesn't work)

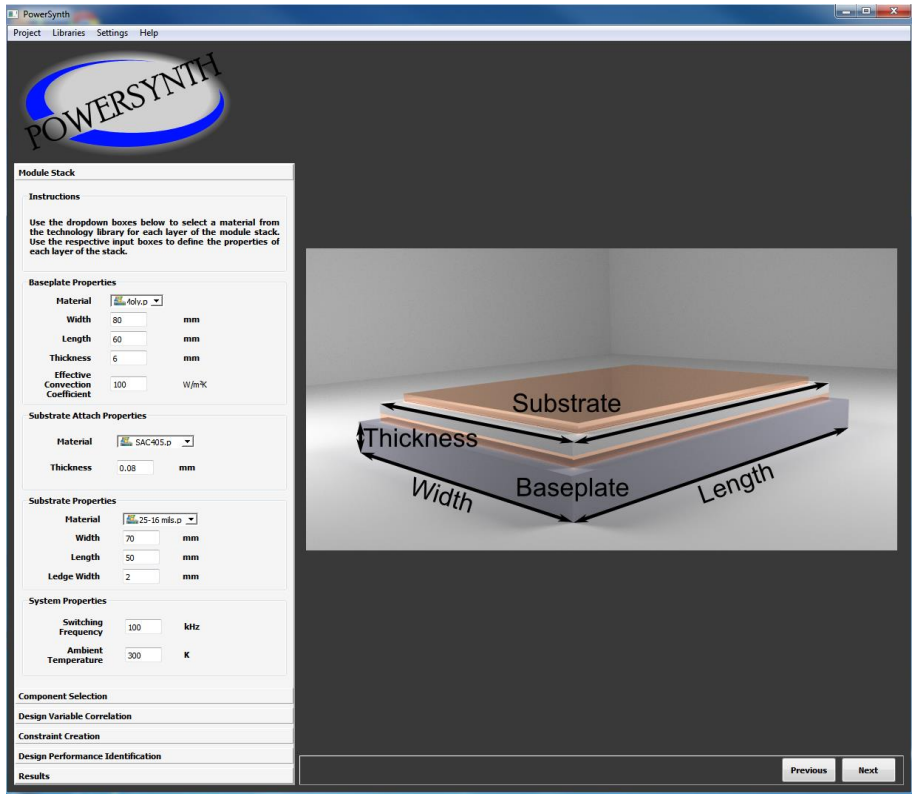
No full verification flow for power electronics exists

SOLUTION: POWERSYNTH

Multi-objective optimization tool for MCPM design

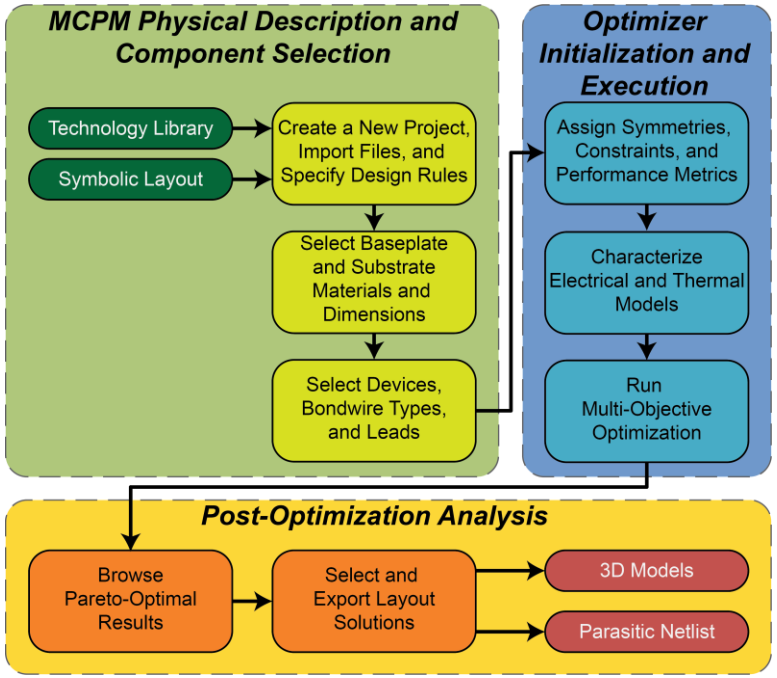


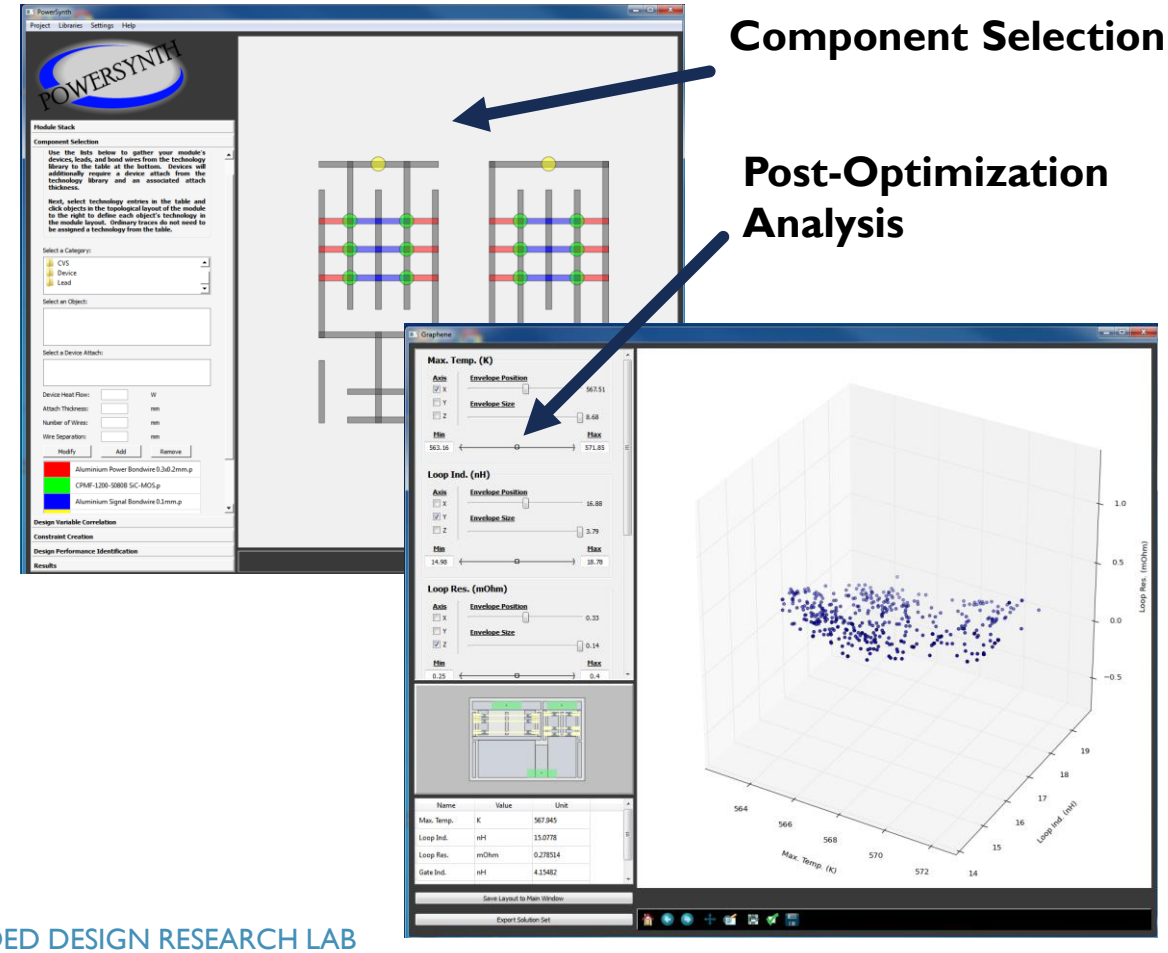
Reduced order electrical and thermal models ⇒ Fast evaluation in optimization loop



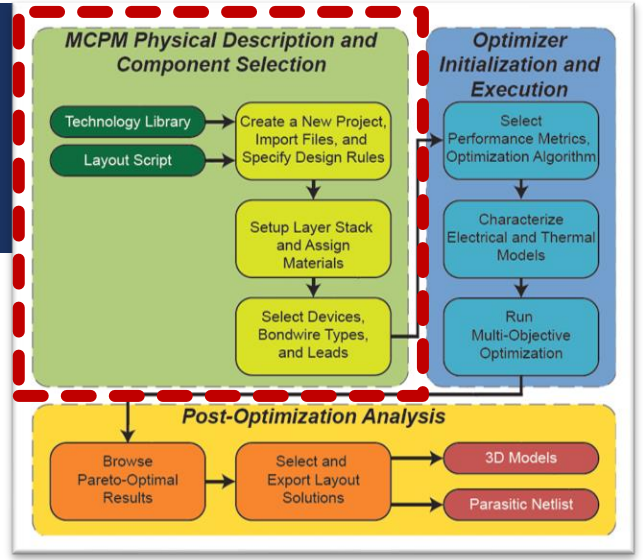
POWERSYNTH: OVERVIEW

Workflow Diagram

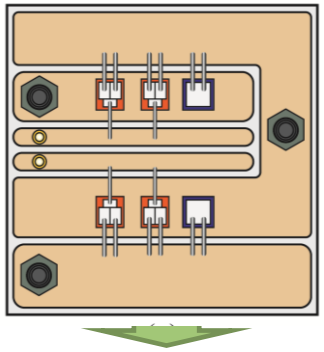




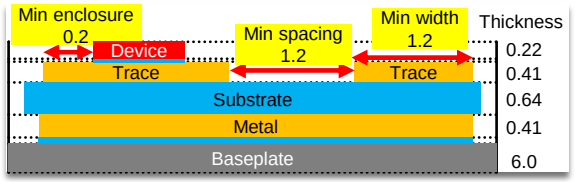
MCPM PHYSICAL DESCRIPTION AND COMPONENT SELECTION



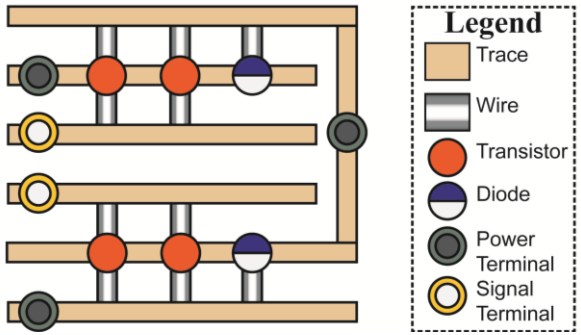
Physical Layout



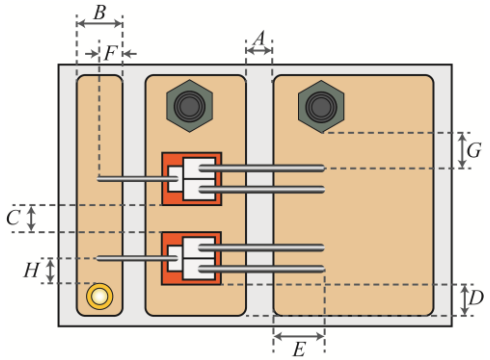
Layer Stack and Materials



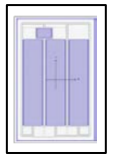
Symbolic Layout



MDK and Constraints

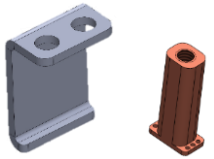


Component Selection



MOSFET

SBD



Terminals and Leads

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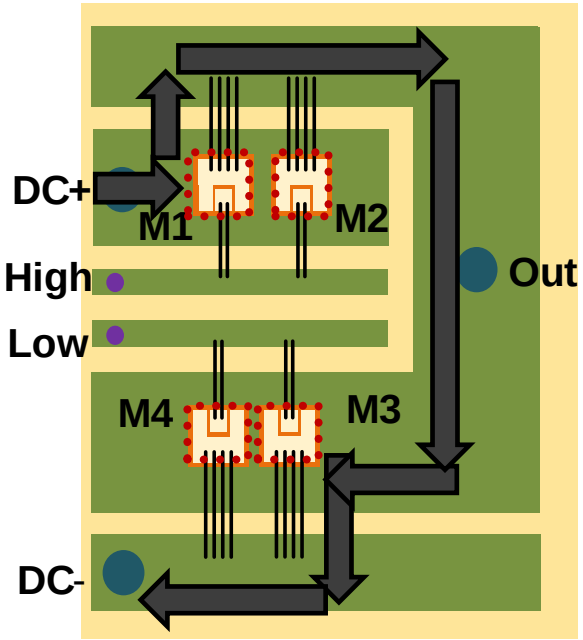
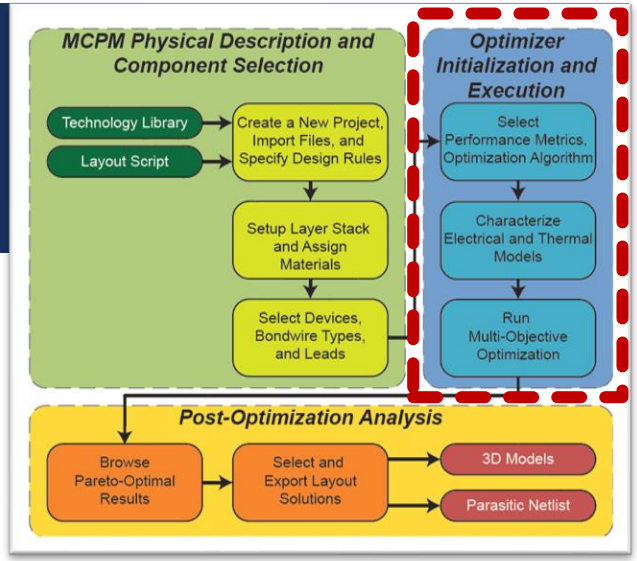
OPTIMIZATION

- **Four different optimization algorithms are available:**
  - **Non-guided randomization : Built-in solution generator**
  - **Evolutionary approach: NSGAII**
  - **Gradient-based approach: Weighted Sum Method**
  - **Stochastic approach: Simulated Annealing**
- **Performance metrics for optimization:**
  - **Electrical parasitics**
  - **Device temperature**

Conducted EMI now a cost function



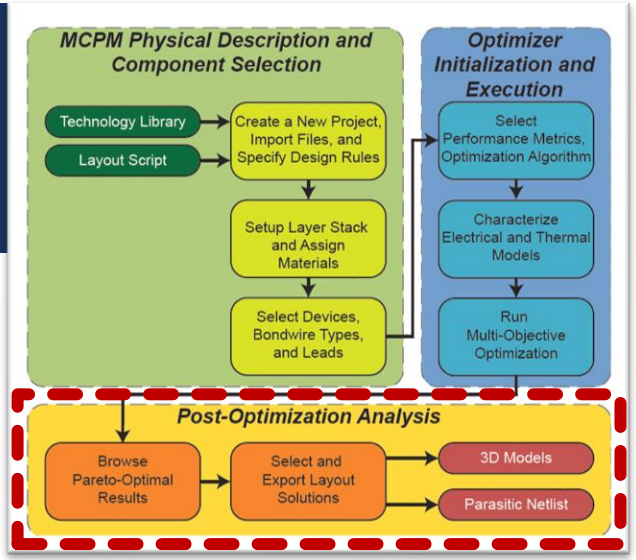
Power loop and heat sources

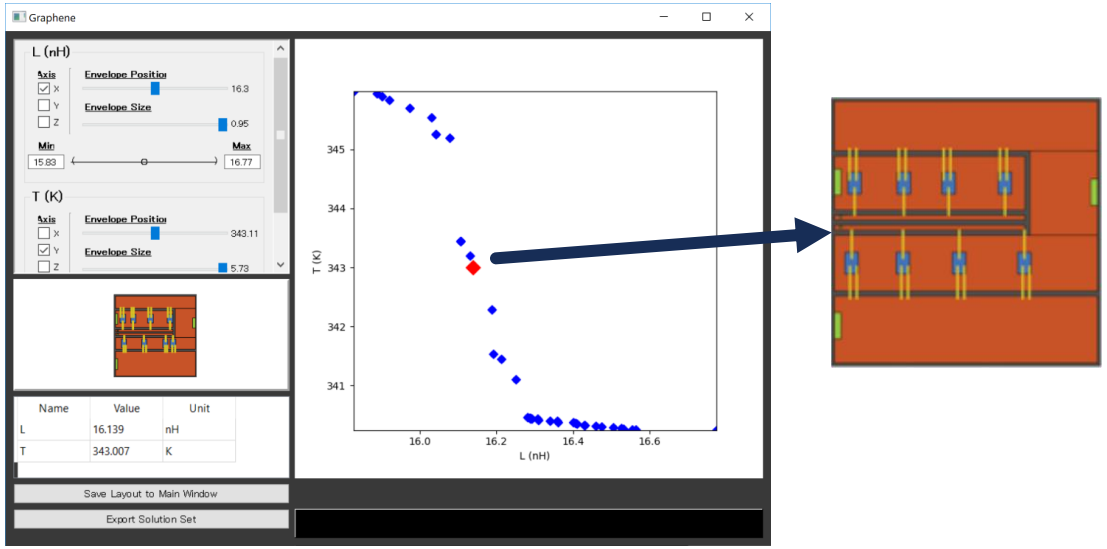


For more information on models:
T. M. Evans et al., "PowerSynth: A Power Module Layout Generation Tool," in IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5063-5078, June 2019. doi: 10.1109/TPEL.2018.2870346

MULTI-OBJECTIVE SOLUTION BROWSER

- View and sort through performance trade-off data
- Select solution which best suits design problem
- Supports 2D and 3D data visualization
- An envelope or window is used to sort through high dimensional data

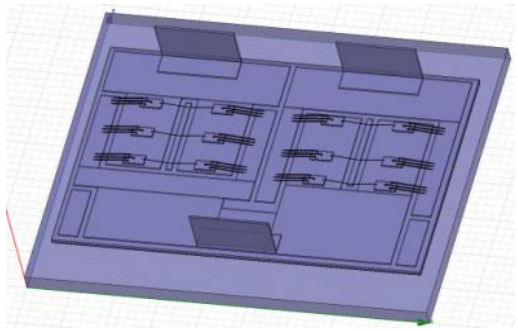




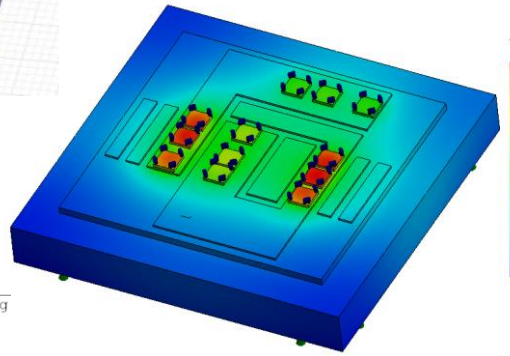
Browser for selecting layout solutions from a Pareto front with the options to save and export

DESIGN EXPORT

- Export to SolidWorks or Q3D
  - Further electrical and thermal verification through Q3D and SolidWorks
  - Export for manufacturing from SolidWorks
  - Export to simulated EMI testbench
- Export electrical parasitics netlist for circuit simulation



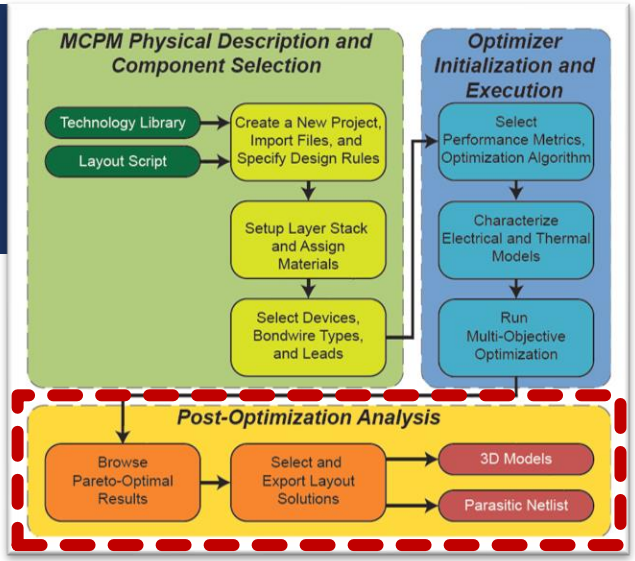
ANSYS Q3D



SolidWorks

```
1  .subckt X1 M2_D M1_D G_Low 0Out DC_plus DC_neg
2  R0 M2_D 0013 0.000297039959493
3  L0 0013 0014 5.55986694848e-09
4  C0 0014 0 1.62289047446e-11
5  R1 M2_D 0015 5.07336176071e-05
6  L1 0015 0016 4.78478054497e-10
7  C1 0016 0 3.08452745304e-12
8  R2 0017 0018 0.00176292565906
9  L2 0018 G_Low 2.15201688066e-08
10 C2 G_Low 0 1.24495697244e-11
11 R3 0017 0019 1e-06
12 L3 0019 0020 1e-12
13 R4 0017 0021 0.000139936684192
14 L4 0021 0022 9.07451993127e-10
15 C4 0022 0 1.08300628673e-12
```

Parasitics Netlist

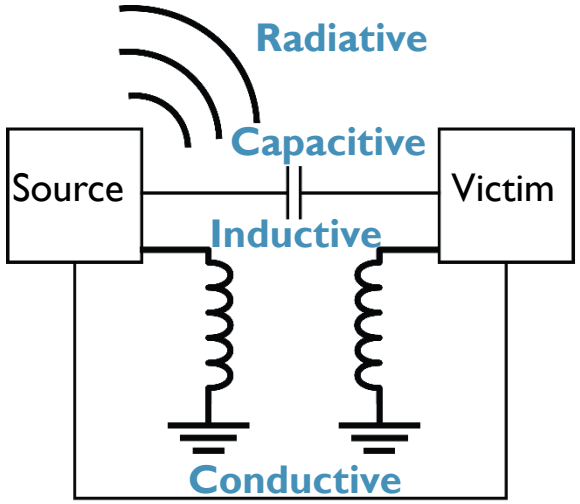


CONDUCTED EMI MODELING

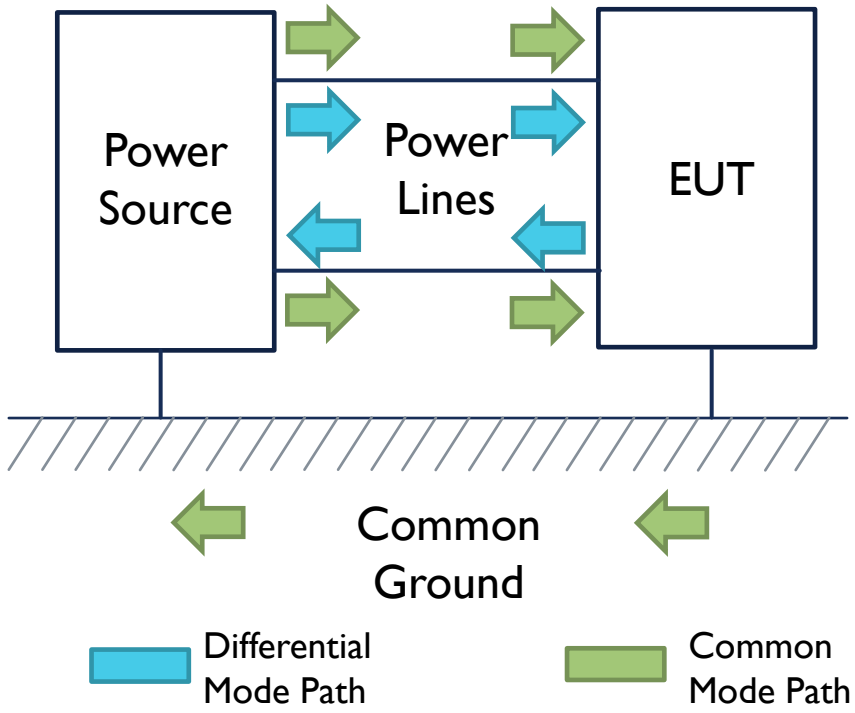
EMI IN POWER ELECTRONICS

- EMI can be radiated or conducted with several coupling paths
- Several standards exist for EMC based on application and region
- **Conducted noise paths:**
  - Common mode (CM) noise between power circuit and ground
  - Differential mode (DM) noise follows same path as power delivery
- Separating CM and DM
  - Accomplished with noise separator
  - Simplifies filter design
  - Aids in troubleshooting

Noise Propagation Mechanisms



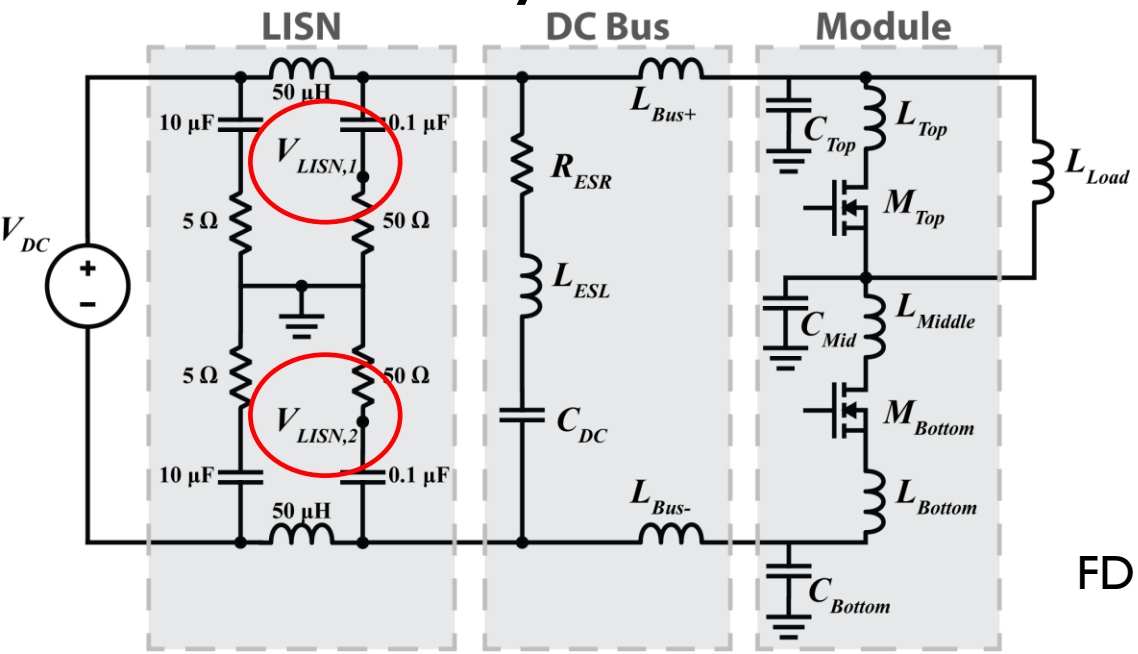
Conducted Noise Paths



How does power module layout affect conducted EMI?

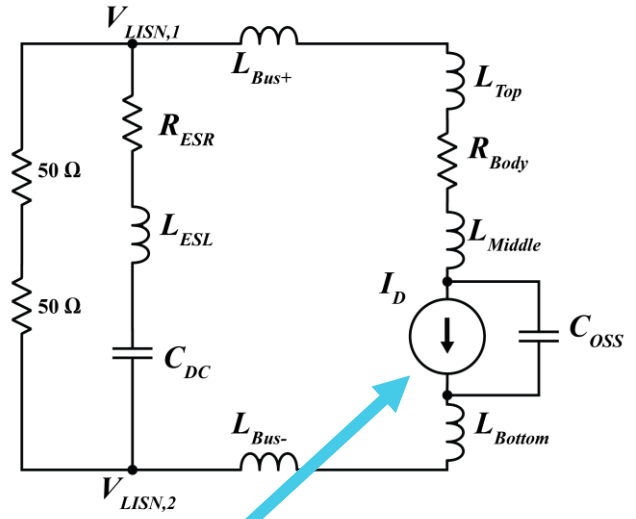
HIGH FREQUENCY EQUIVALENT CIRCUITS

Converter System Overview

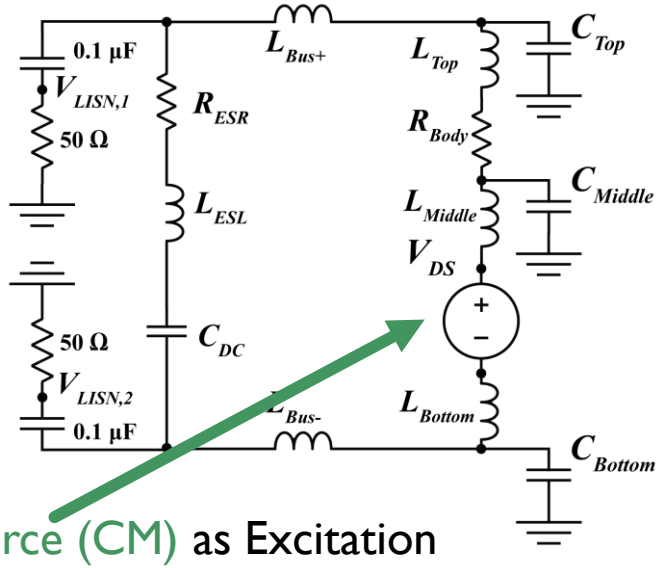


$$V_{DM} = \frac{V_{LISN,1} - V_{LISN,2}}{2} \qquad V_{CM} = \frac{V_{LISN,1} + V_{LISN,2}}{2}$$

DM Equivalent Circuit



CM Equivalent Circuit



FD Current Source (DM) and Voltage Source (CM) as Excitation

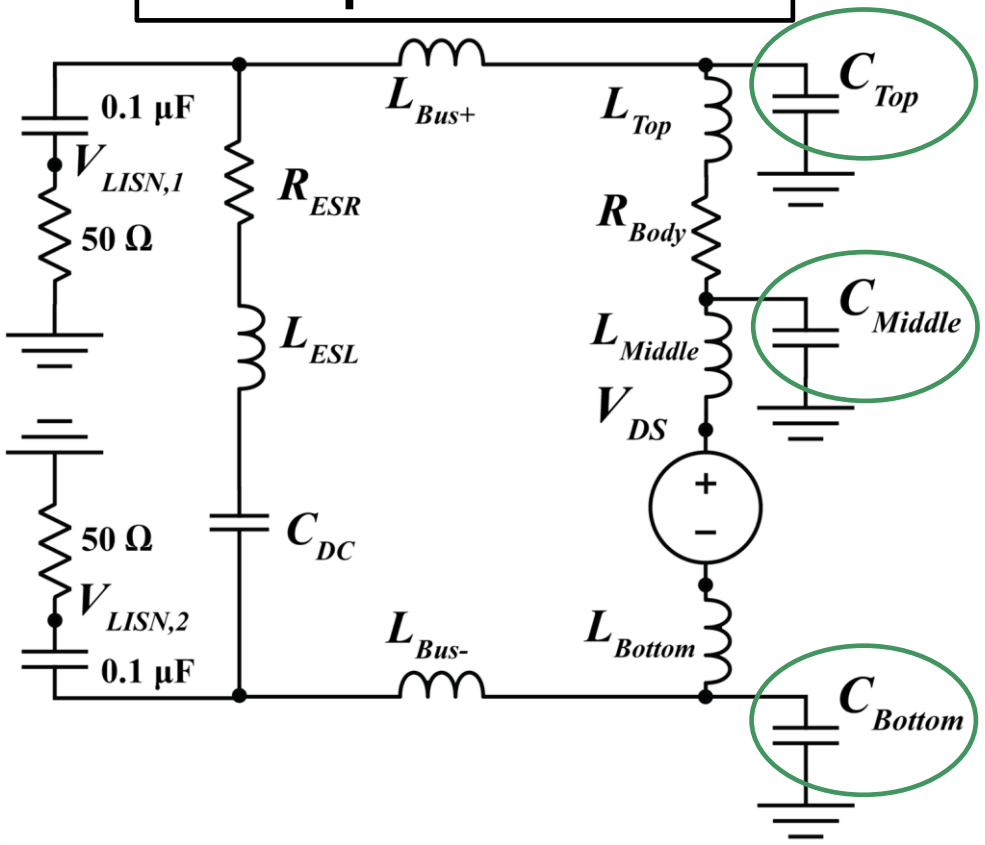
DM: **TOTAL** Loop Inductance & C_{oss} Resonance
CM: Trace Capacitance to Ground

Q. Liu, *Modular Approach for Characterizing and Modeling Conducted EMI Emissions in Power Converters*, Doctoral Dissertation, Virginia Tech, 2005.

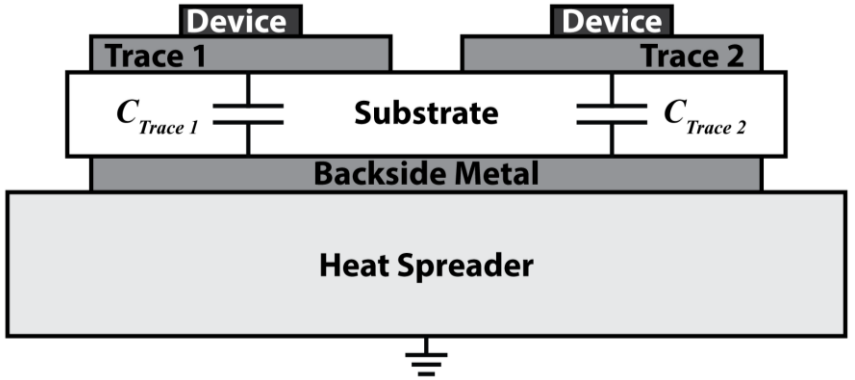
COMMON MODE MODELING

- L, R parasitics extracted using PowerSynth response surface model (RSM)
- Parasitic capacitances calculated based on trace area and separation from ground
- CM voltage gain transfer function employed in calculating CM noise

CM Equivalent Circuit



Module Trace Capacitance



Trace Capacitance:

$$C = \frac{\epsilon A}{d}$$

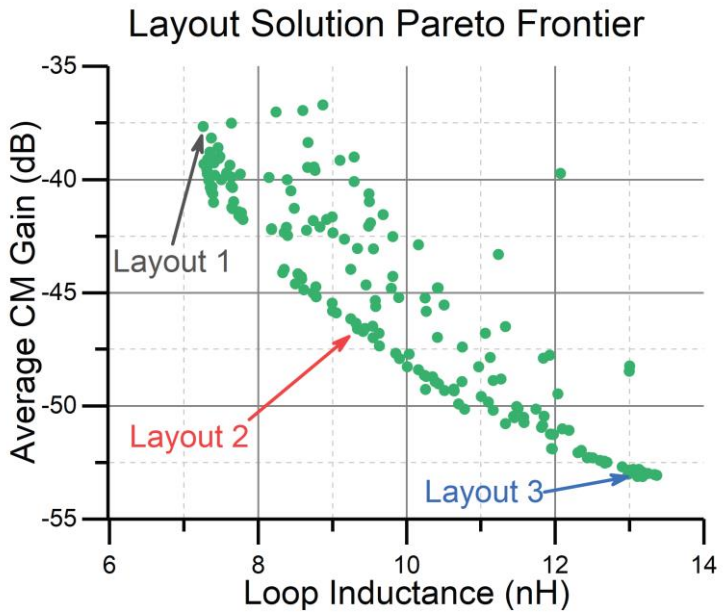
Common Mode Voltage:

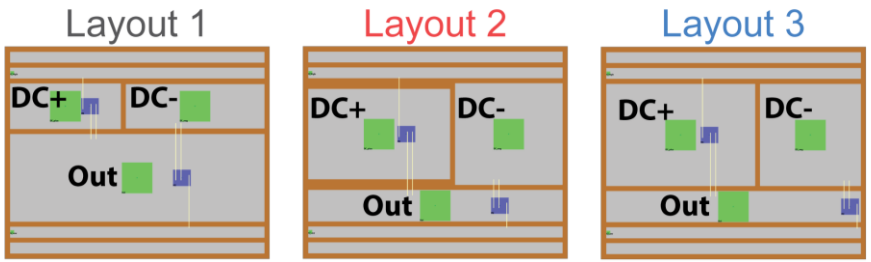
$$V_{CM} = V_{DS} G_{CM}$$

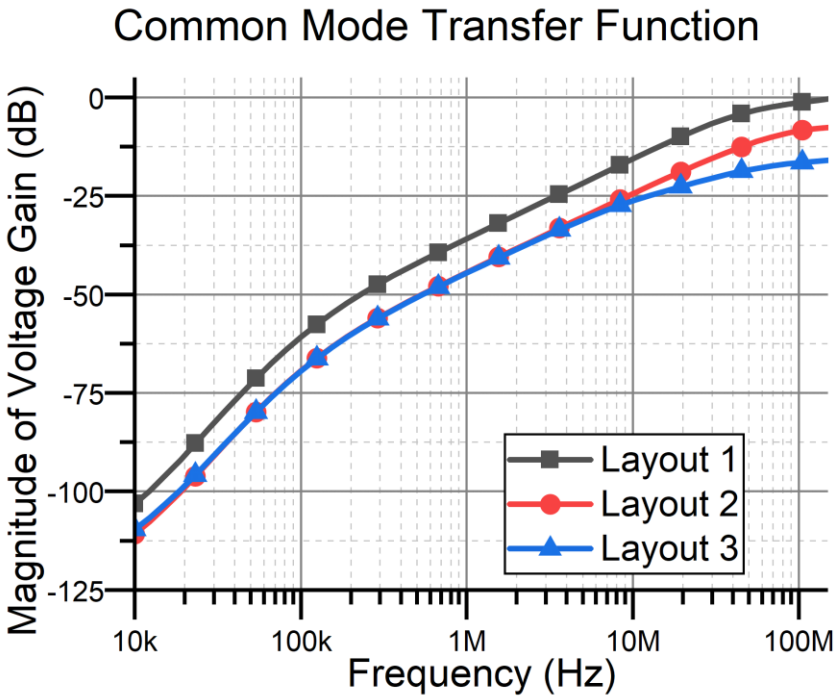
CONDUCTED EMI TEST CASE AND SIMULATION

POWERSYNTH LAYOUT OPTIMIZATION

- Loop inductance (layout only) used as surrogate for DM noise
- CM noise calculated using modified nodal analysis (MNA) on HF equivalent circuit
  - Frequencies sampled geometrically between 10 kHz and 100 MHz
  - Average of CM voltage gain transfer function used in cost function
- 2201 layouts evaluated in 3675 s (228 shown)







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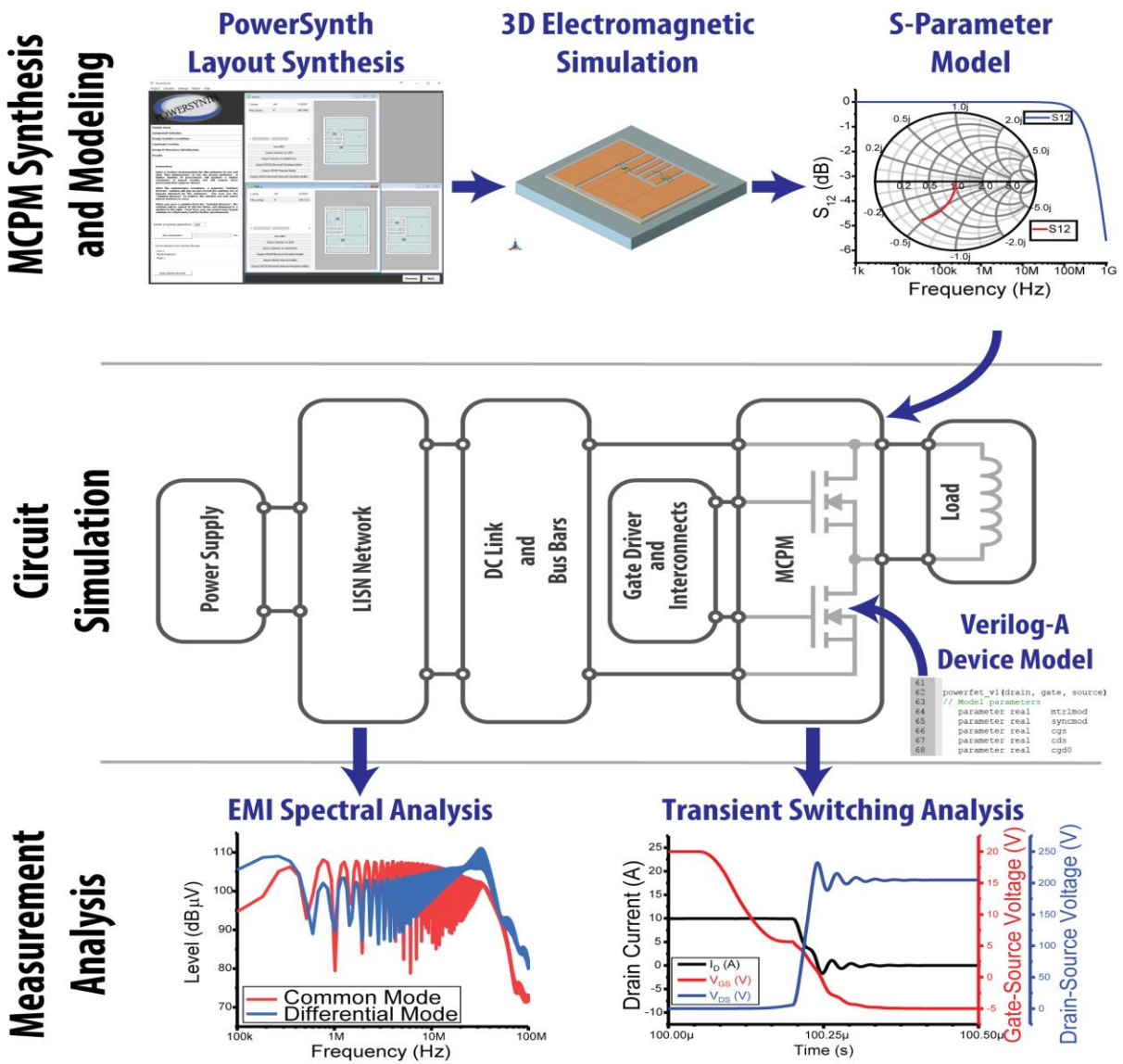
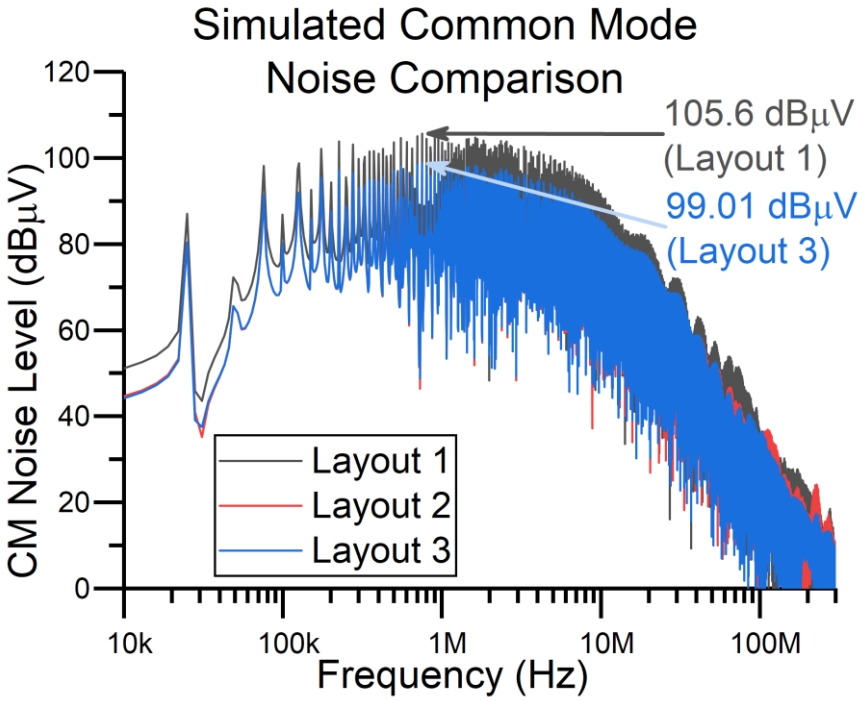
SIMULATED EMI TEST BENCH

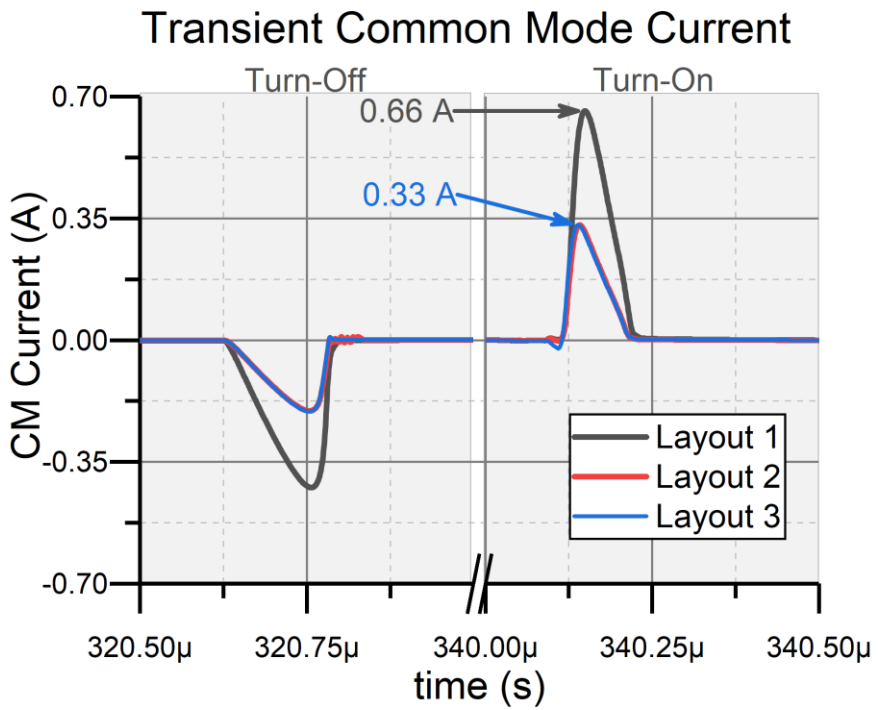
- Automated export of PowerSynth design solutions to commercial FEA EM solver
- 3D EM simulation results exported as S-parameter model for circuit simulation
- Circuit simulation includes total system including detailed device models
- Transient simulations with FFT analysis of results possible

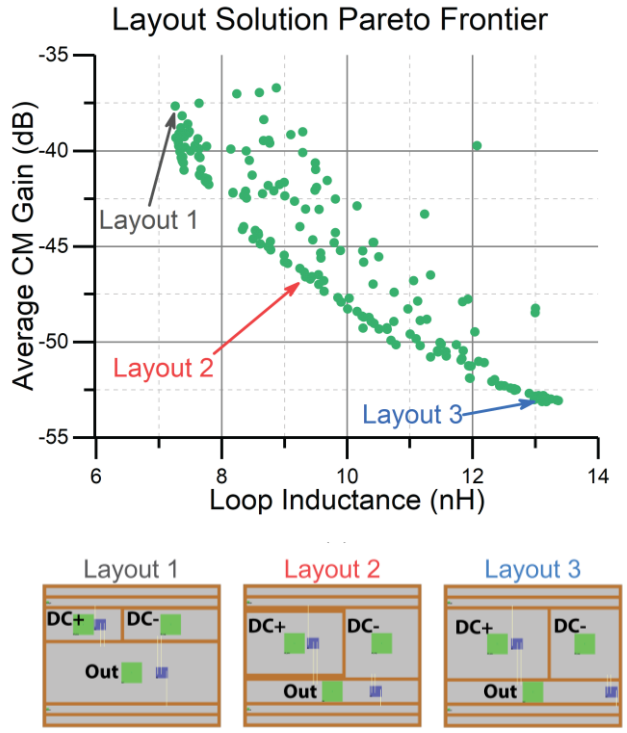
Circuit Setup Used:
- Half bridge power module, double pulse test
- Single SiC device / switch pos.
- 10 A, 600 V DC Bus
- 25 kHz switching, 50% duty cycle



CM RESULTS COMPARISON



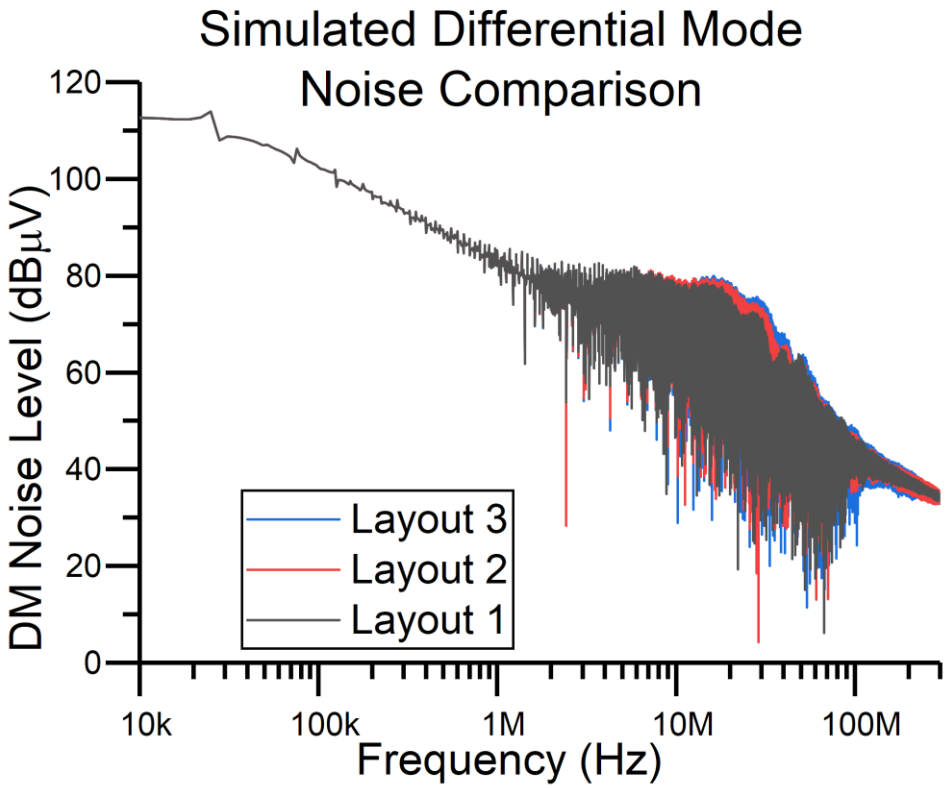


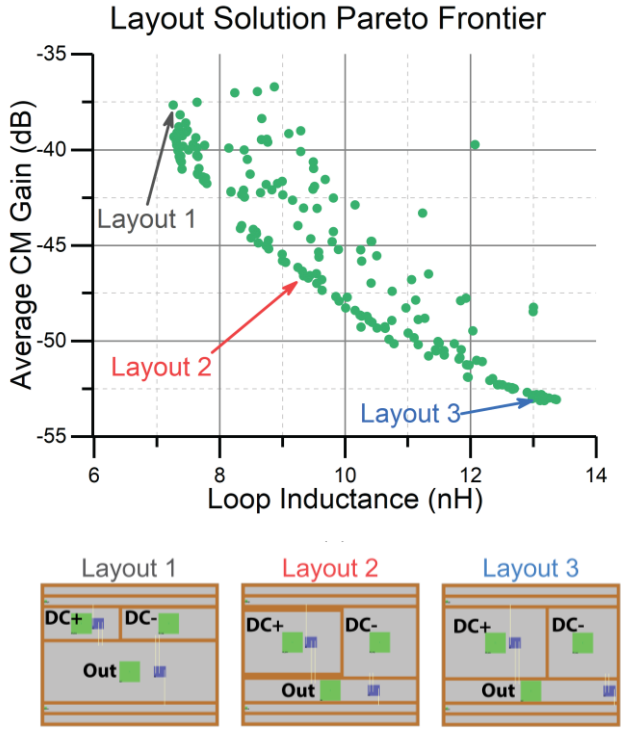


PowerSynth correctly identifies trend in CM noise genereation

DM RESULTS COMPARISON

DM results not as profound, but PowerSynth prediction still follows simulated trends





CONCLUSIONS

- EDA techniques for power electronic modules show promise for reducing design iterations
- Moving toward performance-based optimization instead of simply pure analytics (EMI reduction instead of blind parasitics reduction)
- Moving forward:
  - Optimize for signal integrity in gate loop toward preventing false turn on and improving current sharing
  - Explore layout impacts on radiated EMI
  - Test and validate with physical measurements