PEEC Method and Hierarchical Approach Towards 3D Multichip Power Module (MCPM) Layout Optimization

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- Conclusion and future work
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The power module design flow is computationally and labor intensive.
What Do We Need?

“Imagine we design a circuit without a circuit simulator…
How about designing module layout?”

We need:

• A more efficient design flow.
• Fast and accurate models for electro-thermal assessment.
• An Electronic Design Automation tool for Power Module design

This would enhance the productivity of the whole design process
PowerSynth Overview

- Fast and accurate models
  - Electrical parasitics
  - Fast 2D thermal model
- Design automation through multi-objective optimization
- Quickly explore trade-offs in solution space
- Export to commercial solvers for further analysis

PowerSynth Design Flow and Strategy

- Fast layout generation to explore the design spaces of integrated power modules
- Fast thermal and electrical analysis to gauge power module performance quickly
- Multi-objective optimization accounts for many trade-off design solutions.
- Easily export layout solution to FEA tools for post-analysis
- PowerSynth Journal Article [1]

Parasitics Extraction in PowerSynth

Initial Approach

- **The Laplacian Matrix Method:**
  - Linear approximation of loop Inductance and Resistance values.
  - Fast evaluation and accurate extraction for most 2D layouts
  - Response surface for accurate extraction

- **Limitations:**
  - Does not consider mutual inductance between nets.
  - No branch current and node voltage information
Limitations of the Prior Approach

The Laplacian matrix can yield good approximation however it fails to compare and contrast between layout cases with these characteristics.

<table>
<thead>
<tr>
<th>Case</th>
<th>Old Model</th>
<th>Expected Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>L1 greater than L2</td>
<td>L1 less than L2</td>
</tr>
<tr>
<td>2</td>
<td>L1 equal L2</td>
<td>L1 greater than L2</td>
</tr>
</tbody>
</table>
Mutual Inductance Impact Case Study

- Analyze gate signal integrity with and without mutual inductance impact.
- False turn-on voltage in the gate-source signals has been observed in the two cases.
- More mutual impact with 3D layout cases.
  → Crucial to layout automation design.
  → We can consider most of these issues using PEEC techniques.
The Partial Element Equivalent Circuit (PEEC) is a parasitics extraction technique using element stamping and matrix solving.

\[(G + sC)\): the conductance and capacitance matrix
\[A\]: adjacency matrix
\[I_i\]: input current sources
\[V_i\]: input voltage sources

\[
\begin{bmatrix}
  G + sC & A \\
  A^T & -(R + sL)
\end{bmatrix}
\begin{bmatrix}
  \Phi \\
  I
\end{bmatrix}
=
\begin{bmatrix}
  I_i \\
  V_i
\end{bmatrix}
\]
Solution types:

No Current Solution:
\[
[(G + sC) + A(R + sL)A^T]\Phi = I_i + A(R + sL)^{-1}V_i
\]

No Voltage Solution:
\[
[(R + sL) + A^T(G + sC)^{-1}A]I = -V_i + A^T(G + sC)^{-1}I_i
\]

Advantage:
- Can switch between above matrices formations to optimize evaluation time
- Current solution can be used to evaluate electric field and current density inside conductor
- Voltage solution can be used to evaluate electric field between different conductor

Disadvantage:
- Increased in computation time due to problem size in MCPM versus the skin-depth
Meshing Process

**Coarse meshing:**
- Input
- Simple Split
- Coarse Mesh

**Mesh for parasitic capacitance:**
- Top view
- Side view
  - Overlapped region
  - Isolation

**Edges and nodes assignment for R, L evaluation:**
- Node Tracking
- Edge Formation
- Assign Edge Dimension

“**A coarse mesh is used in this paper for branch current and node voltage evaluation with less computational effort**”
RLCM Elements Evaluation

Pre-computed model through response surface technique [*]. These models take input width (W), length (L) of traces and frequency (f).

RLCM Elements Evaluation

Exact analytical equation for mutual inductance calculation is used.

Take into account widths, lengths and distances between rectangular bars

Hierarchical Representation

Hierarchical representation:
• Symmetrical designs on same substrate.
• Reduces evaluation time.
• Meshing operation is independent for each group.

Components and terminals connections:
• Connections for devices and terminals in each different trace group are represented by a hierarchical tree structure.
• A subgraph is used to represent components internal parasitics (if they exist).
Current Density Extraction Results

Simple 10 mm x 10 mm U-shaped structure

Evaluation time comparison

<table>
<thead>
<tr>
<th>Method</th>
<th>Evaluation Time</th>
<th>#Mesh</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model</td>
<td>30 ms</td>
<td>120</td>
</tr>
<tr>
<td>HFSS</td>
<td>180 s</td>
<td>1371</td>
</tr>
</tbody>
</table>

- Current density results are extracted using model and compared with Ansys HFSS.
- Good agreement versus HFSS simulation
Experimental Setup for Coupling Verification

- Netlist is extracted using model for each selected frequency from 10 kHz – 1 GHz
- Synopsys Hspice was used to extract the s-parameter from the netlist
- Same layout is simulated in ANSYS HFSS for validation

Test case 2
Experimental Results for Coupling Verification

- Measurement results show some noise in the frequency range less than 100 kHz.
  - Lower dynamic range at intermediate frequency of 3 kHz
  - Contact resistance between solder and SMA connector
- Results fit very well in the high-frequency region (>100 kHz).
Current Density Extraction @ 1MHz

Good current density agreement with HFSS

Test Structure

Model

HFSS

50 Ohm termination

DUT

Overview
Motivation
Methodology
Results
Conclusion
Experimental Result for Loop Verification

Layout and Mesh Structure

Parasitics Extraction and Measurement Comparison

Test case 3

## Extraction Time Comparison

<table>
<thead>
<tr>
<th></th>
<th>FastHenry</th>
<th>Previous Model [1]</th>
<th>Model without M</th>
<th>Model with M</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Extraction Time</strong></td>
<td>~300 s</td>
<td>~50 ms</td>
<td>~180 ms</td>
<td>~1.5 s</td>
</tr>
<tr>
<td><strong>Speed-up Factor</strong></td>
<td>1</td>
<td>x6000</td>
<td>x1666</td>
<td>x200</td>
</tr>
<tr>
<td><strong>Mutual Inductance</strong></td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>I/V Distribution</strong></td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>
Conclusion and Future Work

- Accurate model considering mutual coupling and I,V information during optimization.
- Validation through S-parameter measurement.

- Validation for 3D layout.
- Combine with layout engine and optimization engine for layout optimization.
- EMI mitigation model


Acknowledgement
Thank you for your attention!

Merci de votre attention!