PEEC Method and Hierarchical Approach Towards 3D Multichip Power Module (MCPM) Layout Optimization

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Outline

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- PowerSynth Introduction

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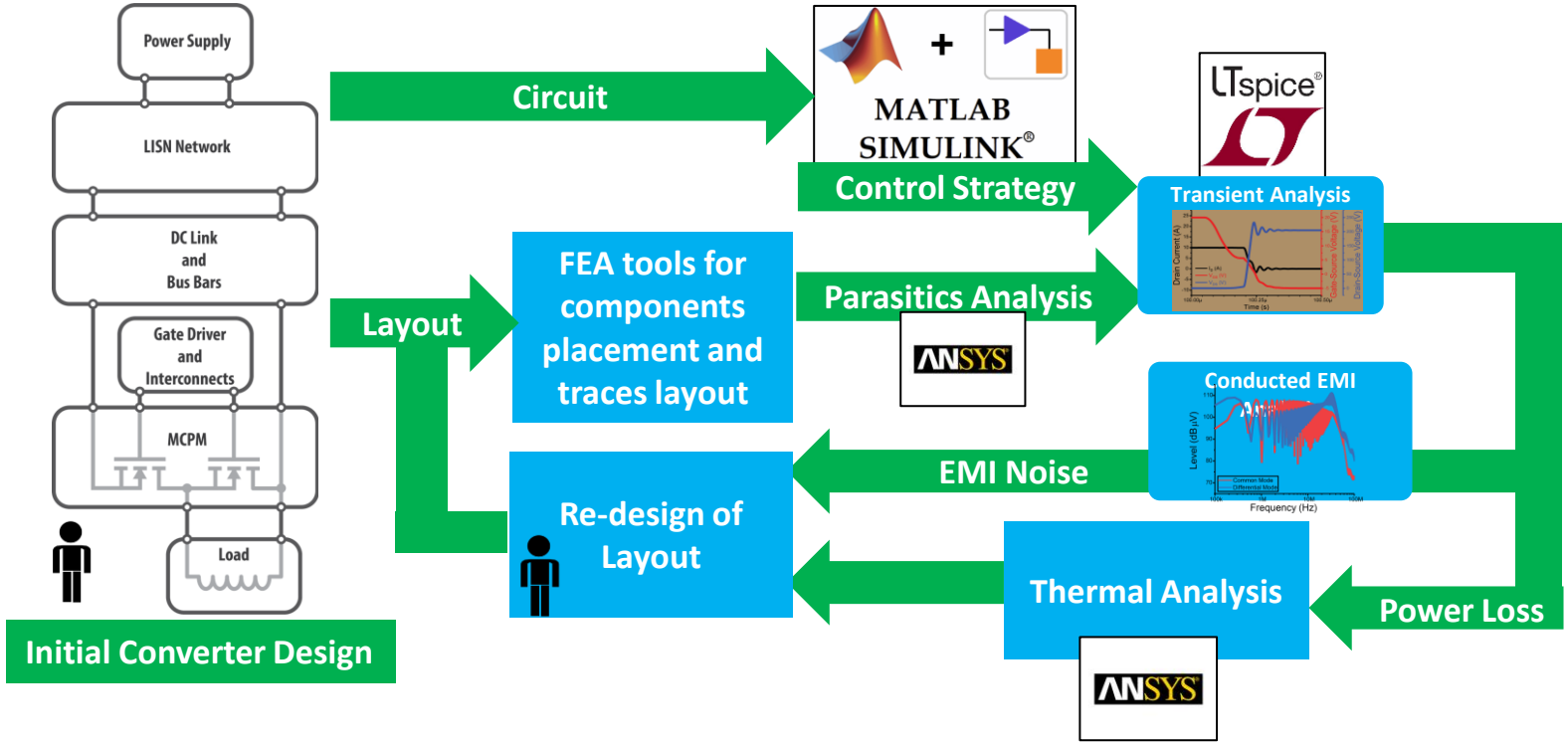
- S-parameter extraction for coupling validation
- Loop R, L validation
- Comparisons between models

V. Conclusion and future work

- Conclusion and future work
- Acknowledgement

Traditional Module Design Flow



The power module design flow is computationally and labor intensive

A. Bindra and A. Mantooth, "Modern Tool Limitations in Design Automation: Advancing Automation in Design Tools is Gathering Momentum," in *IEEE Power Electronics Magazine*, vol. 6, no. 1, pp. 28-33, March 2019.

What Do We Need?

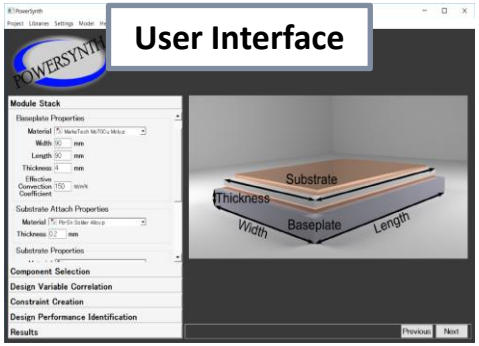
"Imagine we design a circuit without a circuit simulator…
How about designing module layout?"

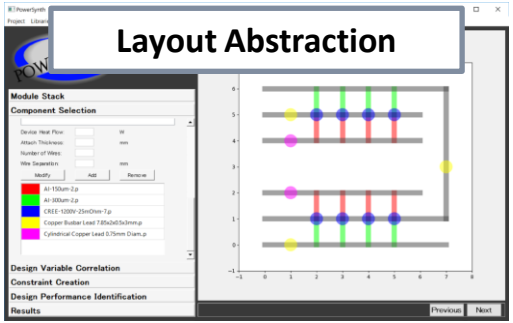
We need:

- A more efficient design flow.
- Fast and accurate models for electro-thermal assessment.
- An **E**lectronic **D**esign **A**utomation tool for Power Module design

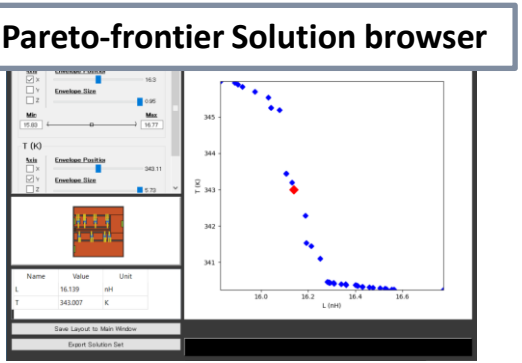
This would enhance the productivity of the whole design process

PowerSynth Overview





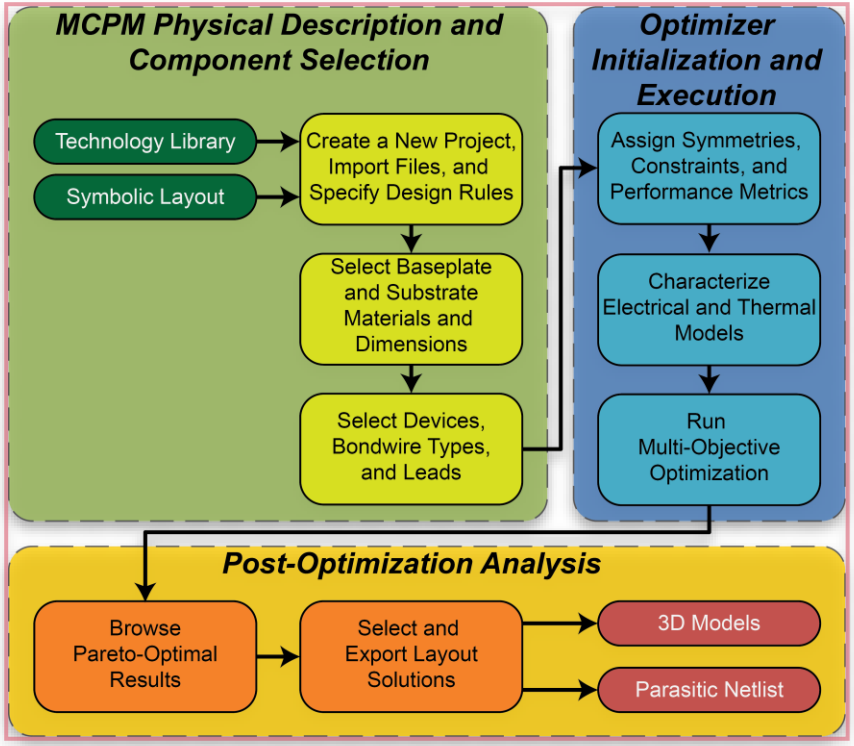
- **Fast and accurate models**
  - Electrical parasitics
  - Fast 2D thermal model
- **Design automation through multi-objective optimization**
- **Quickly explore trade-offs in solution space**
- **Export to commercial solvers for further analysis**



3D Model Export

T. M. Evans *et al.*, "PowerSynth: A Power Module Layout Generation Tool," in *IEEE Transactions on Power Electronics*.

PowerSynth Design Flow and Strategy



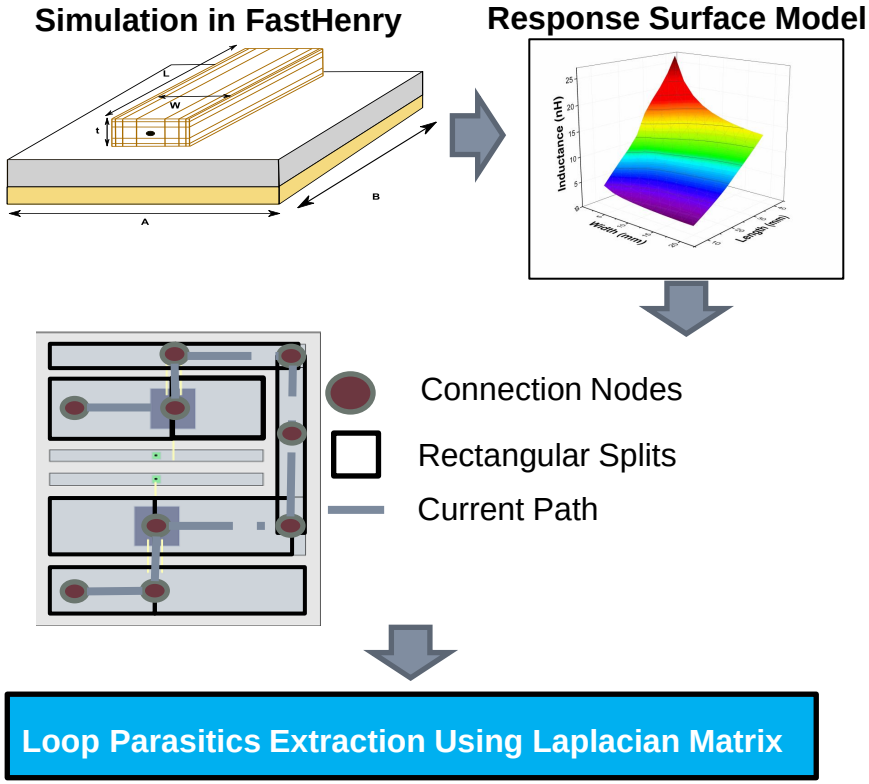
- Fast layout generation to explore the design spaces of integrated power modules
- Fast thermal and electrical analysis to gauge power module performance quickly
- Multi-objective optimization accounts for many trade-off design solutions.
- Easily export layout solution to FEA tools for post-analysis
- PowerSynth Journal Article [1]

[1] T. M. Evans *et al*., "PowerSynth: A Power Module Layout Generation Tool," in *IEEE Transactions on Power Electronics*.

Parasitics Extraction in PowerSynth

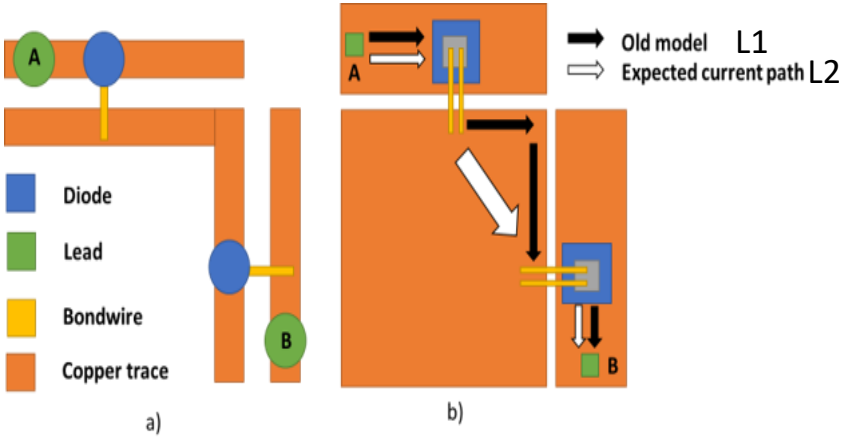
Initial Approach

- **The Laplacian Matrix Method:**
  - Linear approximation of loop Inductance and Resistance values.
  - Fast evaluation and accurate extraction for most 2D layouts
  - Response surface for accurate extraction
- **Limitations:**
  - Does not consider mutual inductance between nets.
  - No branch current and node voltage information

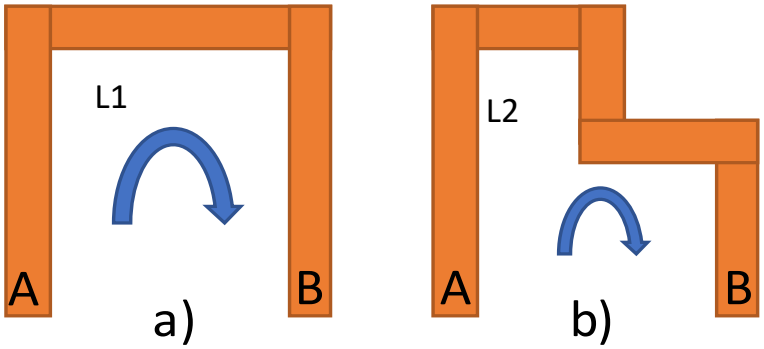


Limitations of the Prior Approach

Case 1



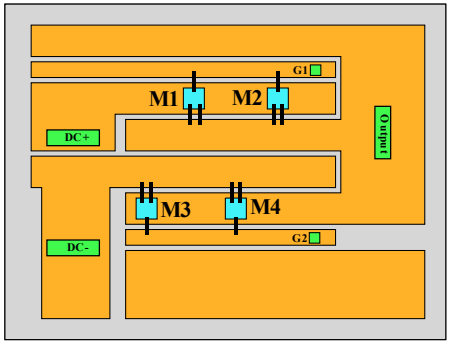
Case 2



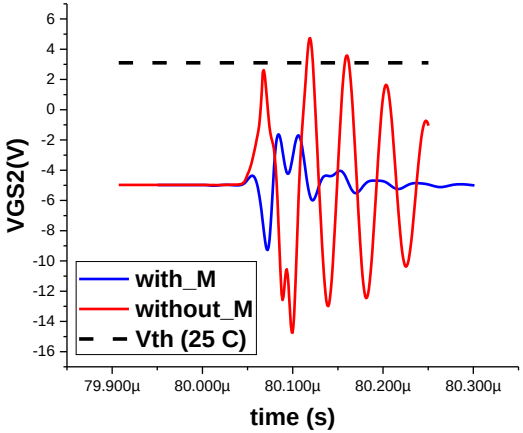
Case	Old Model	Expected Result
1	L1 greater than L2	L1 less than L2
2	L1 equal L2	L1 greater than L2

The Laplacian matrix can yield good approximation however it fails to compare and contrast between layout cases with these characteristics.

Mutual Inductance Impact Case Study



Double Pulse Test

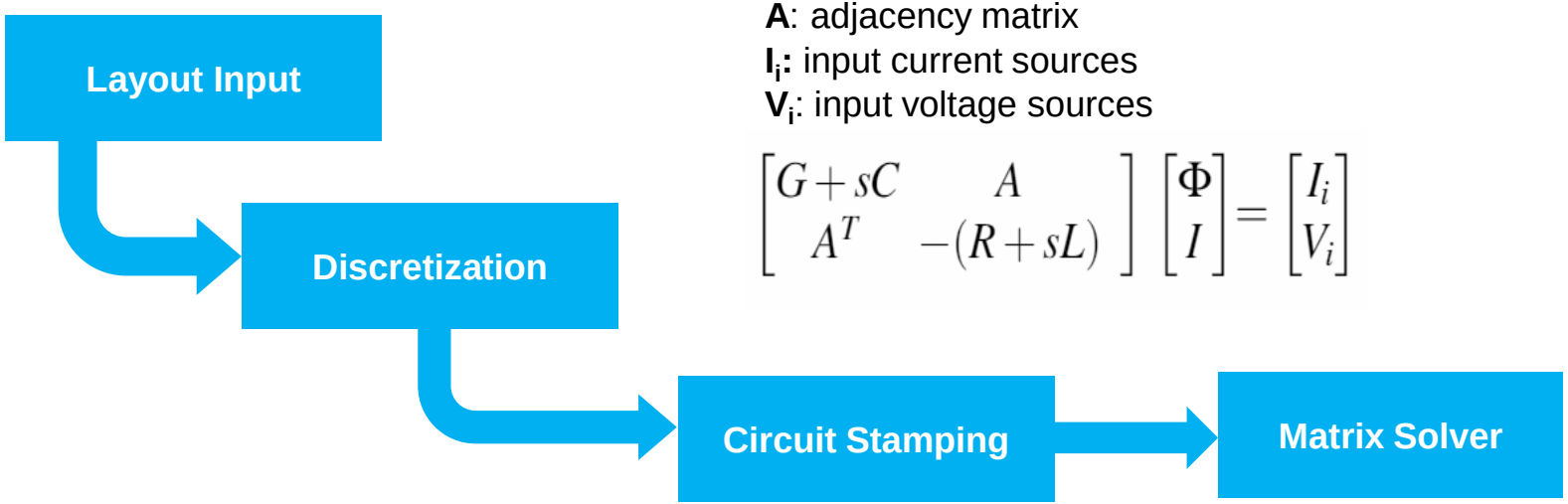


- Analyze gate signal integrity with and without mutual inductance impact.
- False turn-on voltage in the gate-source signals has been observed in the two cases
- More mutual impact with 3D layout cases

→ Crucial to layout automation design

→ We can consider most of these issues using PEEC techniques

PEEC Overview



(**G + sC**): the conductance and capacitance matrix
A: adjacency matrix
$\mathbf{I_i}$: input current sources
$\mathbf{V_i}$: input voltage sources

$$\begin{bmatrix} G+sC & A \\ A^T & -(R+sL) \end{bmatrix} \begin{bmatrix} \Phi \\ I \end{bmatrix} = \begin{bmatrix} I_i \\ V_i \end{bmatrix}$$

The **P**artial **E**lement **E**quivalent **C**ircuit (PEEC) is a parasitics extraction technique using element stamping and matrix solving.

A. Ruehli, G. Antonini, and L. Jiang, *Circuit Oriented Electromagnetic Modeling Using the PEEC Techniques*. John Wiley & Sons, 2017

PEEC Overview

Solution types:

No Current Solution:

$$[(\mathbf{G}+\mathrm{s}\mathbf{C})+\mathbf{A}(\mathbf{R}+\mathrm{s}\mathbf{L})\mathbf{A}^{\mathbf{T}}]\Phi=\mathbf{I_i}+\mathrm{A}(\mathbf{R}+\mathrm{s}\mathbf{L})^{-1}\mathbf{V_i}]$$

No Voltage Solution:

$$[(\mathbf{R}+\mathrm{s}\mathbf{L})+\mathbf{A}^{\mathrm{T}}(\mathbf{G}+\mathrm{s}\mathbf{C})^{-1}\mathbf{A}]\mathrm{I}=-\mathbf{V_i}+\mathbf{A}^{\mathbf{T}}(\mathbf{G}+\mathrm{s}\mathbf{C})^{-1}\mathbf{I_i}]$$

Advantage:

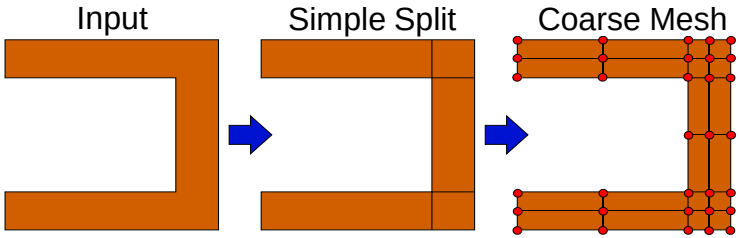
- Can switch between above matrices formations to optimize evaluation time
- Current solution can be used to evaluate electric field and current density inside conductor
- Voltage solution can be used to evaluate electric field between different conductor

Disadvantage:

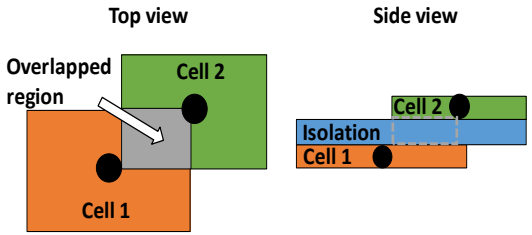
- Increased in computation time due to problem size in MCPM versus the skin-depth

Meshing Process

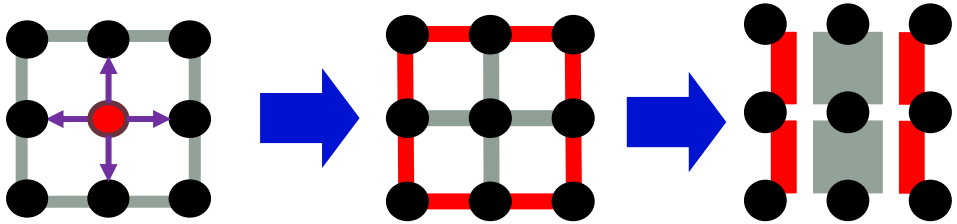
Coarse meshing:



Mesh for parasitic capacitance:



Edges and nodes assignment for R, L evaluation:



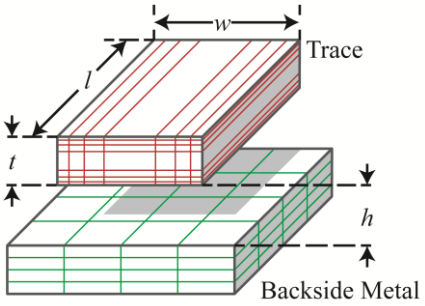
Node Tracking

Edge Formation

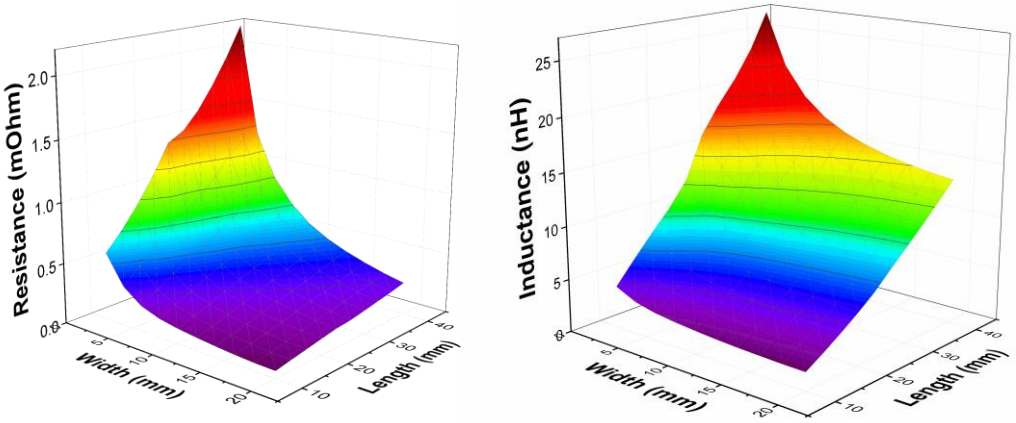
Assign Edge Dimension

"A coarse mesh is used in this paper for branch current and node voltage evaluation with less computational effort"

RLCM Elements Evaluation



Meshing structure for response surface

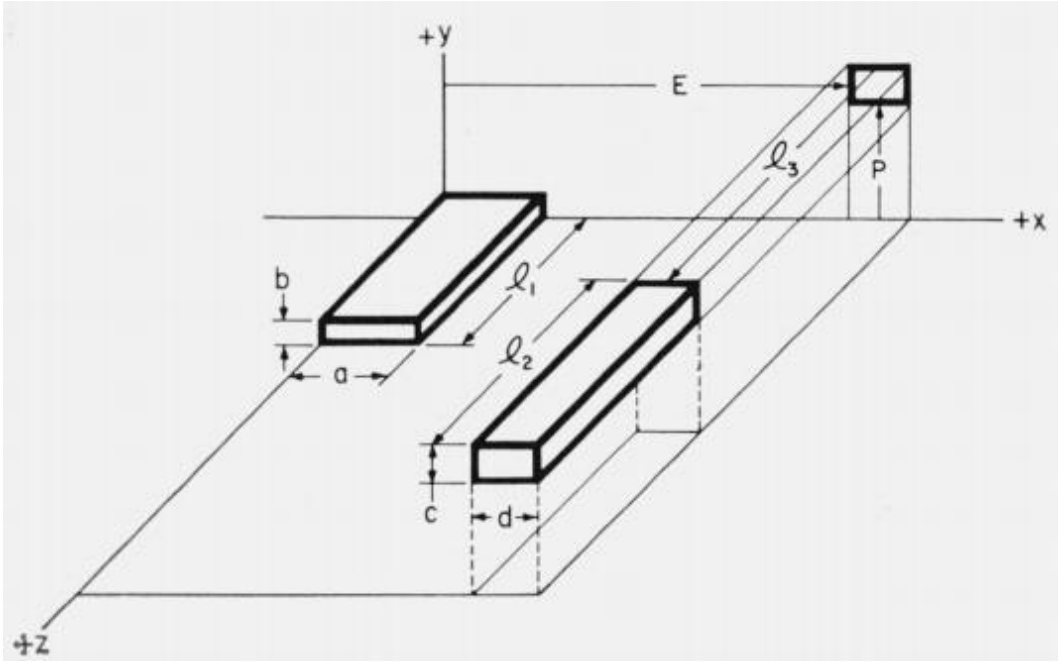


Trace resistance and inductance response surface

Pre-computed model through response surface technique [*]. These models take input width (W), length (L) of traces and frequency (f).

* Q. Le, T. Evans, S. Mukherjee, Y. Peng, T. Vrotsos and H. A. Mantooth, "Response surface modeling for parasitic extraction for multi-objective optimization of multi-chip power modules (MCPMs)," *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, 2017, pp. 327-334.

RLCM Elements Evaluation

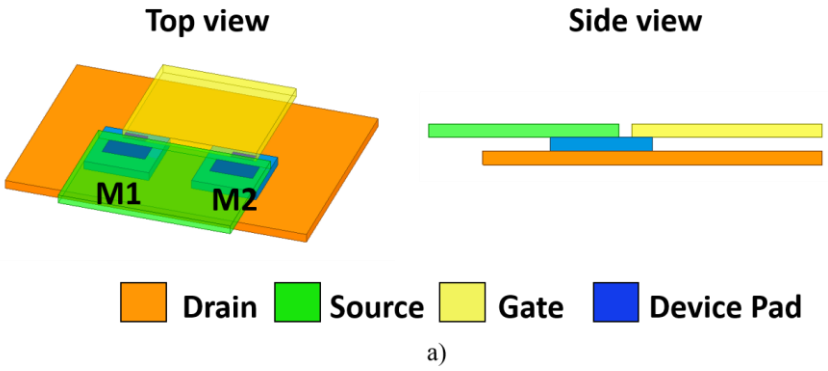


Exact analytical equation for mutual inductance calculation is used.

Take into account widths, lengths and distances between rectangular bars

C. Hoer and C. Love, "Exact Inductance Equations for Rectangular Conductors with Applications to more Complicated Geometries," *J. Res. Natl. Bur. Stand. Sect. C Eng. Instrum.*, vol. 69C, p. 127, 1965.

Hierarchical Representation



Hierarchical representation:

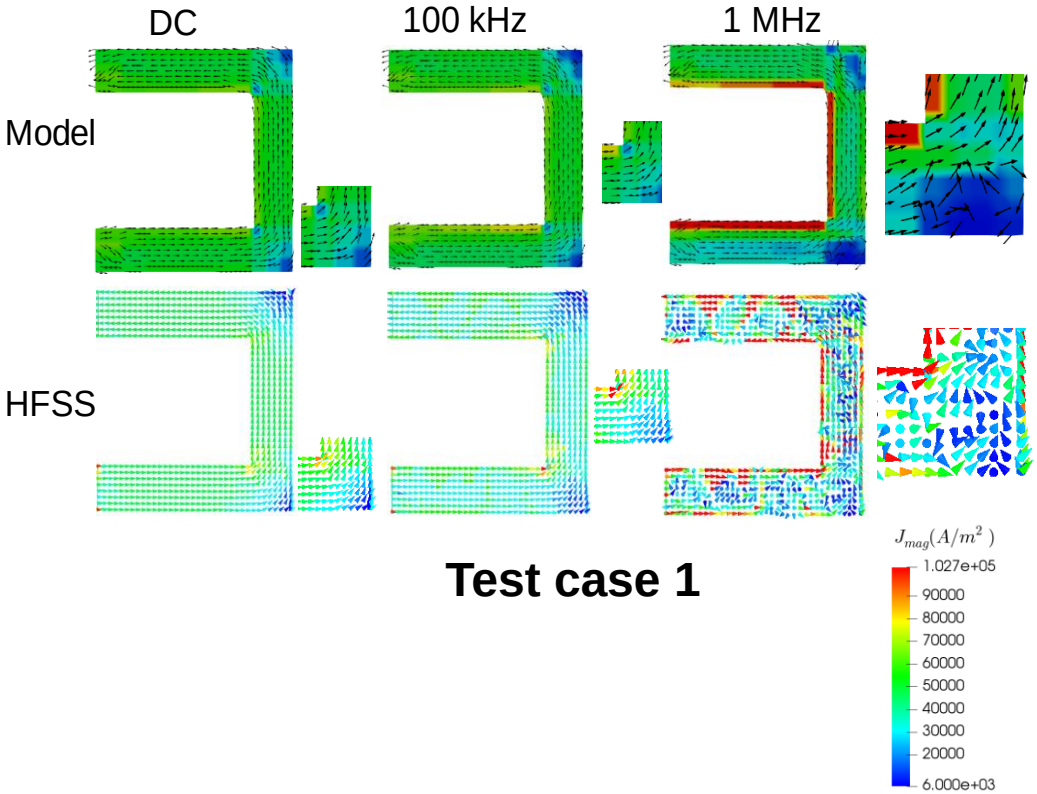
- Symmetrical designs on same substrate.
- Reduces evaluation time.
- Meshing operation is independent for each group.

Components and terminals connections:

- Connections for devices and terminals in each different trace group are represented by a hierarchical tree structure.
- A subgraph is used to represent components internal parasitics (if they exist).

Current Density Extraction Results

Simple 10 mm x 10 mm U-shaped structure



Test case 1

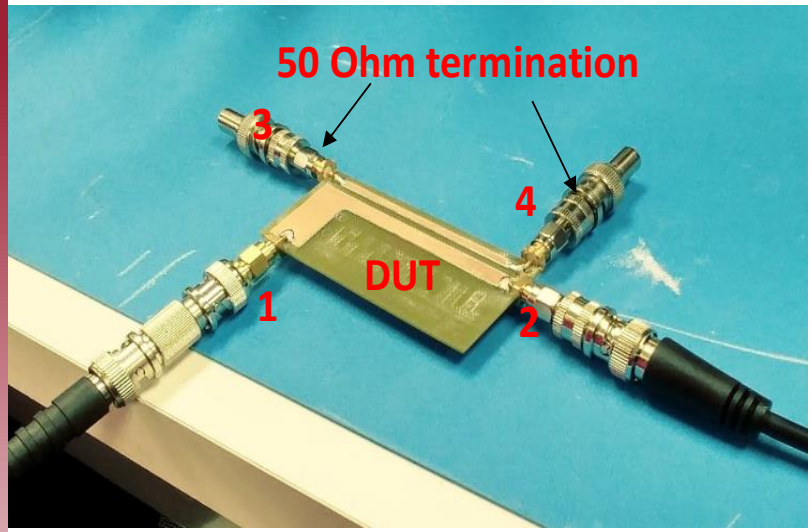
Evaluation time comparison

Method	Evaluation Time	#Mesh
Model	30 ms	120
HFSS	180 s	1371

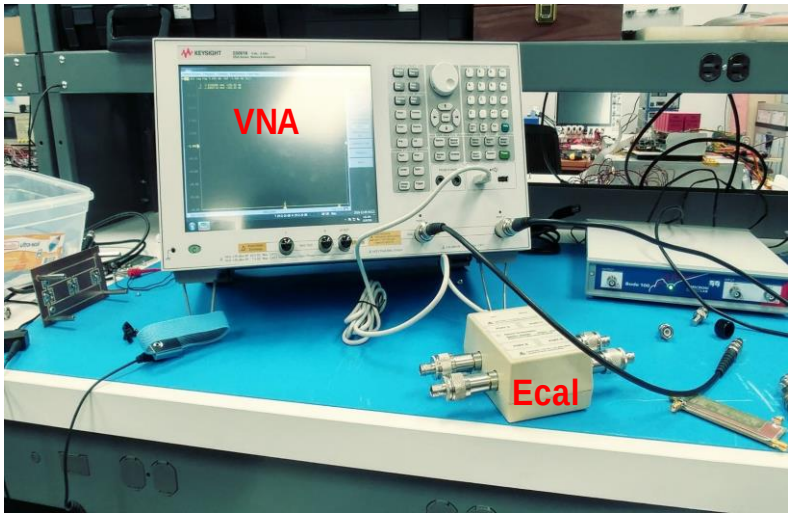
- Current density results are extracted using model and compared with Ansys HFSS.
- Good agreement versus HFSS simulation

Experimental Setup for Coupling Verification

4-port test board



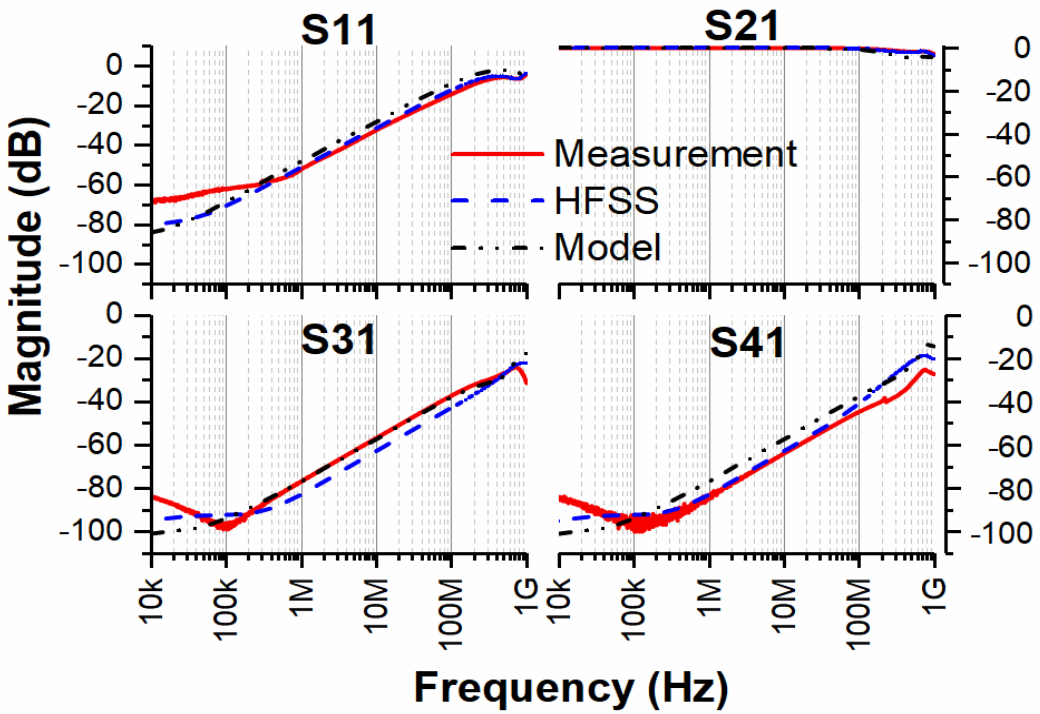
Experiment setup using Keysight E5061B VNA



- Netlist is extracted using model for each selected frequency from 10 kHz – 1 GHz
- Synopsys Hspice was used to extract the s-parameter from the netlist
- Same layout is simulated in ANSYS HFSS for validation

Test case 2

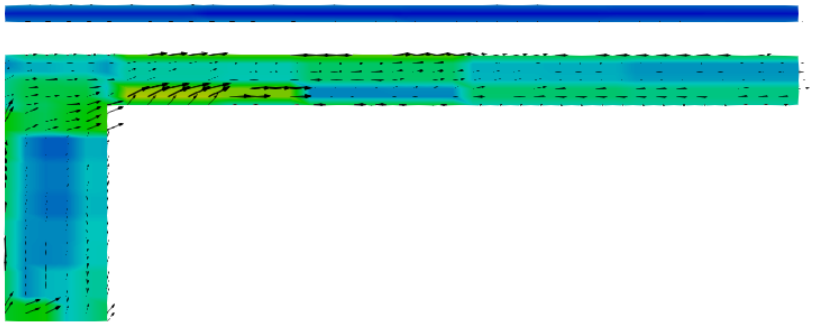
Experimental Results for Coupling Verification



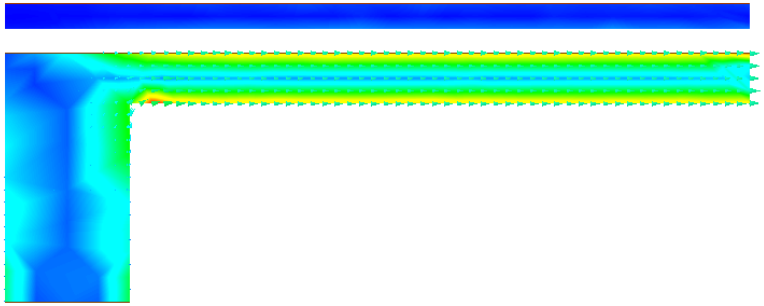
- Measurement results show some noise in the frequency range less than 100 kHz.
  - Lower dynamic range at intermediate frequency of 3 kHz
  - Contact resistance between solder and SMA connector
- Results fit very well in the high-frequency region (>100 kHz).

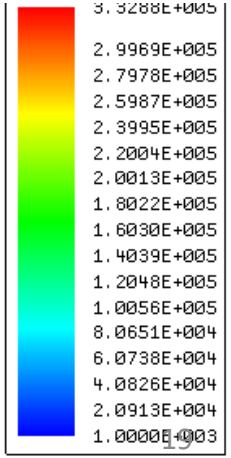
Current Density Extraction @ 1MHz

Model

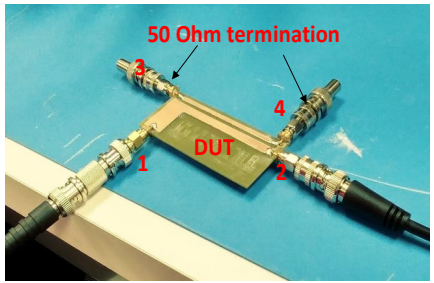


HFSS





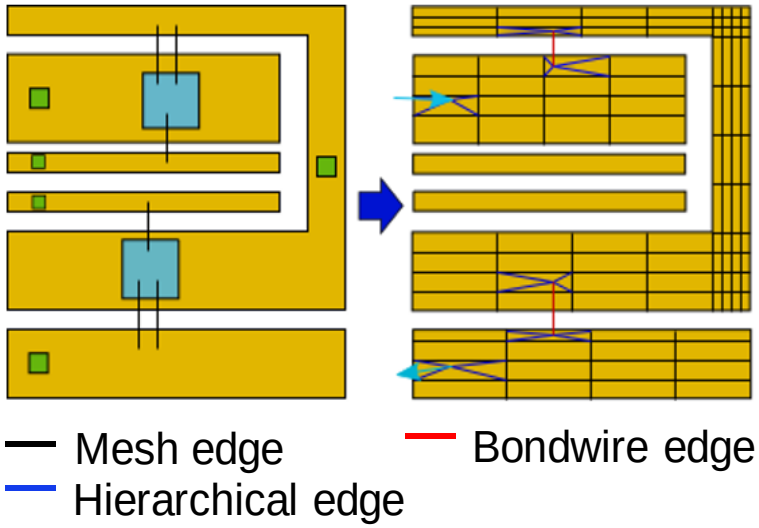
Test Structure



Good current density agreement with HFSS

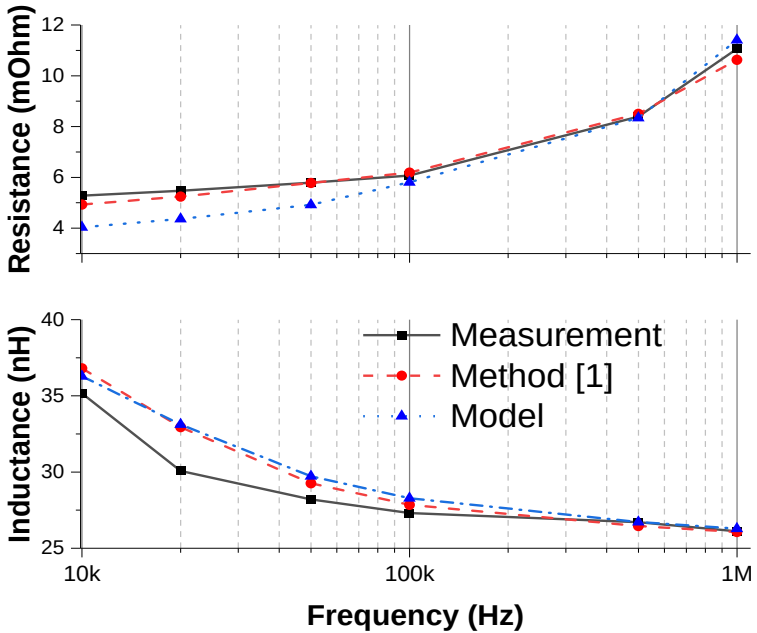
Experimental Result for Loop Verification

Layout and Mesh Structure



Test case 3

Parasitics Extraction and Measurement Comparison



[1] T. M. Evans *et al.*, "PowerSynth: A Power Module Layout Generation Tool," in *IEEE Transactions on Power Electronics*.

Extraction Time Comparison

	FastHenry	Previous Model [1]	Model without M	Model with M
Extraction Time	~300 s	~50 ms	~180 ms	~1.5 s
Speed-up Factor	1	x6000	x1666	x200
Mutual Inductance	Yes	No	No	Yes
I/V Distribution	No	No	Yes	Yes

Conclusion and Future Work

- Accurate model considering mutual coupling and I,V information during optimization.
- Validation through S-parameter measurement.

- Validation for 3D layout.
- Combine with layout engine and optimization engine for layout optimization.
- EMI mitigation model

References

[1] Bindra and A. Mantooth, "Modern Tool Limitations in Design Automation: Advancing Automation in Design Tools is Gathering Momentum," in *IEEE Power Electronics Magazine*, vol. 6, no. 1, pp. 28-33, March 2019.

[2] T. M. Evans *et al*., "PowerSynth: A Power Module Layout Generation Tool," in *IEEE Transactions on Power Electronics*.

[3] Q. Le, T. Evans, S. Mukherjee, Y. Peng, T. Vrotsos and H. A. Mantooth, "Response surface modeling for parasitic extraction for multi-objective optimization of multi-chip power modules (MCPMs)," *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, 2017, pp. 327-334.

[4] C. Hoer and C. Love, “Exact Inductance Equations for Rectangular Conductors with Applications to more Complicated Geometries,” *J. Res. Natl. Bur. Stand. Sect. C Eng. Instrum.*, vol. 69C, p. 127, 1965

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Acknowledgement

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Thank you for your attention !

Merci de votre attention!