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Hierarchical Layout Synthesis and Design Automation for 2.5D Heterogeneous Multi-Chip Power Modules

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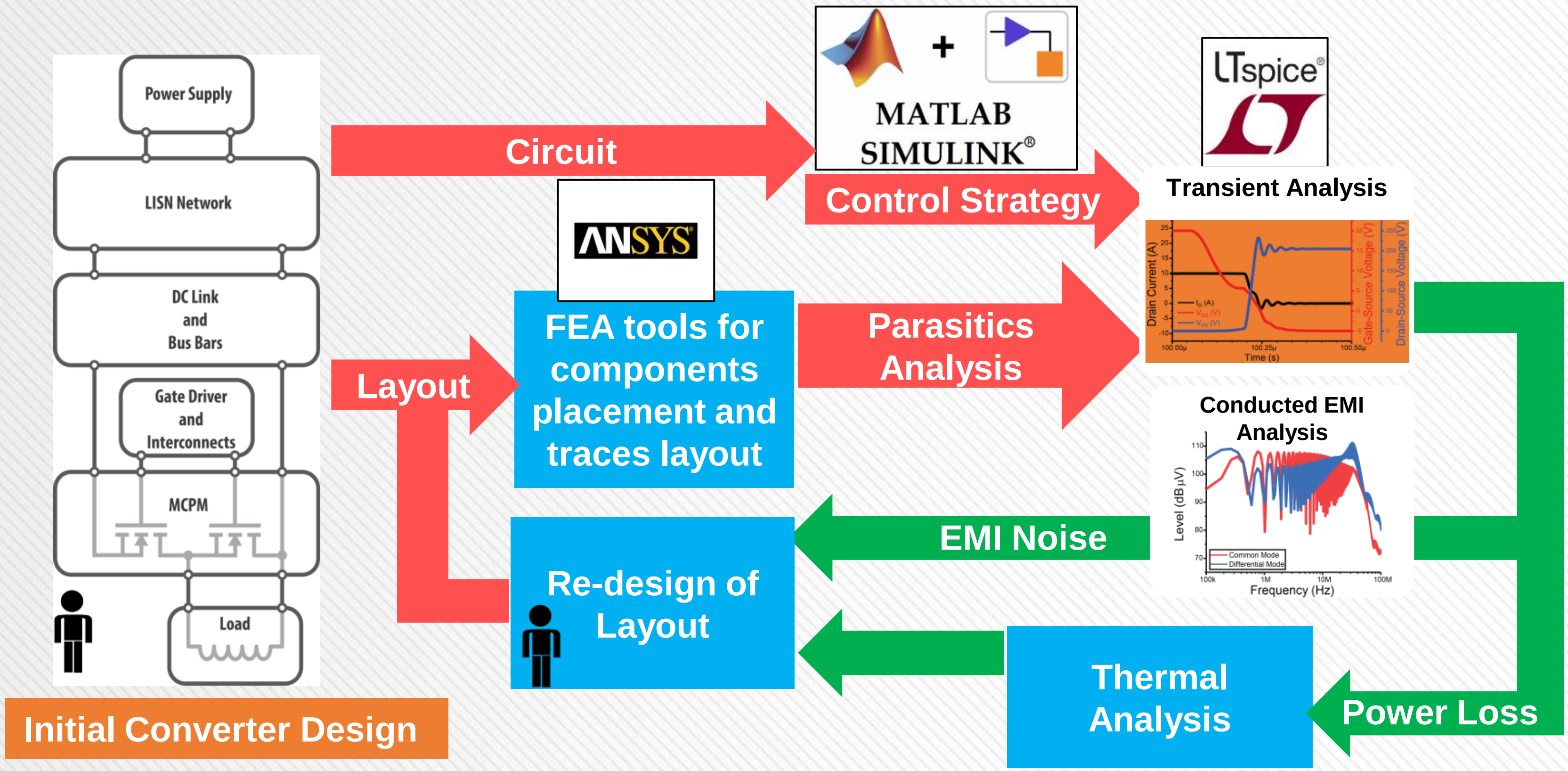
Outline

- **Overview**
  - Traditional design flow
  - PowerSynth (an EDA tool) Introduction
- **Motivation**
- **Methodology**
  - Hierarchical corner stitch and constraint graph
  - Layout generation and optimization algorithm
- **Results**
  - Benefits of hierarchical approach over non-hierarchal approach
- **Conclusions**
- **Future Work**

Traditional Design Flow

- **A Typical Power Electronics Design Flow:**
  - The design flow is both tedious and computationally expensive



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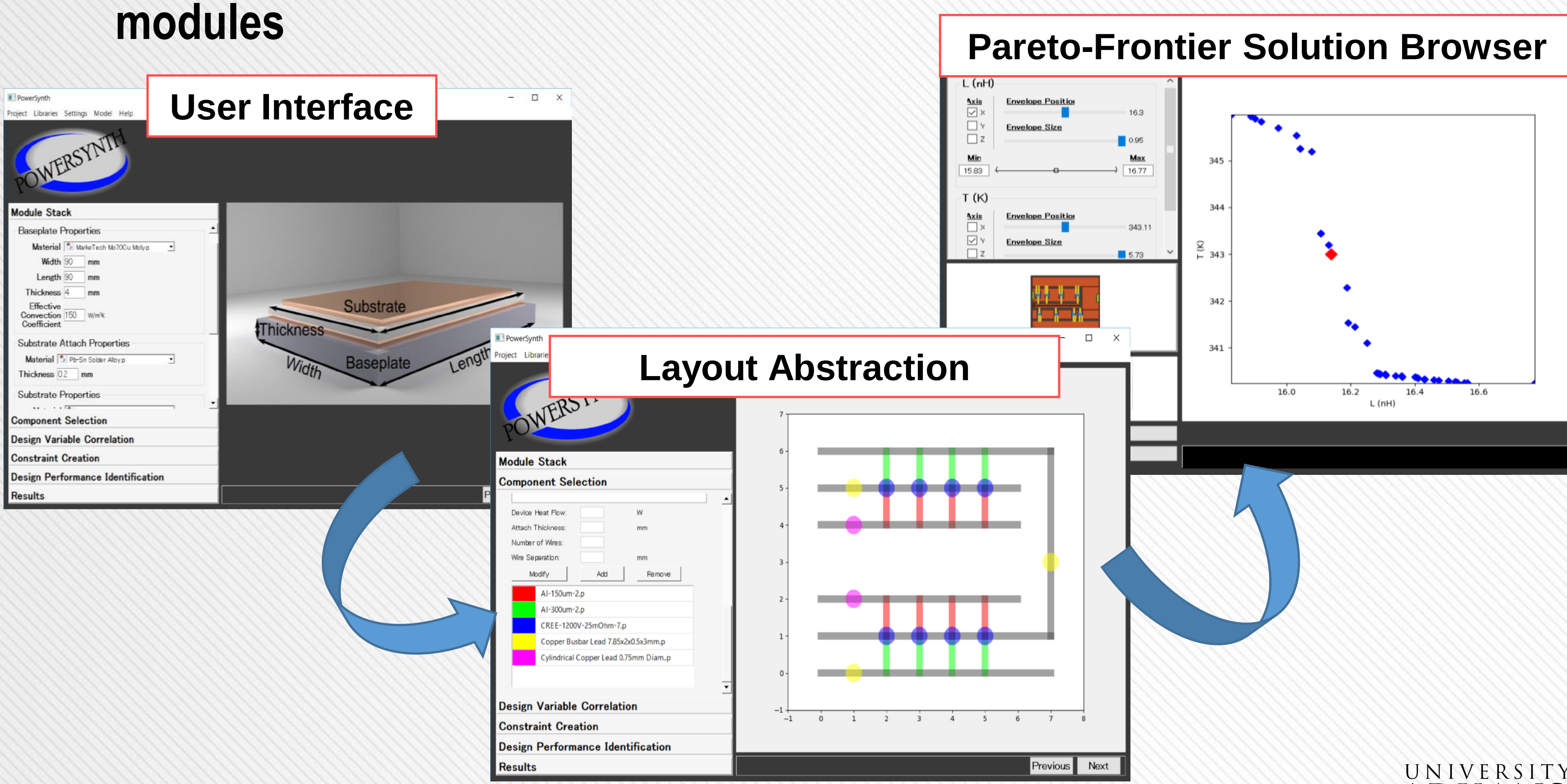
Layout Synthesis and Optimization

❑ PowerSynth

- A software tool for the design and layout of multi-chip integrated power modules



T. M. Evans *et al.*, "PowerSynth: A Power Module Layout Generation Tool," in *IEEE Transactions on Power Electronics*,*2019*.

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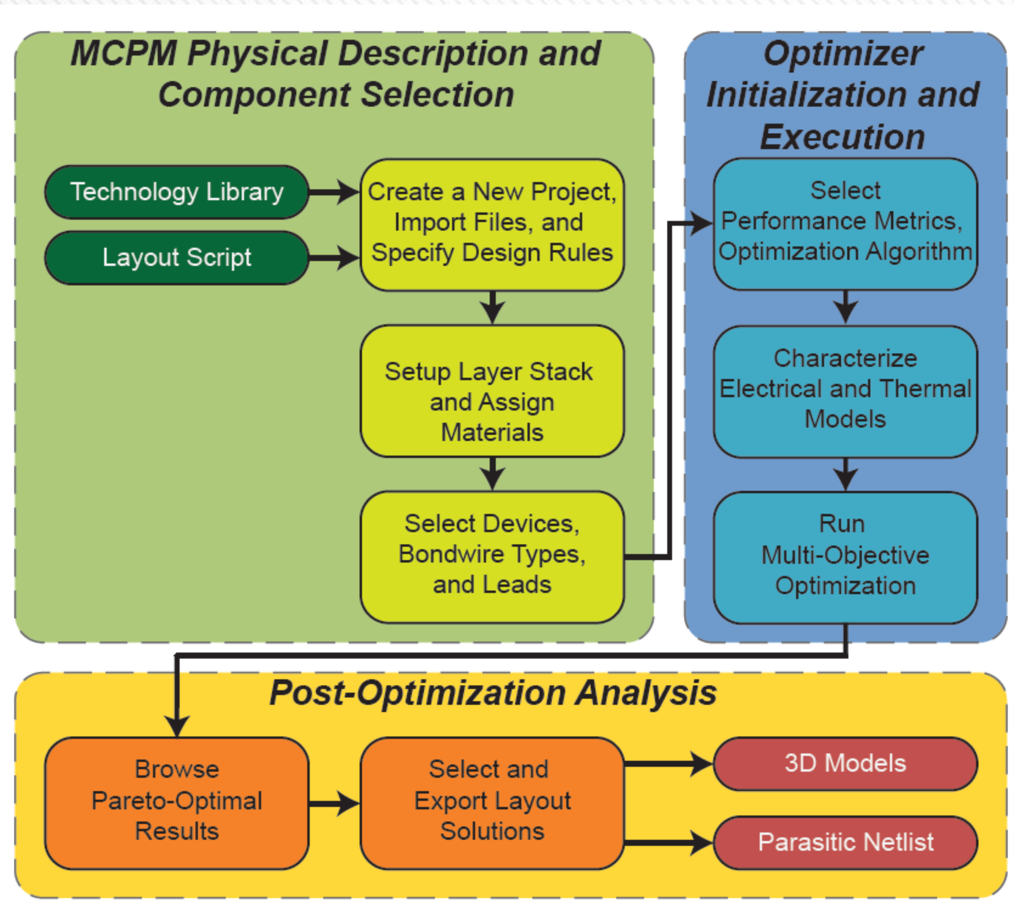
PowerSynth Overview

❑ PowerSynth Features:

- Constraint-aware layout engine to generate DRC-clean layouts
- Explore the design spaces of integrated power modules
- Uses fast thermal and electrical models to gauge power module performance quickly
- Multi-objective optimization allows for many trade-off design solutions to be considered
- Reliability considerations for thermal stress and partial discharge
- Easily export design solutions to FEA tools

PowerSynth Workflow



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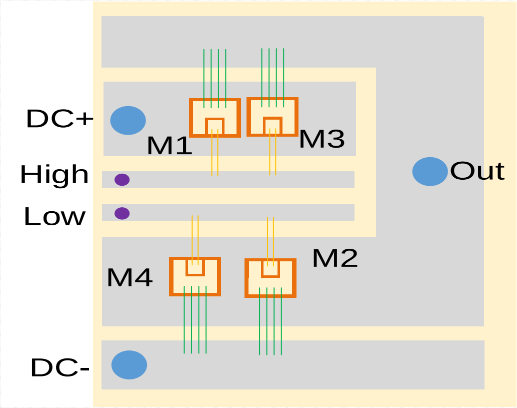
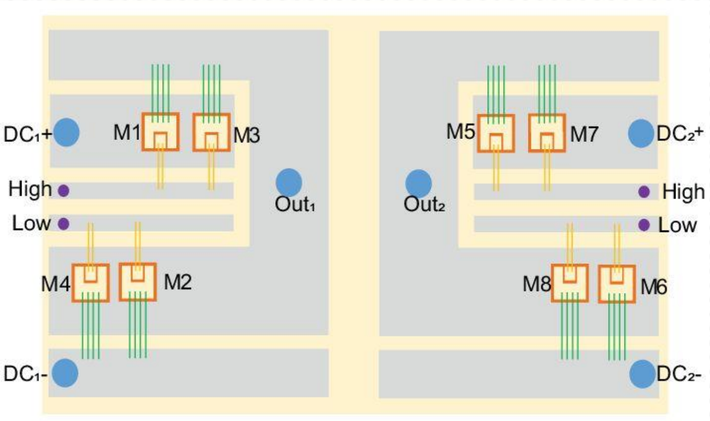
Motivation

- **Already demonstrated:**
  - 2D heterogeneous power module optimization capability.
- **To increase the power density :**
  - 2.5D and 3D heterogeneous power modules optimization are obvious.
- **2.5D power module layout generation and optimization algorithms are developed as a continuing work.**
  - Two symmetrical half-bridge power modules on the same substrate.



Half-bridge power module



Full-bridge power module

I. Al Razi et al, "Constraint-Aware Algorithms for Heterogeneous Power Module Layout Synthesis and Reliability Optimization, in WIPDA, pp. 323–330, Oct 2018

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Methodology

❑ Strategies:

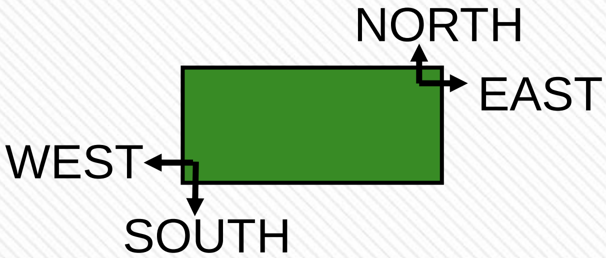
- Re-use optimization results to reduce computational effort (2.5D power module layout optimization)
- Reduce coordinate correlation among components
- Handle fixed dimension components in a generic way

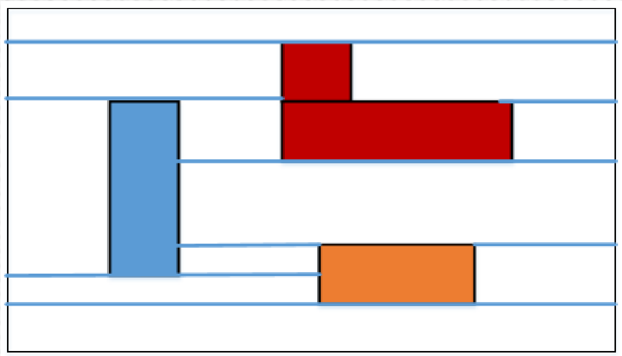
❑ Methodologies:

- Hierarchical corner stitch data structure
  - Tree data structure of the corner-stitched planes
- Hierarchical constraint graph
  - Manipulation of constraints for solution generation
- Optimization algorithms
  - Tradeoff among multiple objectives

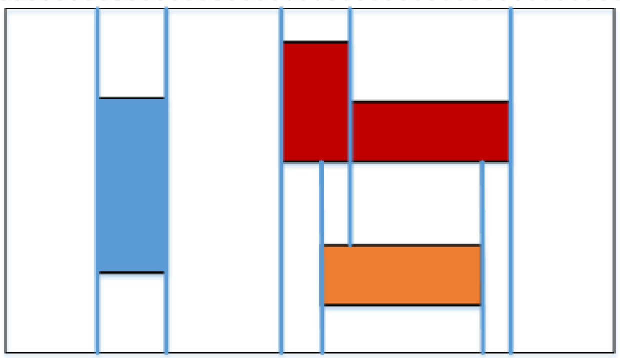
Corner Stitch

- **Layout area is tiled with non-overlapping rectangles:**
  - Empty tiles and different types of solid tiles
- **Each tile contains four pointers:**
  - Two at its top right corner, two at lower left
- **Rules for horizontal (vertical) corner stitch:**
  - Rule #1: First, each tile must be as wide (tall) as possible.
  - Rule #2: Then, each tile must be as tall (wide) as possible.





Horizontal Corner Stitch

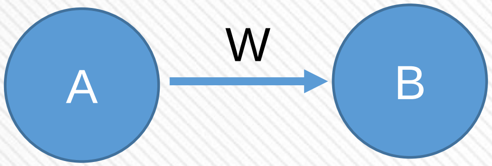


Vertical Corner Stitch

J. Ousterhout, "Corner Stitching: A Data-Structuring Technique for VLSI Layout Tools", TCAD, vol. 3, no. 1, pp. 87-100, January 1984

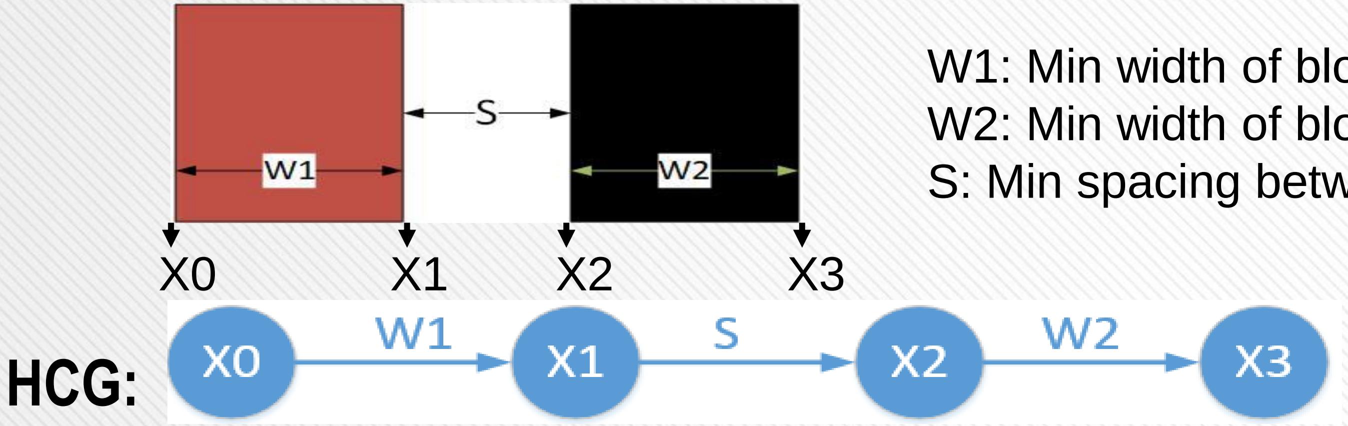
Constraint Graph

- Relationship between nodes with edges having minimum constraint value.



B>=A+W

- A layout can be represented using two graphs:
  - Horizontal constraint graph (HCG): Maintains horizontal relative location among components.
  - Vertical constraint graph (VCG): Maintains vertical relative location among components.



W1: Min width of block 1
W2: Min width of block 2
S: Min spacing between them

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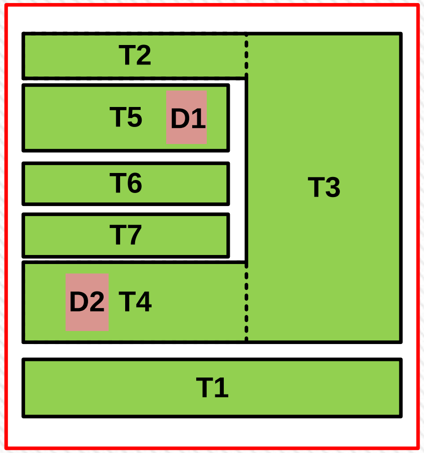
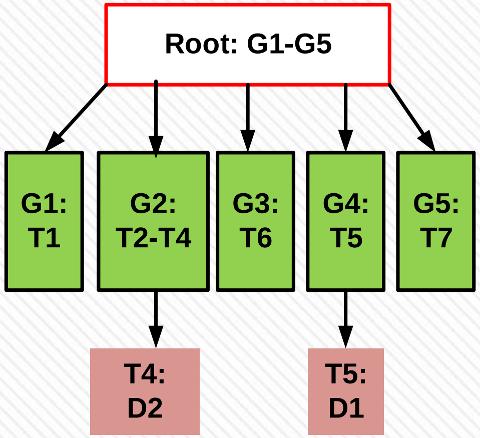
Hierarchical Corner Stitch

- **Basic corner stitch data structure is a planar one .**
- **A tree structure is maintained to consider hierarchy of the components in a layout.**

- **Tree structure construction:**
  - The root is the initial empty tile (substrate rectangle).
  - All components are inserted in a group-wise manner.
  - Two types of hierarchical nodes: parent (background tile) and children (foreground tile).



Layout of a power module



Tree Structure

- **In the example:**
  - All traces are in the root.
  - T2,T3, and T4 are in the same group as they are connected. D1 is placed on T5, that makes D1 child and T5 parent.

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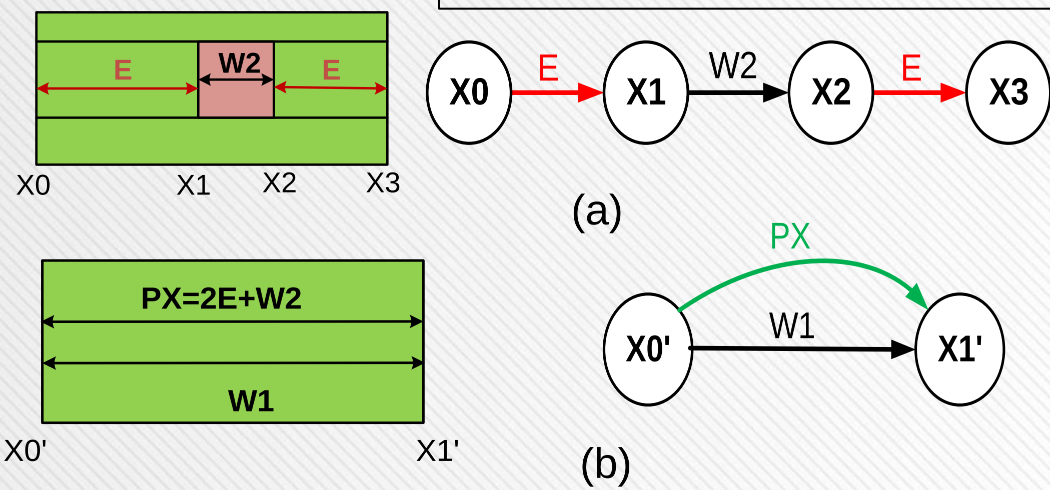
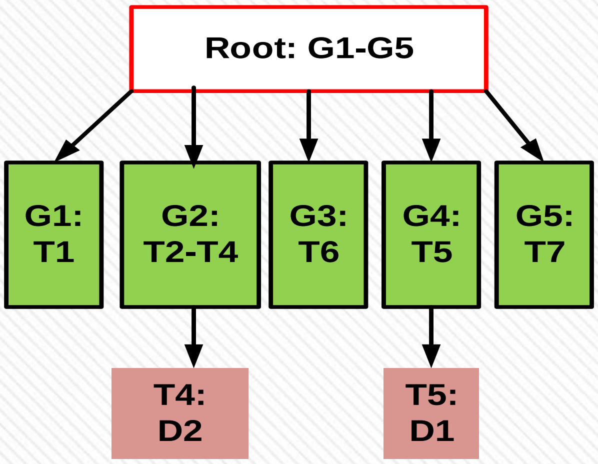
Hierarchical Constraint Graph

- **For each node in the tree, constraint graph (CG) is created.**
  - One-to-one mapping of the design constraints
- **Example**
  - From the tree, G4 (parent) and T5:D1 (child), hierarchical horizontal constraint graph is shown:

W2= min width of device (level-2)
W1= min width of trace (level-1)



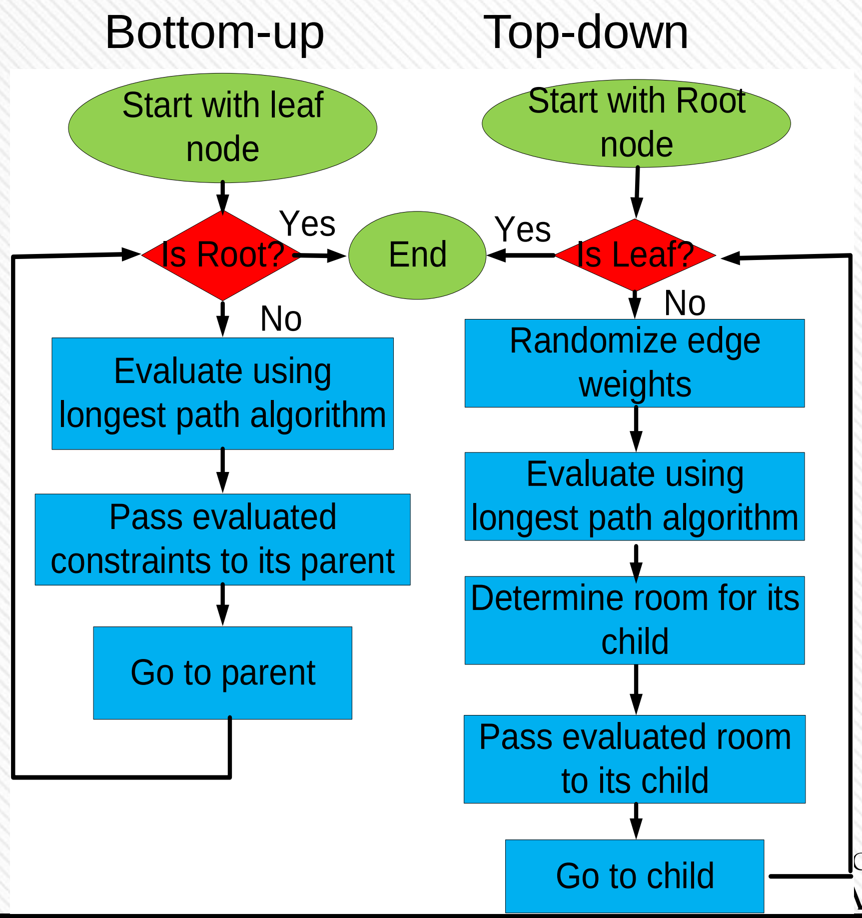


Tree Structure

Horizontal corner-stitched plane and corresponding HCG (a) child, (b) parent node

Evaluated Constraint Propagation

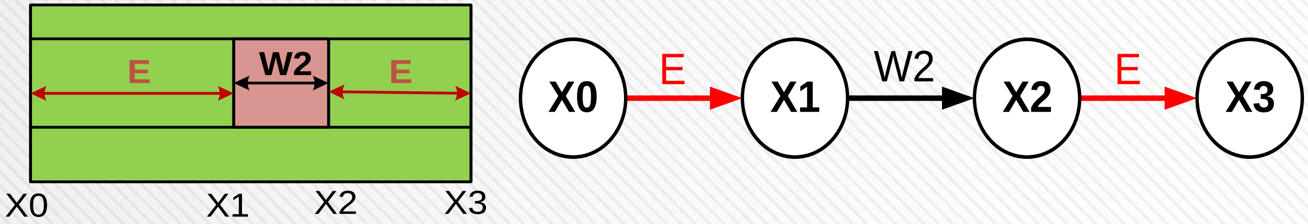
- **Each constraint graph is evaluated using longest path algorithm.**
- **The evaluated constraints are propagated in a bidirectional manner:**
  - **Bottom-up constraint propagation**
    - To generate DRC-clean solution, minimum constraint values are propagated from leaf-to-root.
  - **Top-down location propagation**
    - On arrival of all minimum constraint values, the root node is evaluated and determines appropriate room for each of its child node.
    - The evaluated room is propagated until all child node have their locations.



Fixed-Dimension Handling

❑ In flat level implementation:

- All edges are with variable weights.
- Results in variable dimensions of devices, leads, etc.



  - Here, W2 is the width of a device, which should be fixed. While evaluating the above constraint graph, the edge from X1-to-X2 is in the longest path from X0-to-X3. So, the weight varies during randomization step of CG evaluation.

❑ In this work:

- Algorithms are updated to preserve fixed dimension of necessary components.

Fixed-Dimension Handling

❑ To preserve fixed dimension of components:

- **Two types of edges are considered:**
  - Fixed edge: Having fixed (constant) weight (●·····●)
  - Non-fixed edge: weight can be varied (⟶)

- **Two types of vertices:**
  - Independent : locations are randomized independently. (🔴)
  - Dependent: locations are dependent on independent vertices. (🔵)

- **A vertex is dependent:**
  - If all incoming edges associated with the vertex are fixed edges.
  - No outgoing edges from that vertex to any independent vertex.
- **Dependent vertices are removable from the CG.**
- **Locations are calculated from the corresponding independent vertex.**

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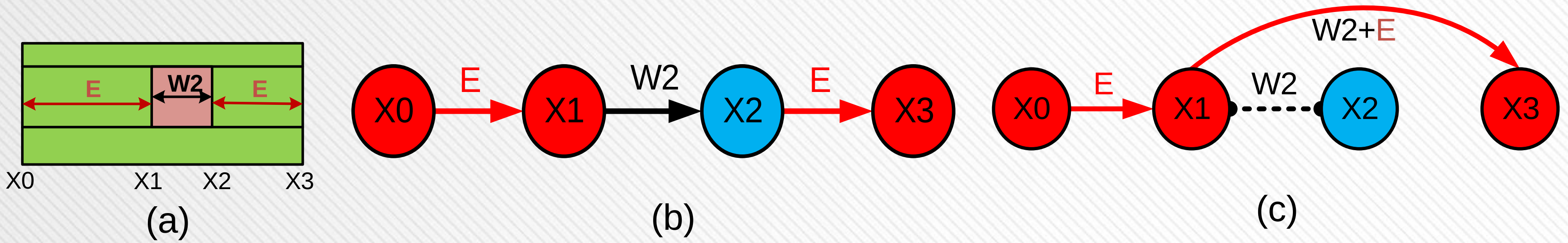
Fixed-Dimension Handling

- All fixed dimension components are mapped into CG with fixed edges.
- Example



(a) Horizontal corner-stitched layout (b) HCG (c) Modified HCG

- W2 is a constant weight
- X2 is dependent on X1
- X2 is removable vertex in the modified HCG

Modes of Operation

- **Four Modes of operation based on evaluation of CG:**

Mode	Purpose
0	Minimum sized layout
1	Variable floorplan sized layouts
2	Fixed floorplan sized layouts
3	Fixed floorplan with fixed component location layouts

- **Mode 0: minimum floorplan size is calculated in the root.**
  - locations are updated accordingly from top-to-bottom.
- **Mode 1-3:**
  - Edge weights in the root node is varied randomly (Mode 1)
  - Edge weights are randomized within the room determined by fixed floorplan (Mode 2,3).
  - Determined room is propagated and fixed floorplan algorithms are used to have final locations.

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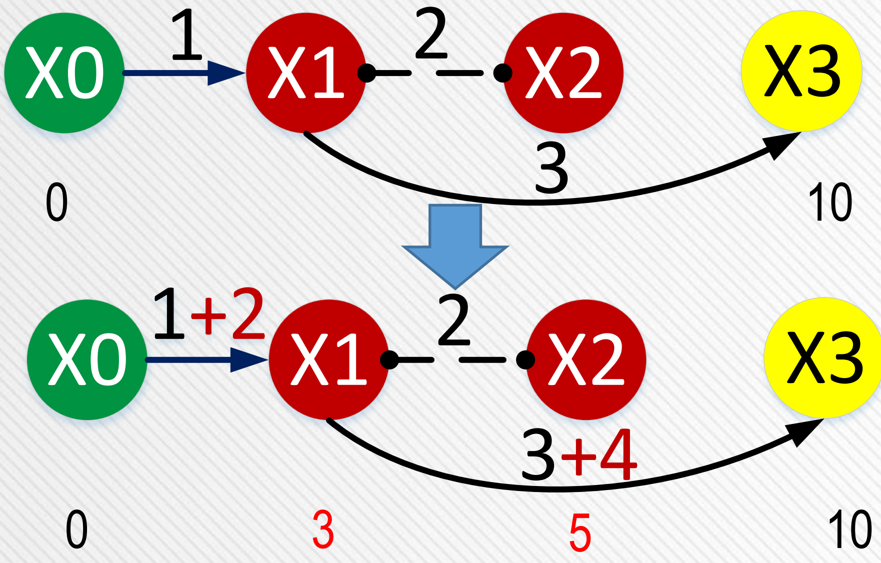
Randomization Method

- Used in all modes except minimum-sized solution.
- Enables creating arbitrary number of solutions without design rule violation.
- Steps:
  - Room = given size – minimum size
  - Distribute room among the edge weights on the longest path

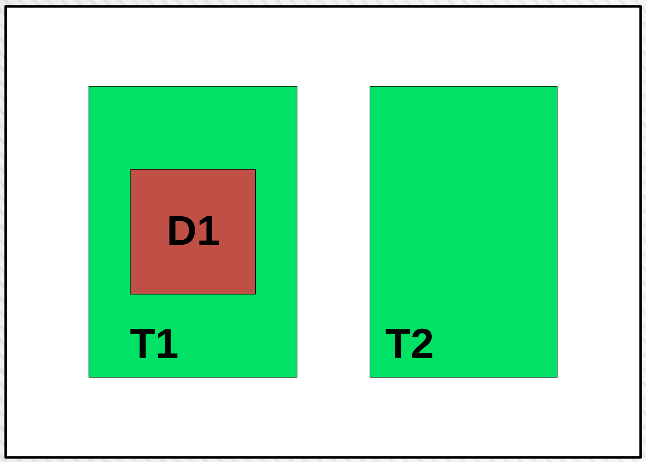


Given size=10
Minimum size= 4
Room=10-4=6.

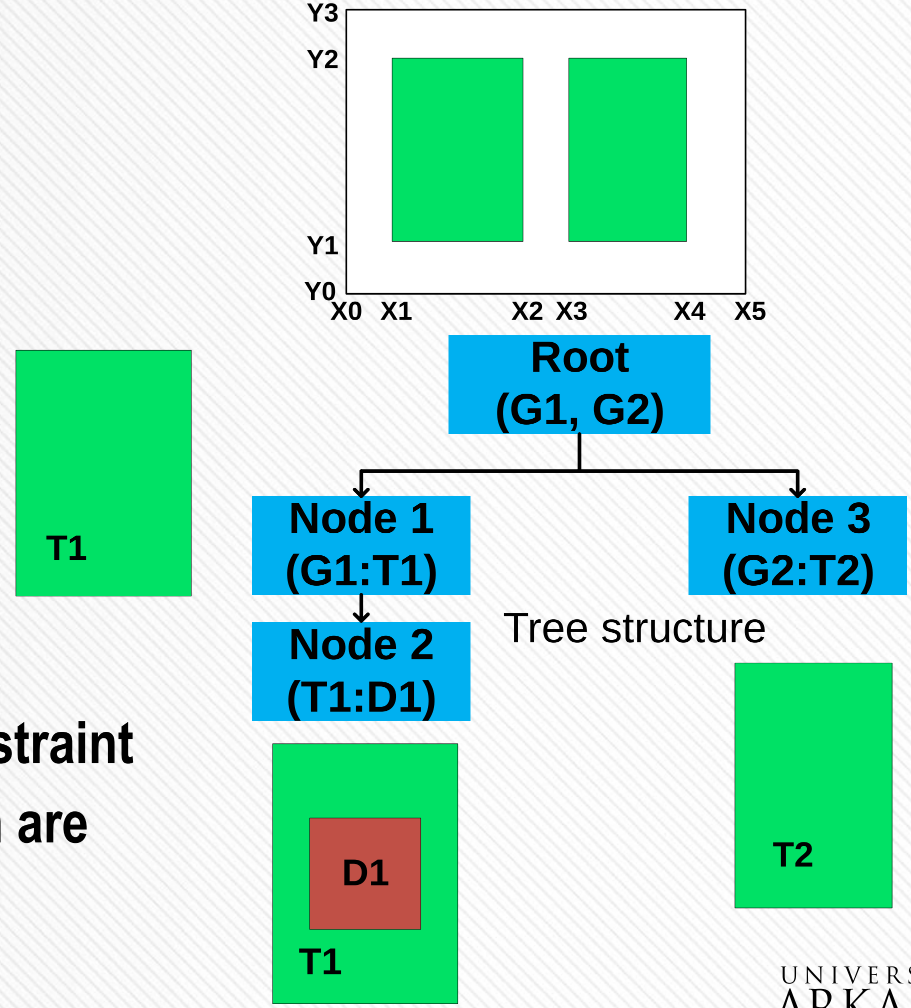
Distribute 6 among two edges on the longest path.
Say, 6 is divided into 2 and 4.

Sample Case

- A sample case is considered to show the hierarchical evaluation process:



Initial layout



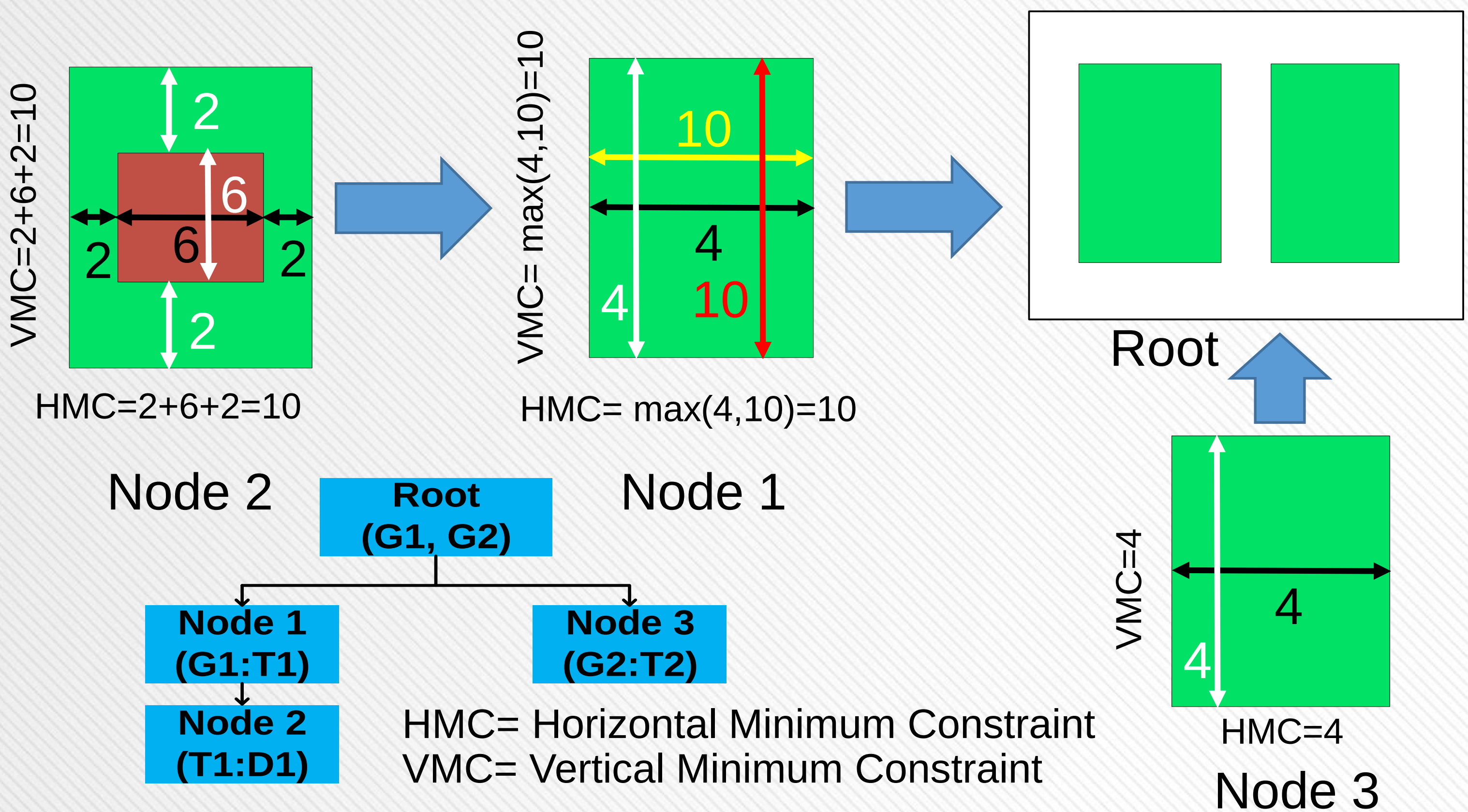
Tree structure

- For this example, bottom-up constraint and top-down location propagation are performed step-by-step.

Sample Case

❑ Bottom-up Constraint Propagation:

- Evaluate child node HCG and VCG
- Propagate the minimum constraints to parent node



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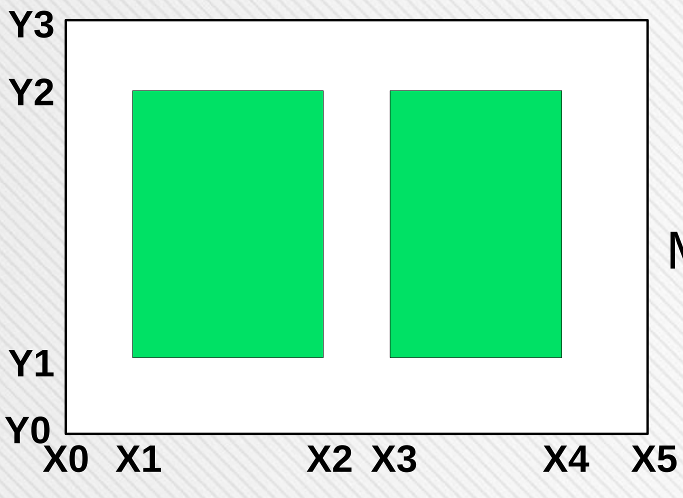
Sample Case

❑ Evaluation of Root Node:

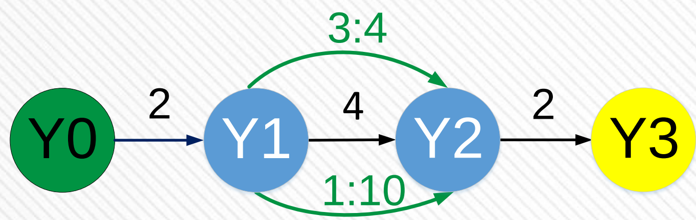
- Evaluate root node

Green edges = propagated edges



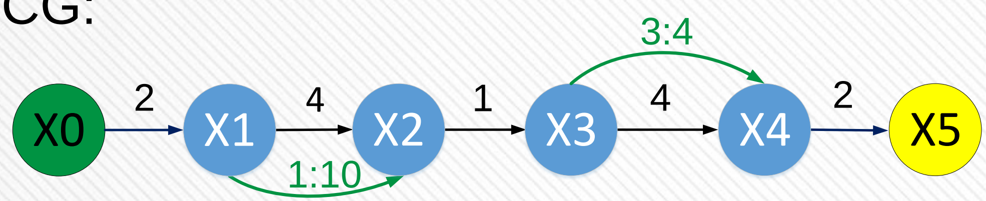
Root

VCG:



Min location: 0 2 12 14

HCG:



Min location: 0 2 12 13 17 19

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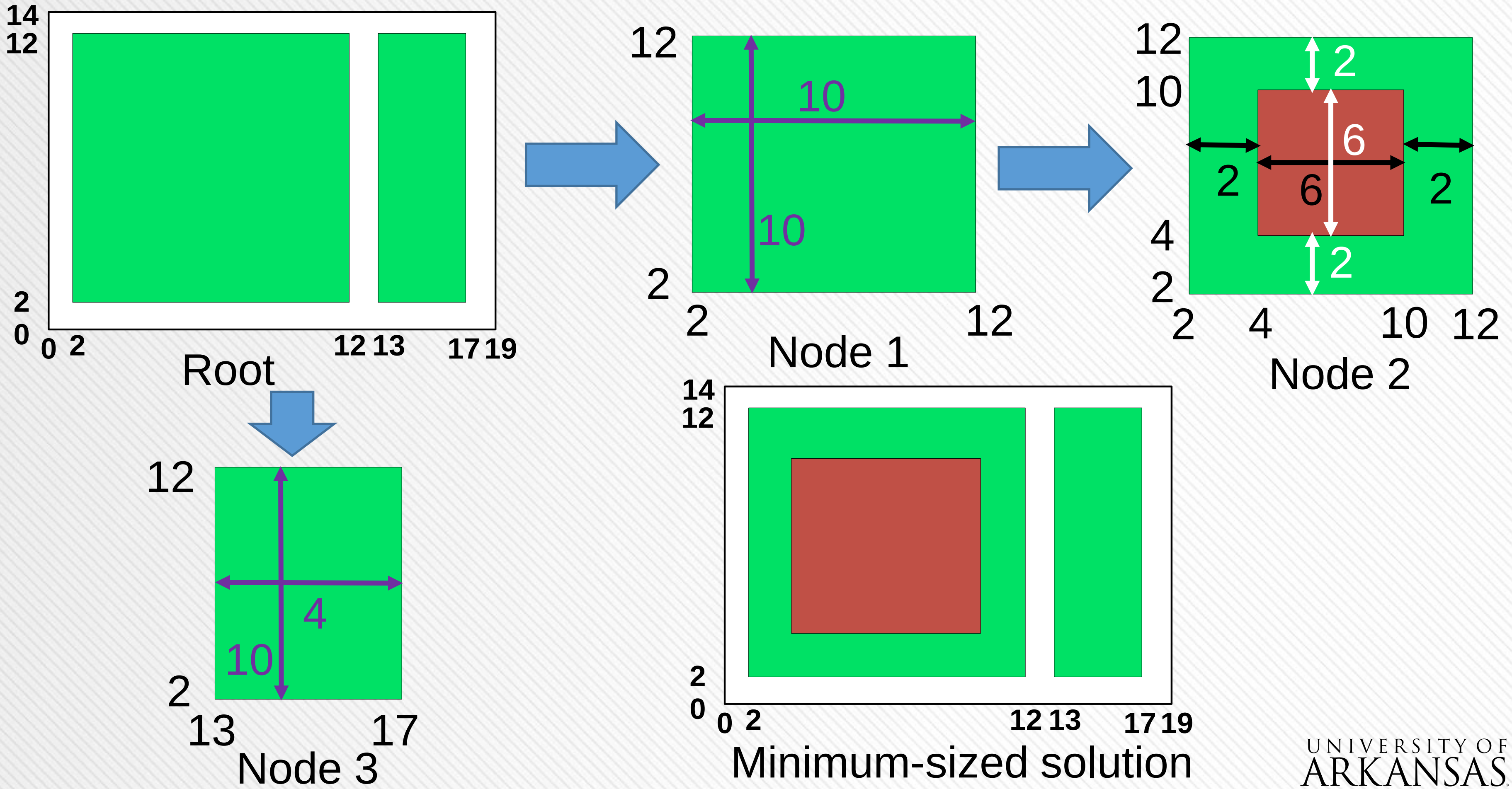
Sample Case

❑ Top-down Location Propagation:

- Propagate locations towards child node



Layout Optimization

- **Hardware-validated electrical and thermal models are used for performance evaluation.**
  - **Electrical: Loop inductance, resistance, capacitance**
  - **Thermal: Maximum temperature, average temperature**

- **Two optimization approaches can be considered:**
  - **Non-guided randomization**
    - Built-in solution generator in PowerSynth layout engine
    - Requires a good number of solutions for achieving a better optimized result.
  - **Non-dominated sorting genetic algorithm**
    - NSGAII is used for quick convergence.

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Hierarchical Vs Non-Hierarchical

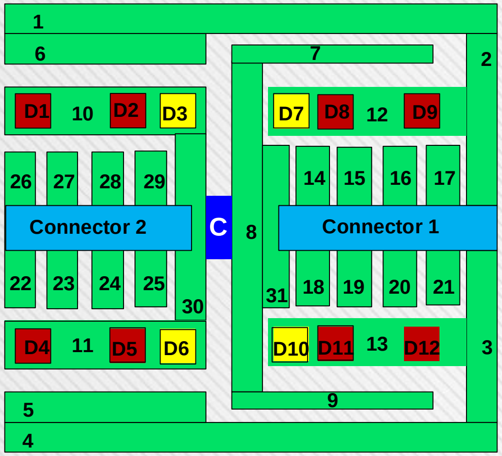
- Qualitative Comparison

Characteristics	Hierarchical Approach	Planar Approach
Benefits of symmetric geometry	Yes	No
Coordinate correlation	Less	Higher
Reusability of optimization results	Yes	No
Computational complexity	Less	Higher
Solution space	Larger	Smaller
Scalability	Higher	Less

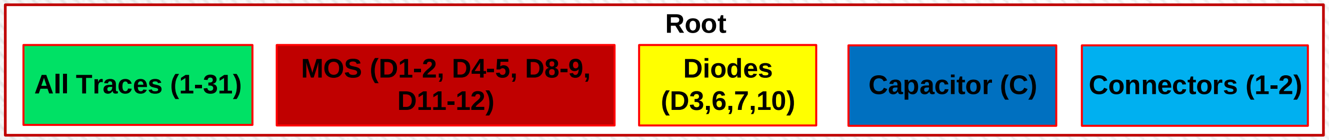
- **For 2.5D and 3D power module optimization, hierarchical approach is a better choice.**

Hierarchical Vs Non-Hierarchical

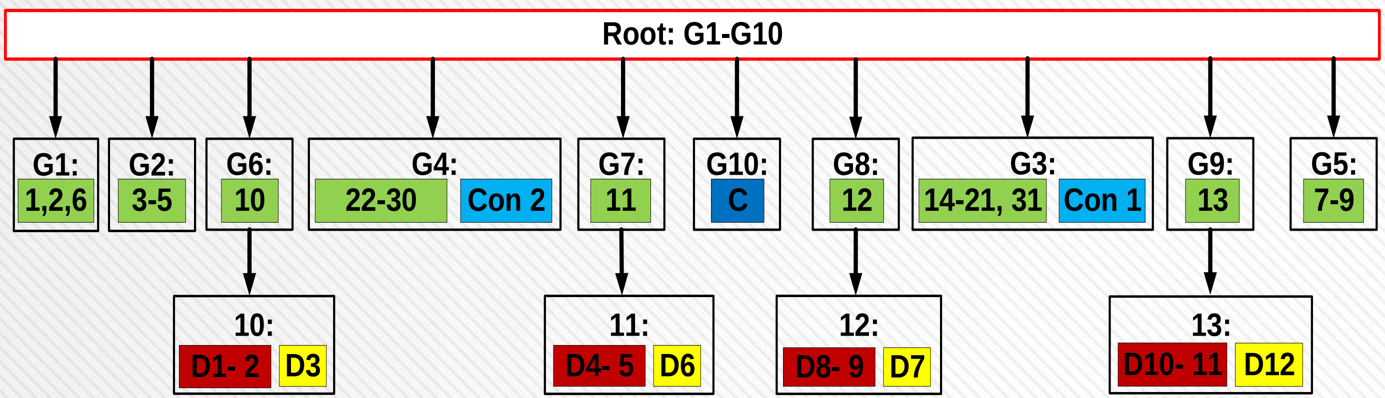
❑ Layout representation



H-bridge power module



Non- hierarchical Structure



Hierarchical Tree Structure

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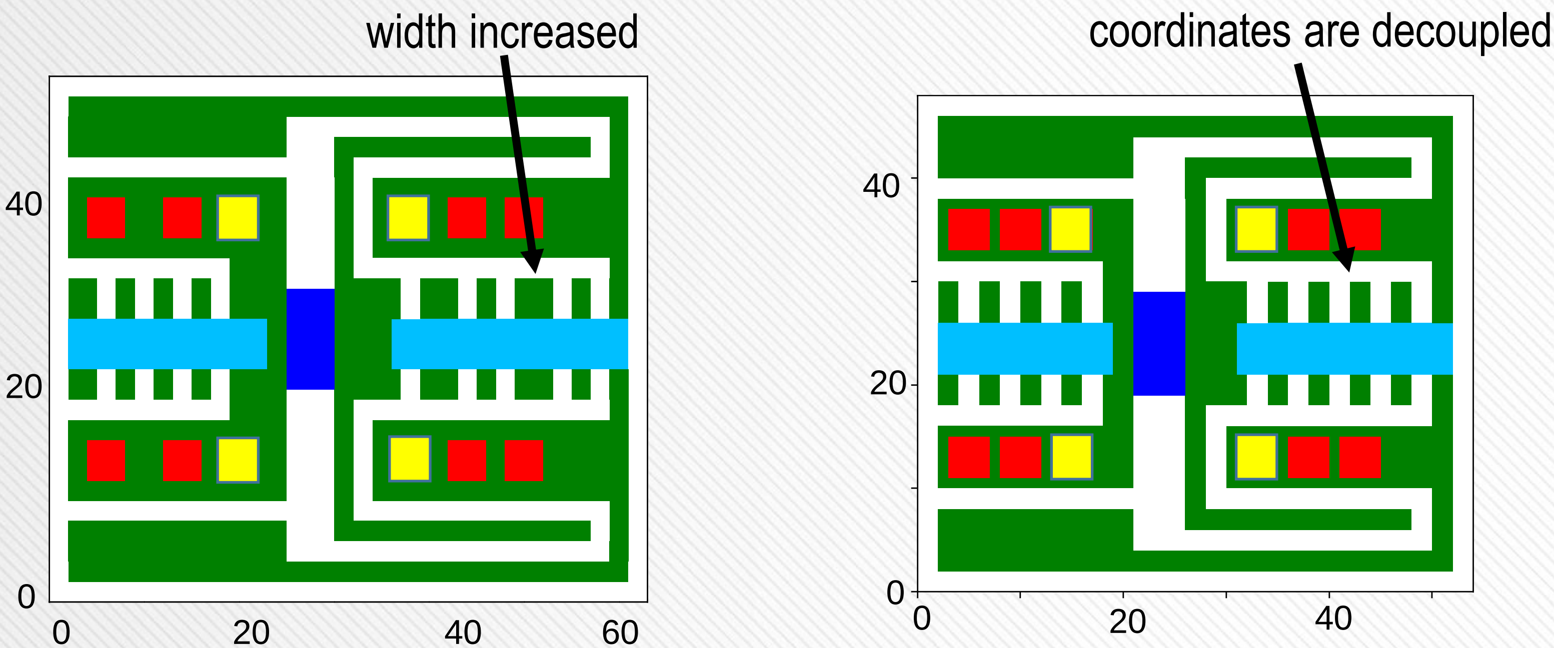
Results

- **Reduced coordinate correlation:**
  - Makes layouts more feasible
  - Layouts with more variation can be generated.

Minimum-sized layout



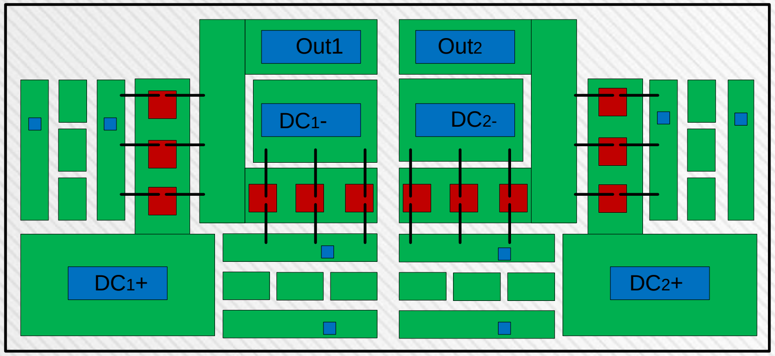
Non-hierarchical (63×52)

Hierarchical (54×48)

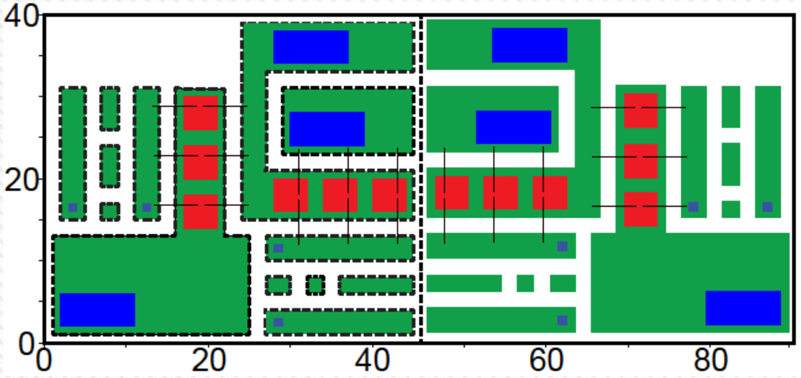
Results

❑ Runtime Improvement :

- **An improved electrical model with current density consideration**
- **The power loop inductance from DC_{1+} - DC_{1-}**
  - For planar approach, computational time is 5.05s.
  - Hierarchy reduces computational time to 0.43s
- **Hierarchy consideration gives 12 times speedup for a single solution.**
  - With reduced problem size



Full-bridge power module



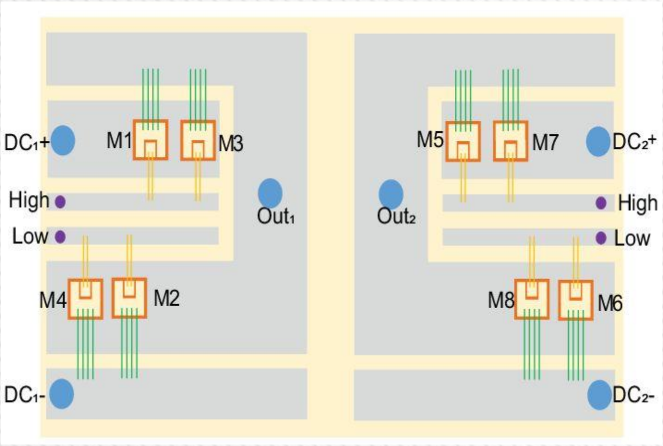
Minimum-sized solution (94×40)

Q. Le et al., "PEEC Method and Hierarchical Approach Towards 3D Multichip Power Module (MCPM) Layout Optimization," IWIPP,2019

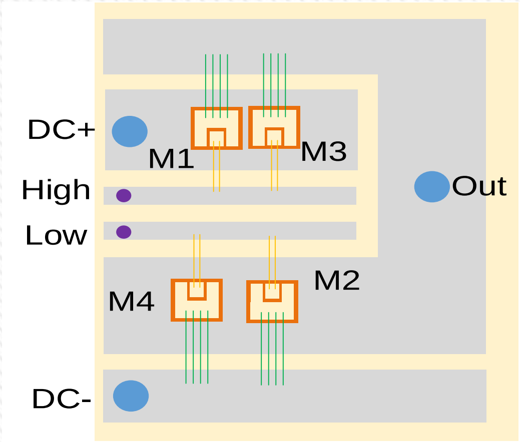
Results

❑ 2.5D Full-Bridge Layout Optimization :

- Hierarchy enables to perform optimization part-by-part.
- Only half of the layout needs to be optimized
- Reduces computational effort by half



Full-bridge power module



Half-bridge power module

- To optimize the loop inductance from DC_{1+} to DC_{2-}, only DC_{1+} -to-DC_{1-} (left half) path can be considered including load inductance due the symmetry.

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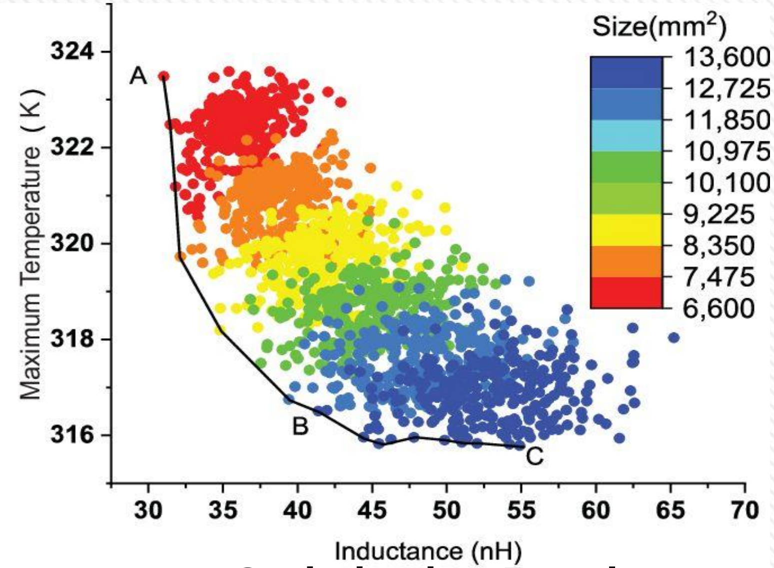
Results

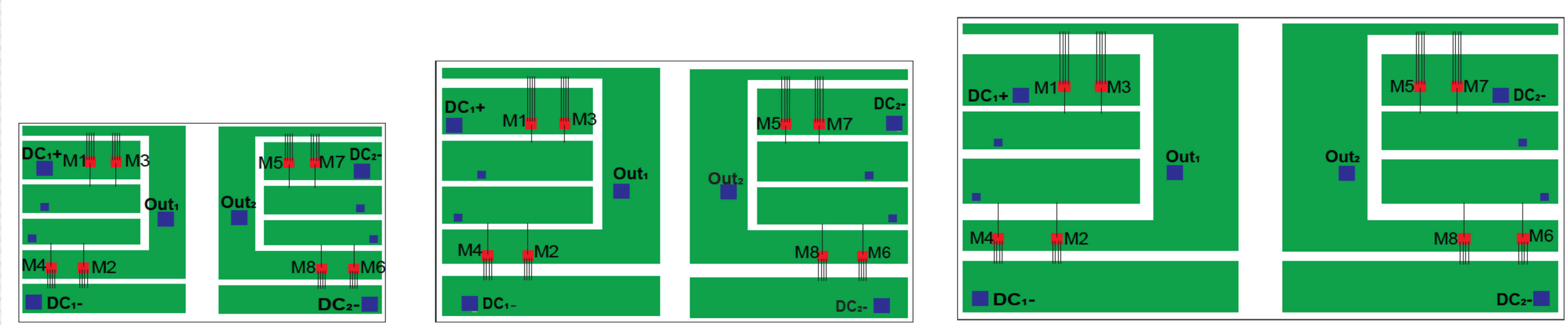
❑ Loop Inductance vs Maximum Temperature:

- For thermal evaluation, the whole full-bridge base plate is characterized.
- For loop inductance, half loop from DC_{1+} to DC_{1-} (with 8nH load inductance) is considered
- 1000 layout solutions are considered



Optimization Results

Three layouts (A,B,C) on the Pareto-front :



(a) (b) (c)

Conclusions

❑ Conclusions:

- Our hierarchical layout algorithm provides a structural design automation method towards optimizing complicated large-scale power design layouts.
- It reduces computational complexity and conflicts among layout components over the traditional planar approach.
- This methodology is scalable to handle an arbitrary number and different types of components in the layout.
- System-level optimization can be benefited by the reduction in design optimization time through hierarchical approach.

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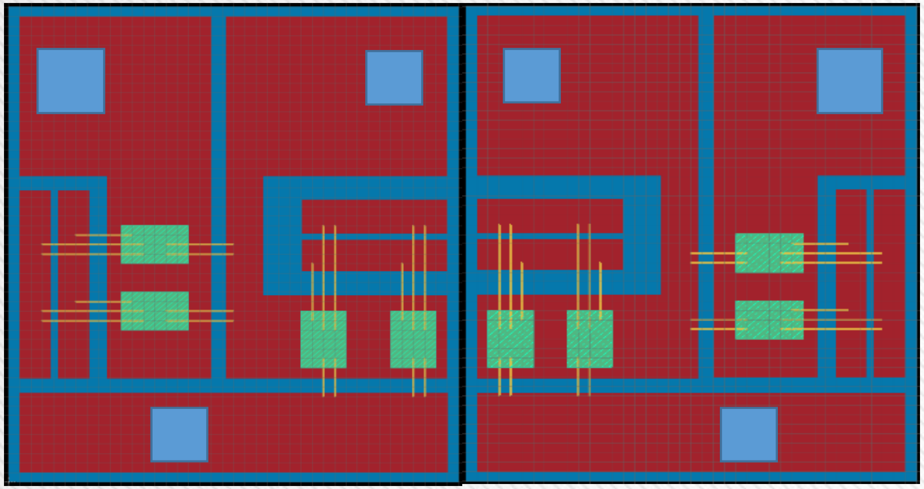
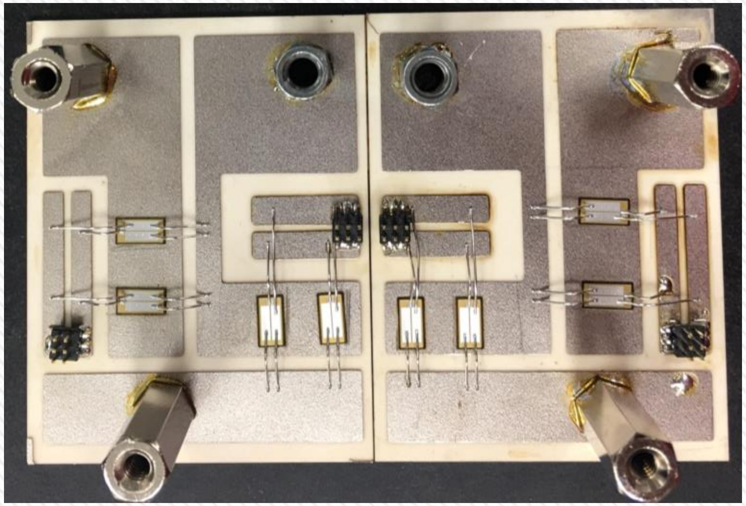
Future Work

- **On-going and Future Work:**
  - **Algorithms for handling intra-layer and inter-layer connections.**
  - **Hardware validation.**



Auto-generated optimized power module



Fabricated module

  - **3D power modules optimization.**

QUESTIONS