Constraint-Aware Algorithms for Heterogeneous Power Module Layout Synthesis and Reliability Optimization

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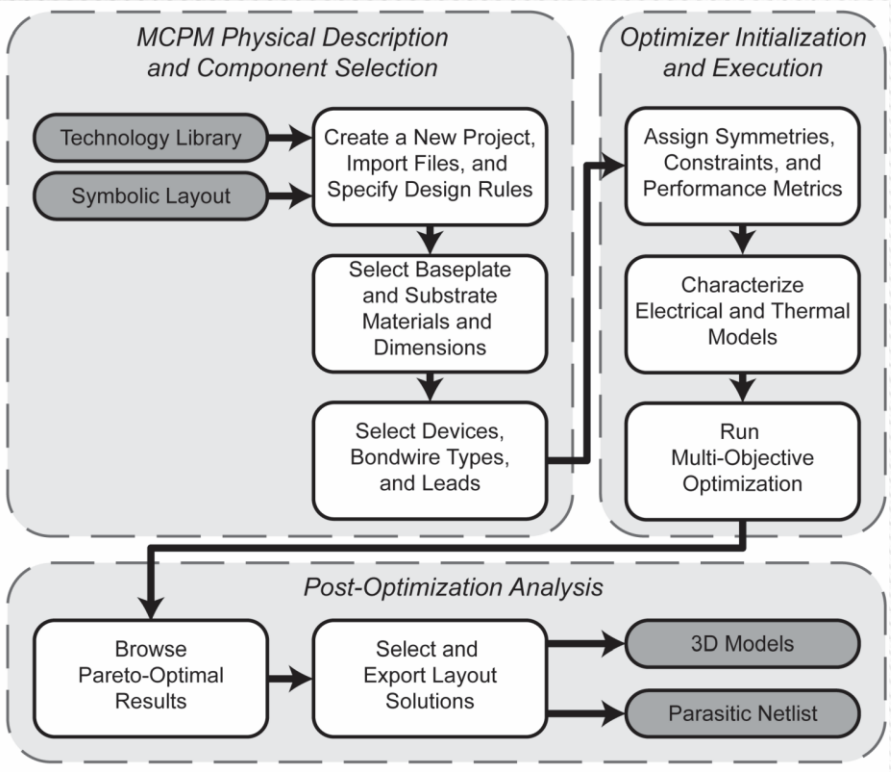
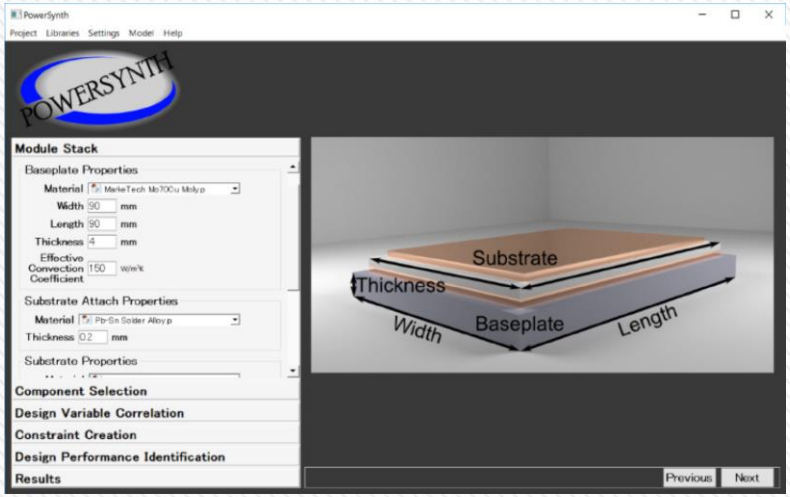
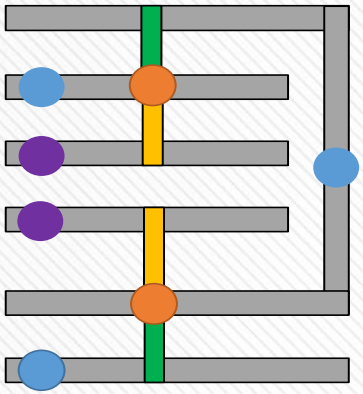
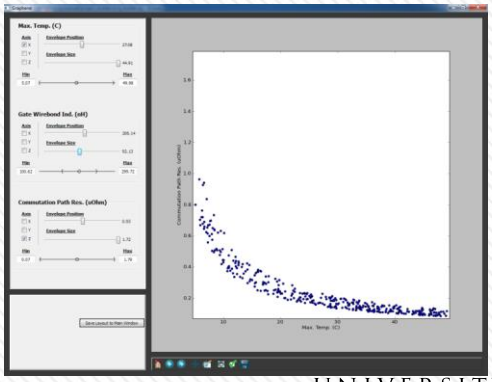
Introduction to PowerSynth

- First Multi-Chip Power Module (MCPM) layout synthesis tool that exploits multi-objective optimization to generate optimum layout solutions









Motivation and Approach

- **Motivation:**
  - PowerSynth current layout engine can optimize 2D power module layouts with limited geometric configurations.
  - DRC unawareness in generation phase: not suitable for heterogeneous and 3D power module.
- **Objective:**
  - To create a constraint-aware layout engine, capable of:
    - Considering both design and reliability constraints
    - Considering heterogeneous components (EMI filter, gate driver, sensors)
    - Implementing generic and scalable algorithms for optimization
    - Processing broader range of layouts with higher complexity
- **Methodologies: Corner Stitch, Constraint Graph, Optimization Algorithms**

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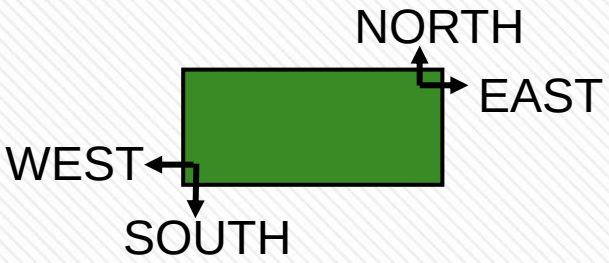
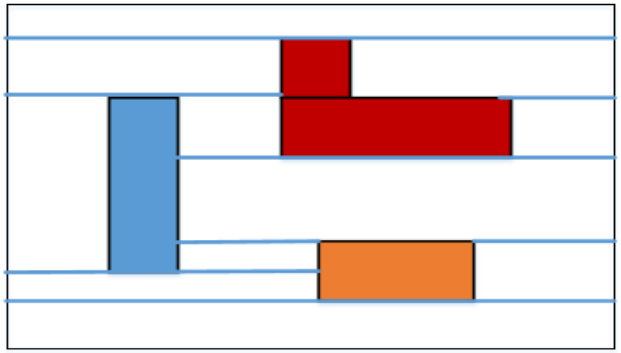
Corner Stitch

- **Layout area is tiled with non-overlapping rectangles:**
  - Empty tiles and different types of solid tiles
- **Each tile contains four pointers:**
  - Two at its top right corner, two at lower left
- **Rules for horizontal (vertical) corner stitch:**
  - Rule #1: First, each tile must be as wide (tall) as possible.
  - Rule #2: Then, each tile must be as tall (wide) as possible.

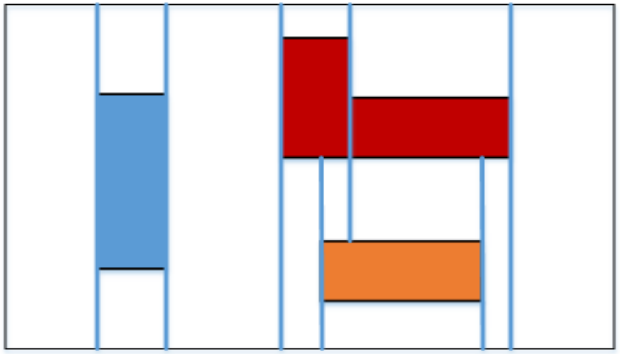




Filled → SOLID

Not Filled → EMPTY

Different color → Different component



Horizontal Corner Stitch

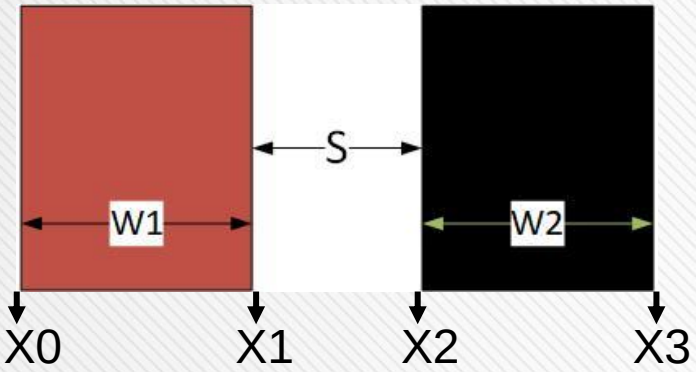
Vertical Corner Stitch

Constraint Graph

- **Relationship between nodes with edges having minimum constraint value.**

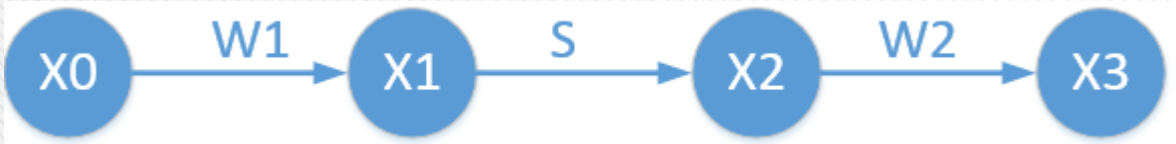
B>=A+W

- **Two Types of Constraint Graphs:**
  - Horizontal/Vertical Constraint Graph (HCG/VCG)



W1: Min width of block 1
W2: Min width of block 2
S: Min spacing between them

HCG:



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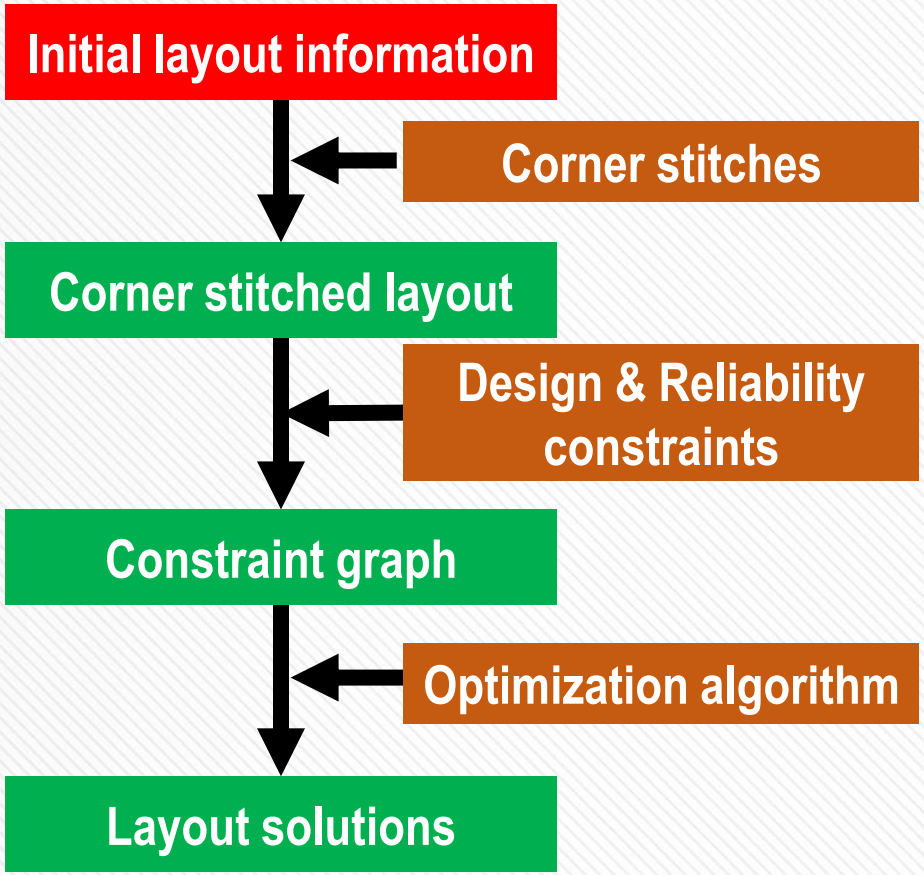
Methodology

- **Overall flow of methodology:**
  - User-defined initial layout
  - Create initial data structure
  - Create constraint graphs for DRC aware layout
  - Generate candidate layouts
  - Use electrical/thermal cost functions for optimization
  - Generate Pareto surface and select best layouts

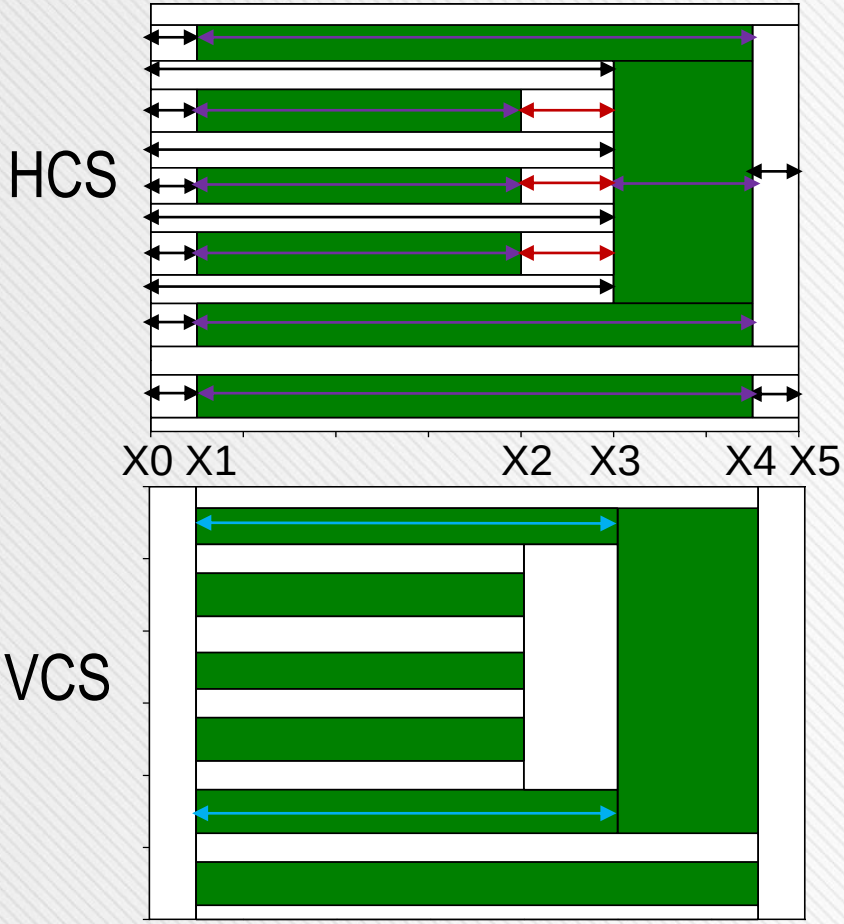


Incorporated Constraints

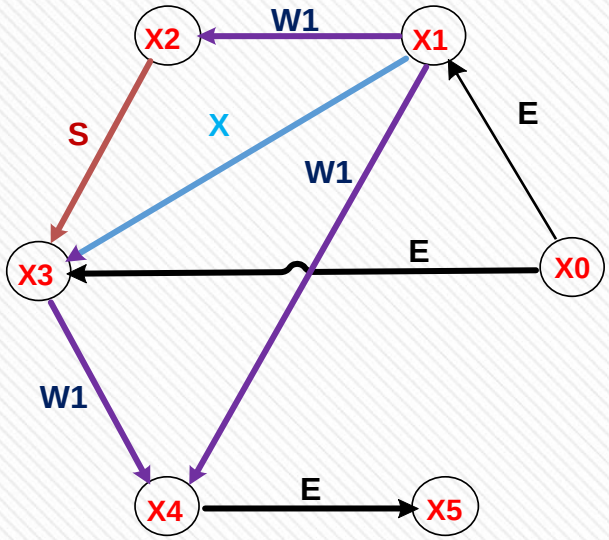
- **Design Constraints:**
  - **To generate DRC-clean fabrication-feasible layouts:**
    - Minimum width along x and y direction
    - Minimum spacing between two components
    - Minimum enclosure of one component to another
    - Minimum extension along horizontal and vertical
- **Reliability Constraints:**
  - **To minimize thermal and electrical (i.e. partial discharge) concerns:**
    - Current-dependent minimum width
    - Voltage-dependent minimum spacing

Horizontal Constraint Graph (HCG)

- **An illustration of creating horizontal constraint graph:**



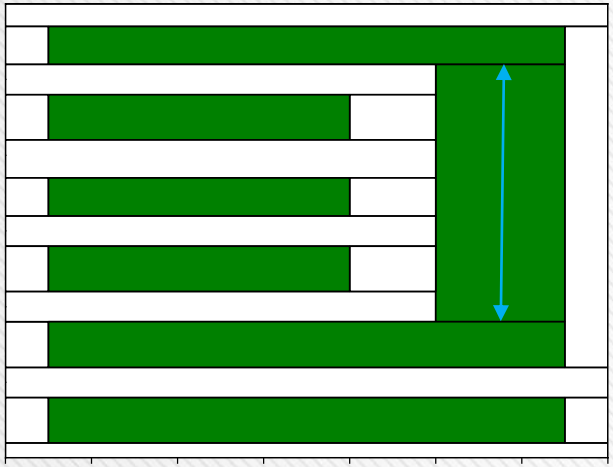
S: Min Spacing
W: Min Width
E: Min Enclosure
X: Min Extension

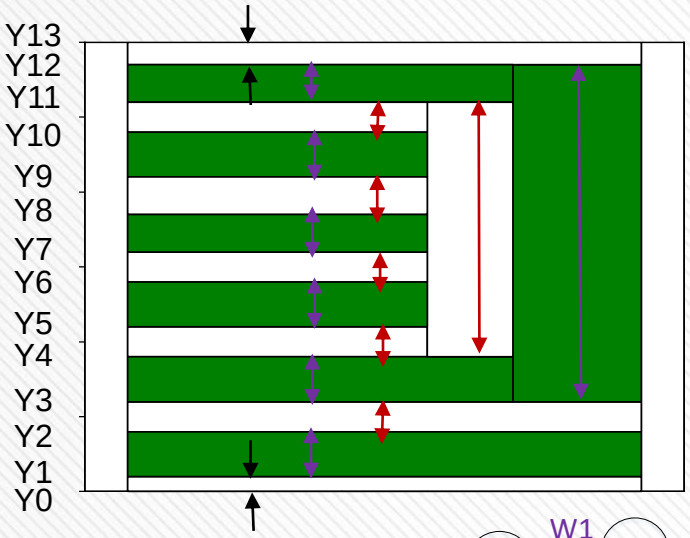


HCG

Vertical Constraint Graph (VCG)

HCS

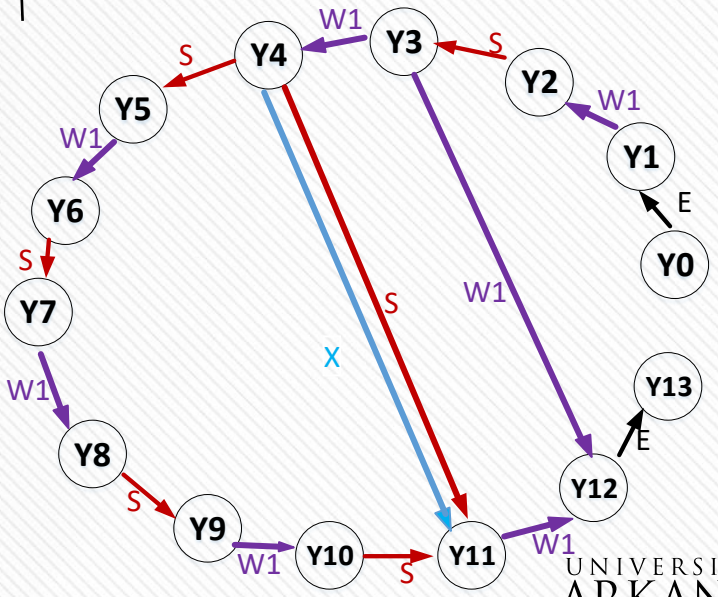




VCS

S: Min Spacing
W: Min Width
E: Min Enclosure
X: Min Extension

VCG



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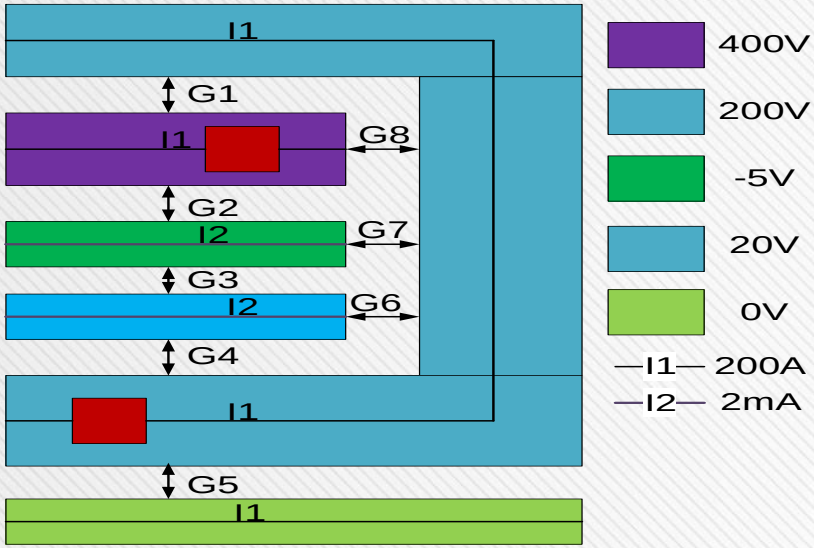
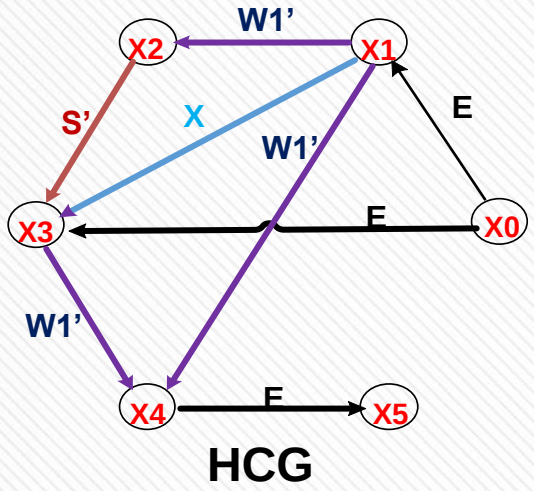
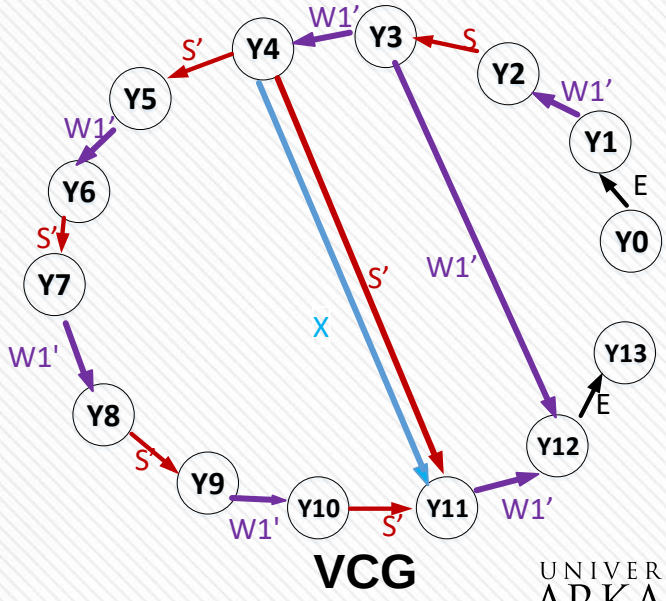
Reliability Constraints

- **I-V value assigned:**







Here, all width (W1') and spacing (S') edge weights are modified to consider reliability constraints, because of high voltage-and-current loading.

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Optimization Algorithms

- Our optimization algorithms have four operating modes-

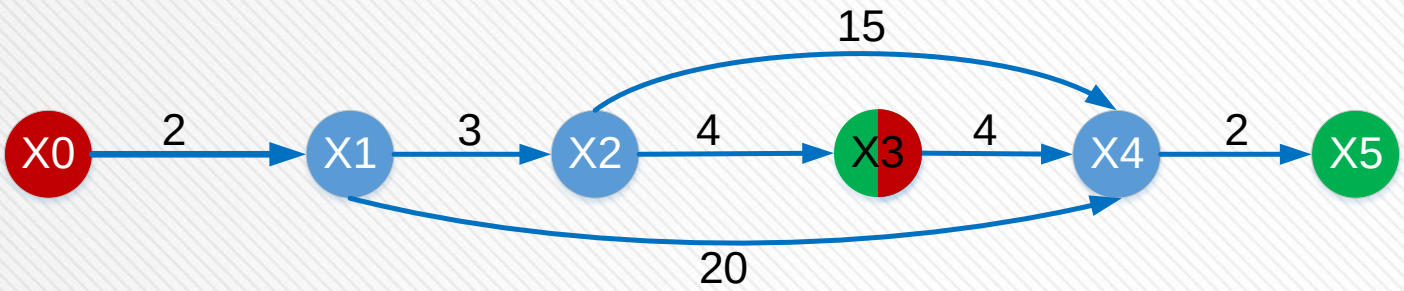
Mode	Purpose	Evaluation Methodology
0	Minimum sized layout	Minimum constraint values
1	Variable floorplan sized layouts	All weights are randomized with minimum constraints No maximum constraint
2	Fixed floorplan sized layouts	All weights are randomized with minimum constraints Some have maximum constraints
3	Fixed floorplan with fixed component location layouts	

Optimization Algorithms

Terminology:

- Source Node: No incoming edge but outgoing edges. Source nodes will always have a fixed location.
- Sink Node: No outgoing edge but incoming edges. Sink nodes may have fixed locations.
- Fixed Node: Has the same max and min location. Can be treated as a source or sink node.
- Non-Fixed Node: Location is not fixed yet. Need to be evaluated

Red- Source
Green-Sink
Blue- Non-fixed



E.g., this graph has fixed nodes: X0,X3,X5

Minimum Sized Layout (Mode 0)

- Min location is determined using longest path algorithm

HCG (VCG)

↓

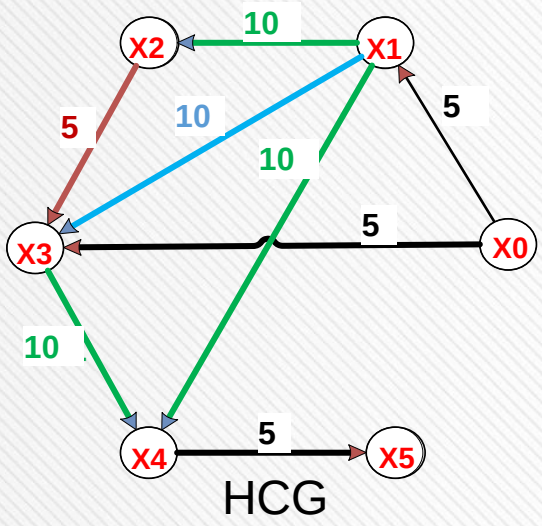
Longest path algorithm

↓

Evaluated HCG (VCG)

↓

Minimum sized layout



HCG

Min constraint values:
E=5 X=10
S=5 W1=10

Node	Parent	Incremental Value	Min Location
X0 Source	-	-	0
X1	X0	0+5	5
X2	X1	5+10	15
X3	X1 X2 X0	5+10 15+5 0+5	20
X4	X1 X3	5+10 20+10	30
X5	X4	30+5	35

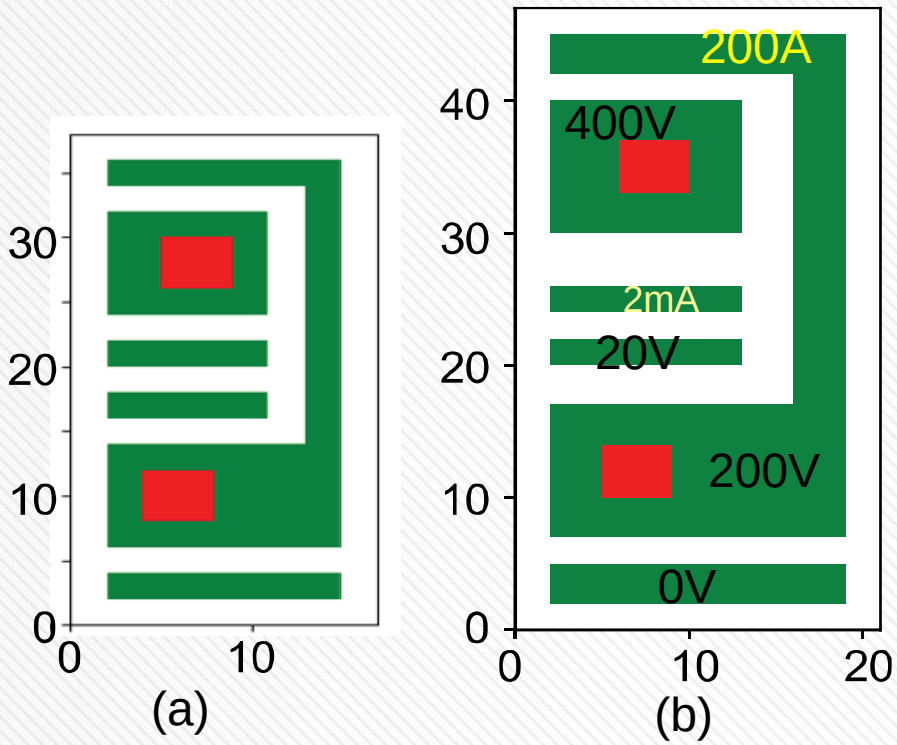
Minimum Sized Layout

Constraint Values:

V Diff. (V)	Spacing (mm)
100	1
200	2
300	3
400	4

Trace I (A)	Width (mm)
200	3
1	2

Design Constraint	Value
Trace Min width	2 mm
Trace to Trace gap	2 mm
Ledge width	2 mm
Die to trace enclosure	1 mm

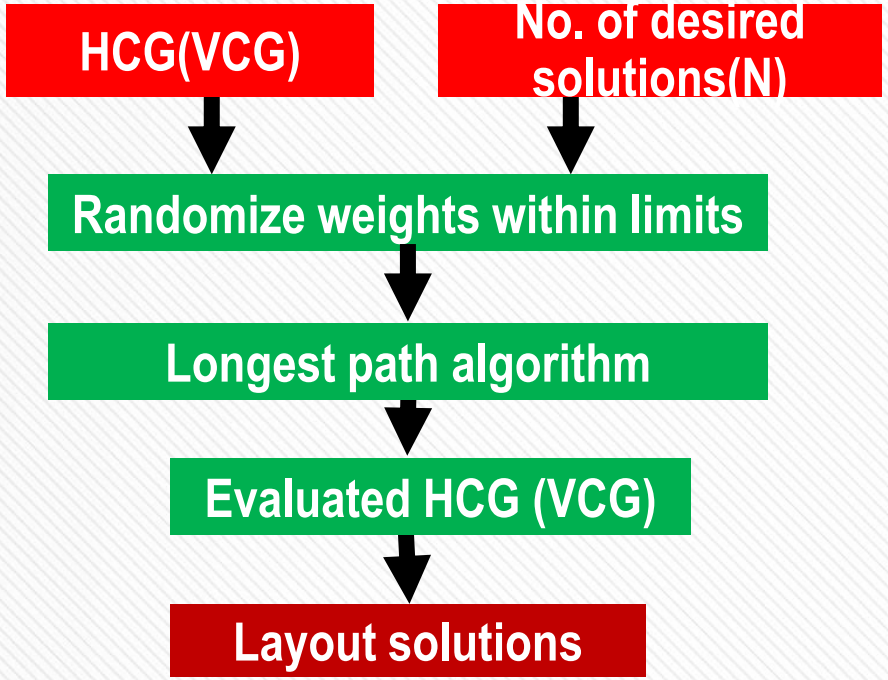


Minimum-sized layout with (a) design constraints only, (b) both design and reliability constraints

Variable Sized Layouts (Mode 1)

- **For Mode-1 optimization the following algorithmic flow is implemented:**
  - In constraint graph, each weight is varied within certain limit:

  (minimum constraint value, random maximum value)
  - HCG evaluation gives x locations.
  - VCG evaluation gives y locations.
  - Whole process is iterated over N times.

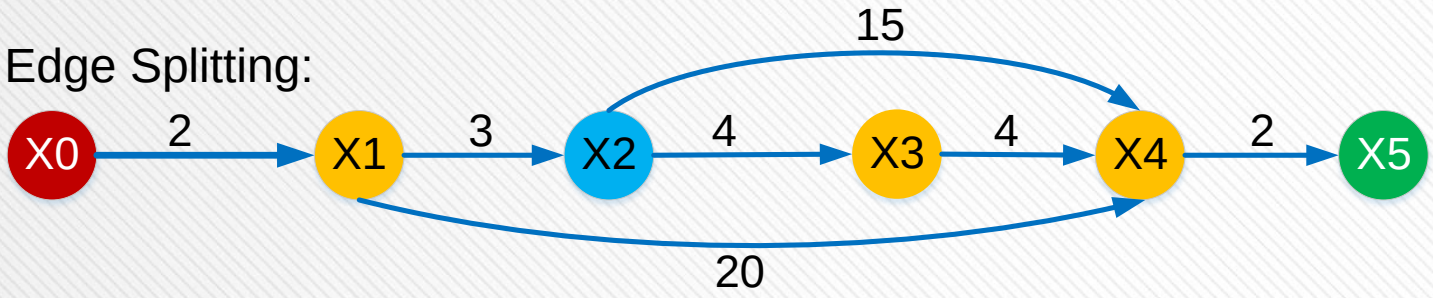


Fixed Floorplan (Mode 2&3)

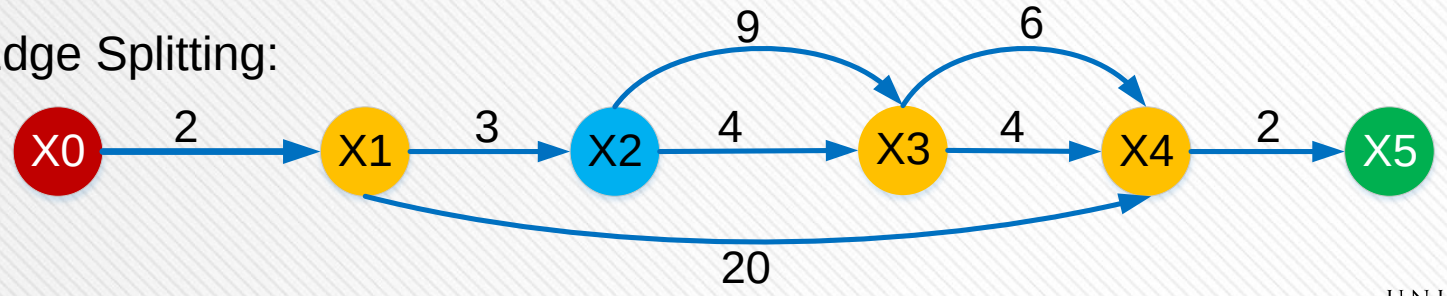
- **Edge Splitting: An edge can be split into two parts, if:**
  - The edge has source or destination at a fixed node.
  - The edge bypasses any fixed node.

Node	X0	X1	X2	X3	X4	X5
Location	0	11	Not fixed	30	36	40

Before Edge Splitting:



After Edge Splitting:



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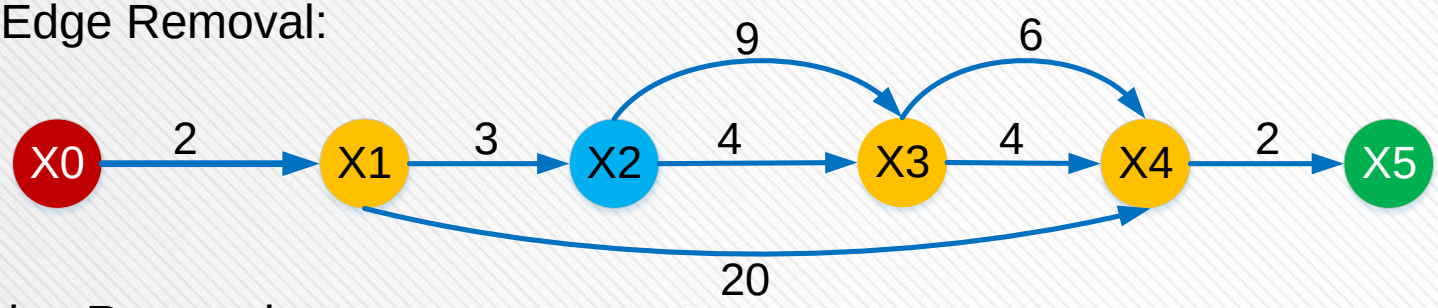
Fixed Floorplan (Mode 2&3)

❑ Edge Removal: An edge can be removed, if:

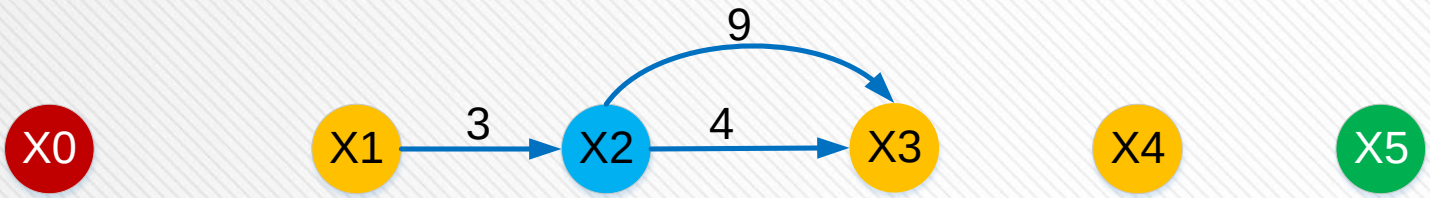
- The edge has both source and destination at fixed nodes.

Node	X0	X1	X2	X3	X4	X5
Location	0	11	Not fixed	30	36	40

Before Edge Removal:



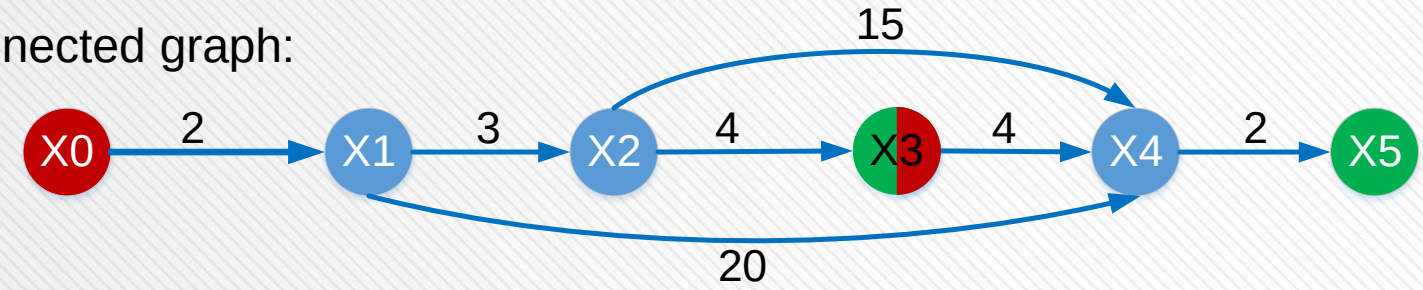
After Edge Removal:



Fixed Floorplan (Mode 2&3)

- **A graph can be split into Sub Connected Graphs:**
  - There is no dependency (connected edge) between each part

A connected graph:



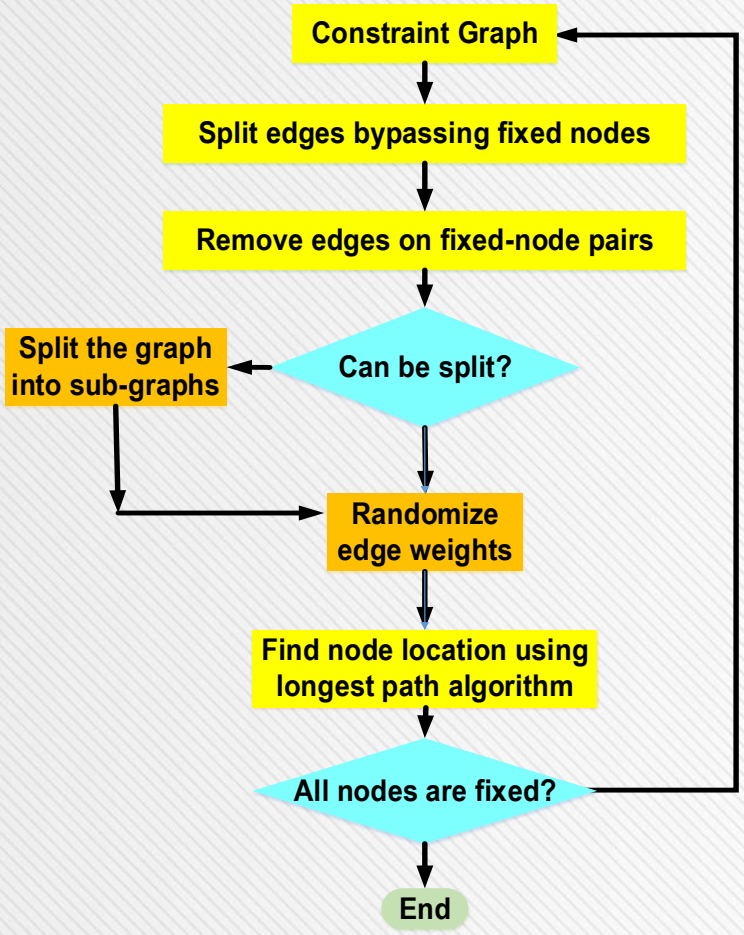
A graph that can be split:

Sub-graph 1:

Sub-graph 2:

Fixed Floorplan (Mode 2&3)

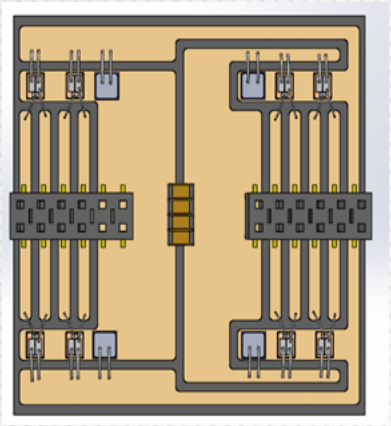
❑ Mode-2 and 3 optimization algorithmic flow:



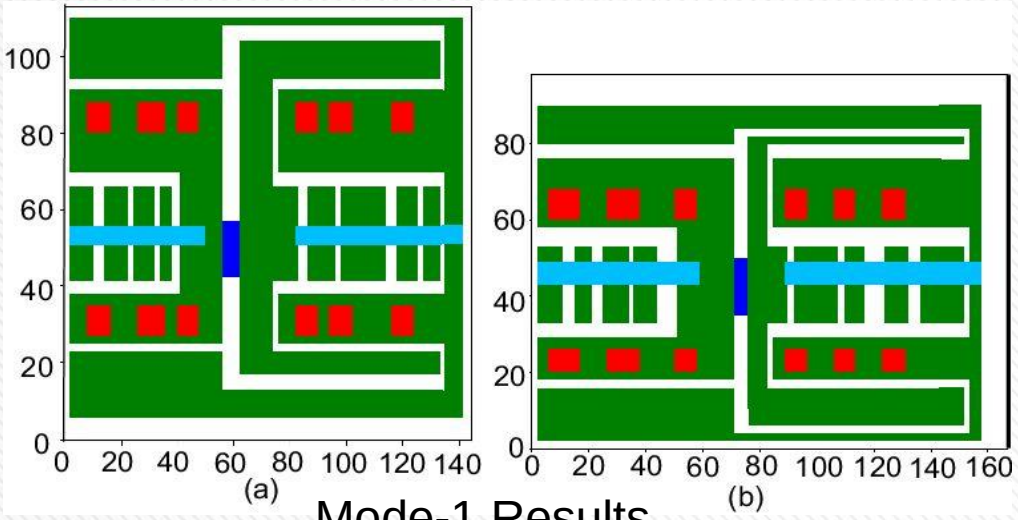
Input: Constraint Graph (G)
Output: Node locations
Function (G):

Split Edge (start, mid, end)
If fixed edge is found:
Remove edge
Split into connected graphs
For each subgraph:
Evaluate graph
If all node locations are fixed:
return
Else:
Function (G)

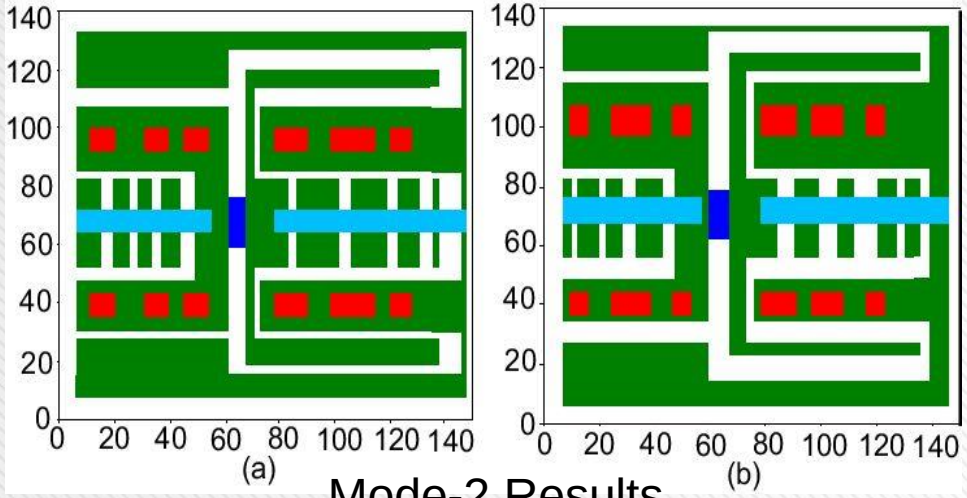
Experimental Results (Mode-1,2,3)



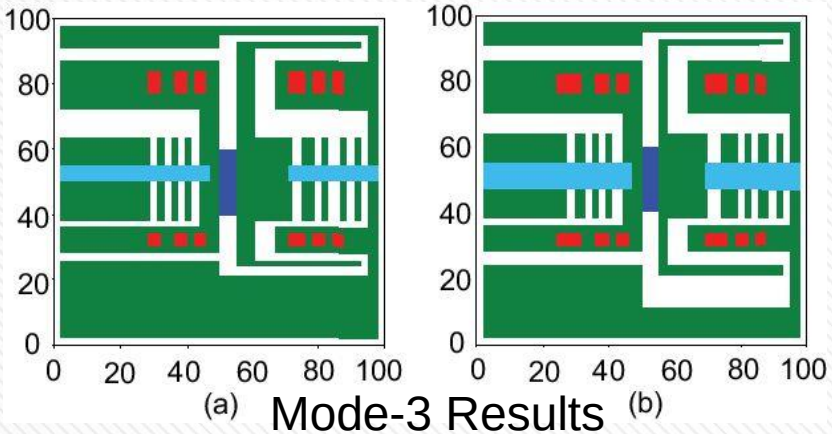
H-Bridge Power Module



Mode-1 Results



Mode-2 Results



Mode-3 Results

DC link cap is fixed at (50,40)

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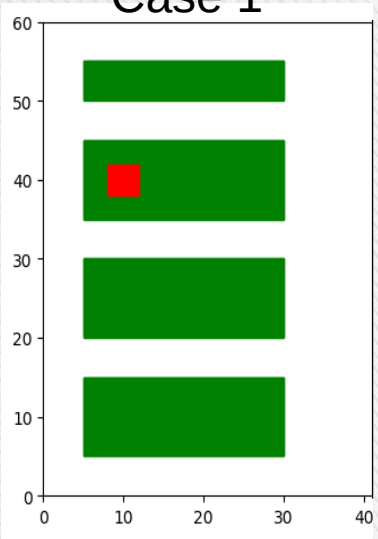
Efficiency Comparison

Case #	Valid # out of 3015 layouts		Time for each valid layout (s)	
	Current	Proposed	Current	Proposed
1	76	3015	0.0098	0.0012
2	1883	3015	0.0006	0.0023
3	0	3015	N/A	0.0113

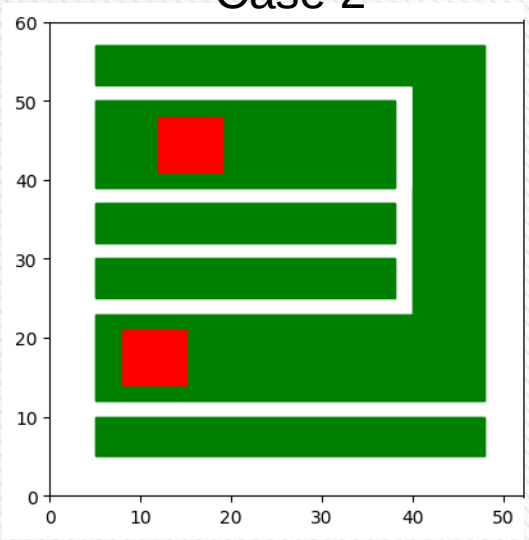
- **Current layout engine cons:**

1.Only fixed floorplan sized layouts
2. Not scalable
3. Limited layout representation capability.

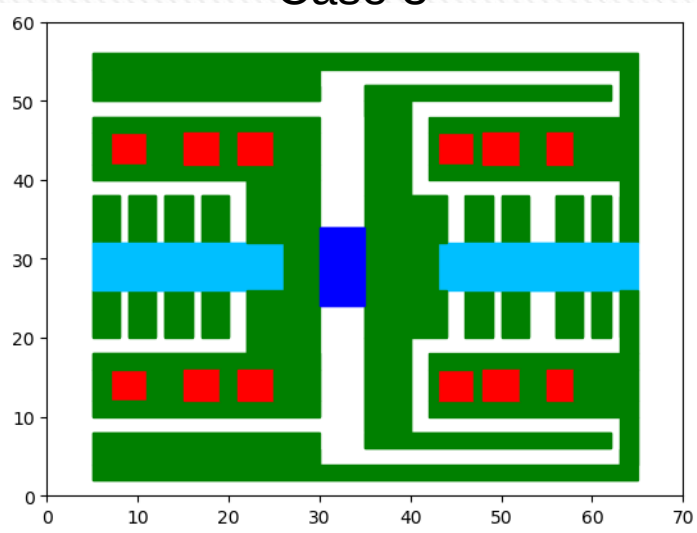
Case 1



Case 2

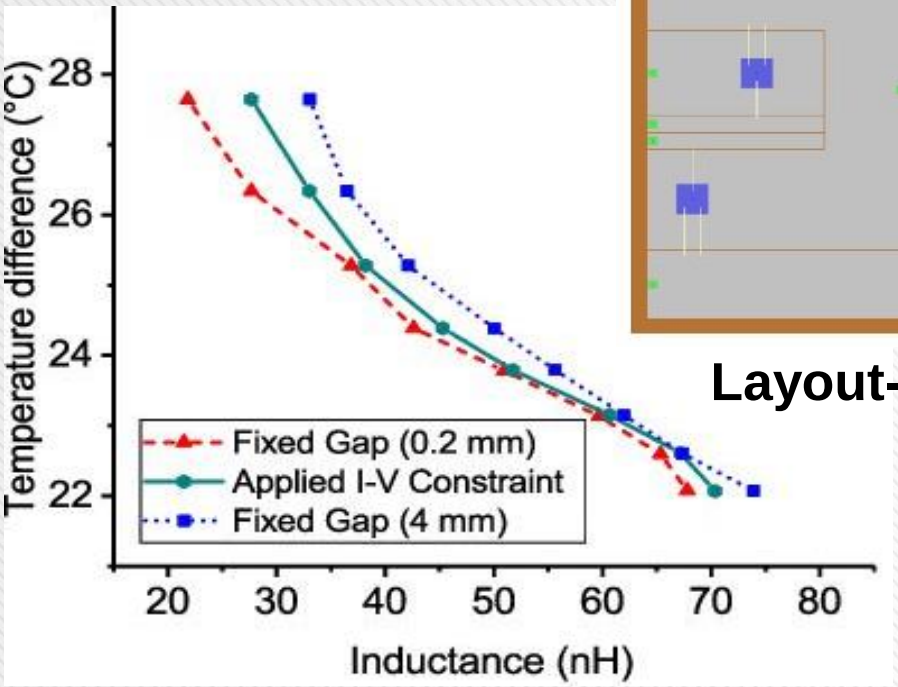


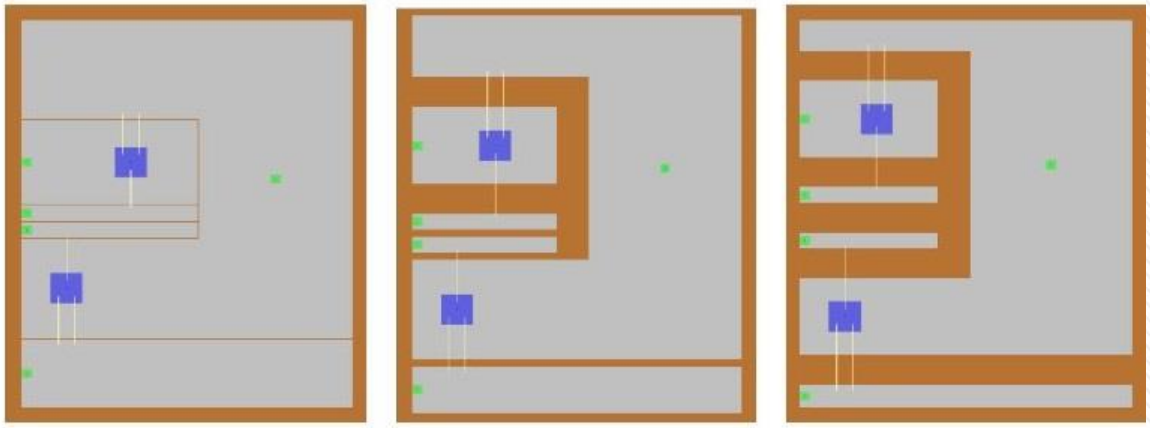
Case 3



Electrical and Thermal Optimization

- In each case, 1000 candidate solutions with varying floorplan sizes (2475 mm^2 to 9000 mm^2) are generated for optimization.
- Electrical and thermal models are used for evaluation.





Layout-1 Layout-2 Layout-3

Conclusions and Future Work

Conclusions:

- We have proved corner stitch and constraint graph methodology can be used in power module layout optimization.
- We have implemented both DRC and reliability constraint-aware layout generation in flat-level floorplan
- Flat level layout representation has coordinate-correlation issues that restricts the variation and flexibility.
- Hierarchical approach is potential solution.

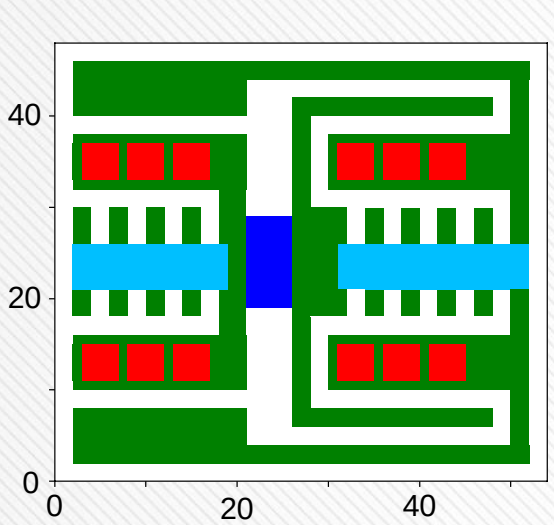
Future Work:

- Layout optimization using hierarchical approach
- 3D layout synthesis and optimization

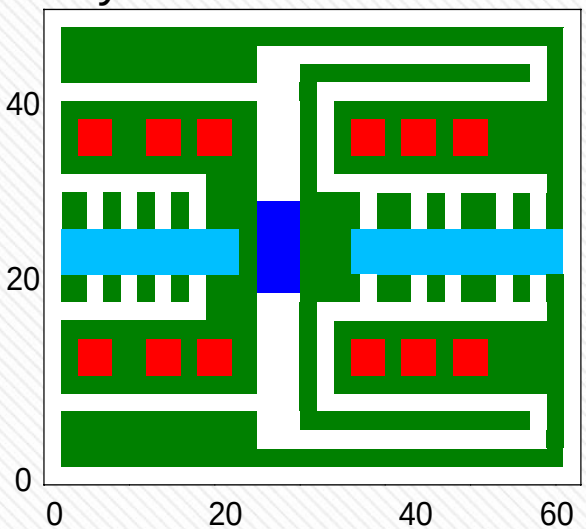
Benefits of Hierarchy

- To have more feasible layouts with larger variation due to less coordinate correlation among components.
- To reduce complexity in both modular and system level optimization using reusability feature
- A generic algorithm which can be extended to process 2.5D and 3D layouts.
- Initial result:

Minimum-sized layout



With hierarchy(54X48)



Flat level (63X52)