Die-to-Package Coupling Extraction for Fan-Out Wafer-Level-Packaging

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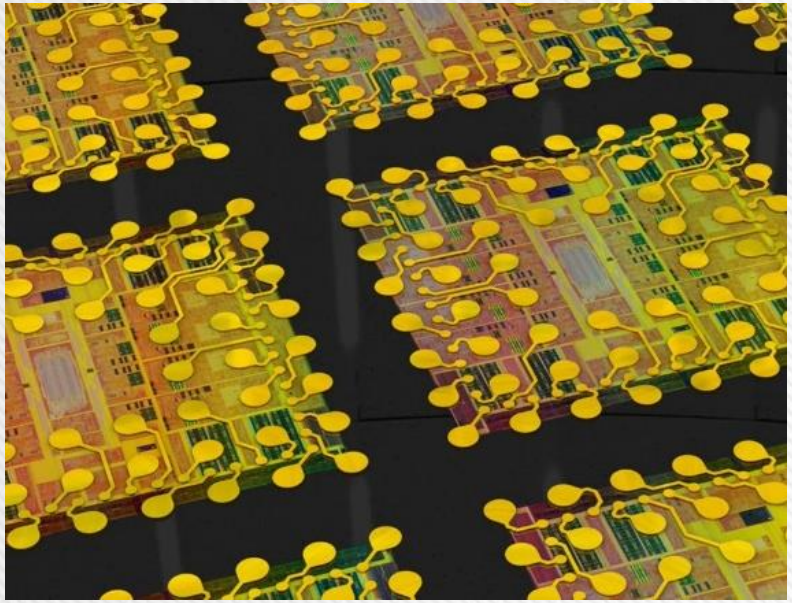
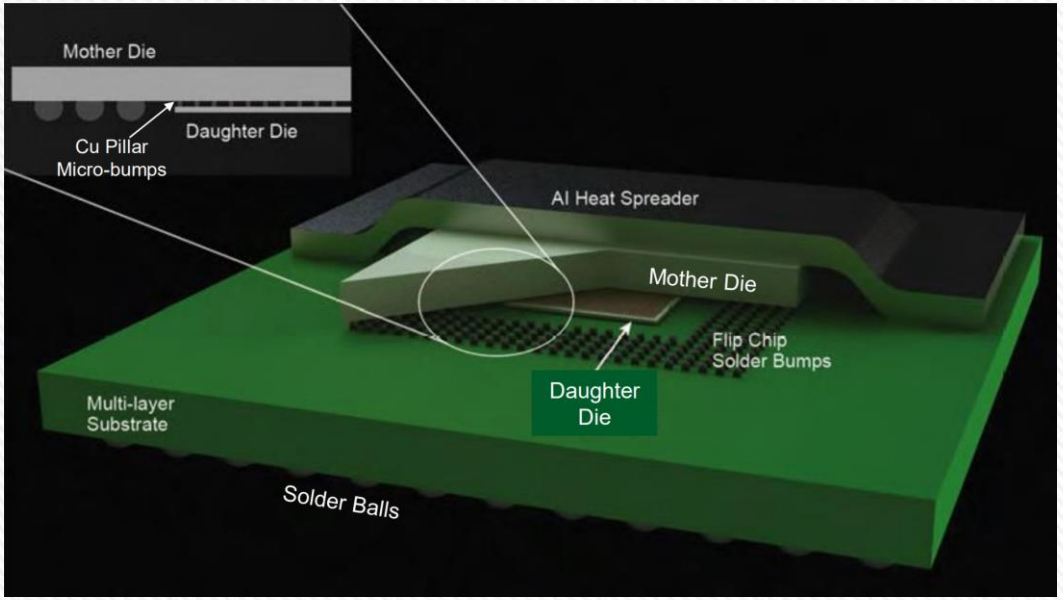
Introduction

- **Fan-out wafer-level-packaging (FOWLP)**
  - Low-cost multi-die solution with excellent thermal and RF properties
  - Allows multiple chip to be tightly integrated with package
  - New parasitics are introduced in the interface layers





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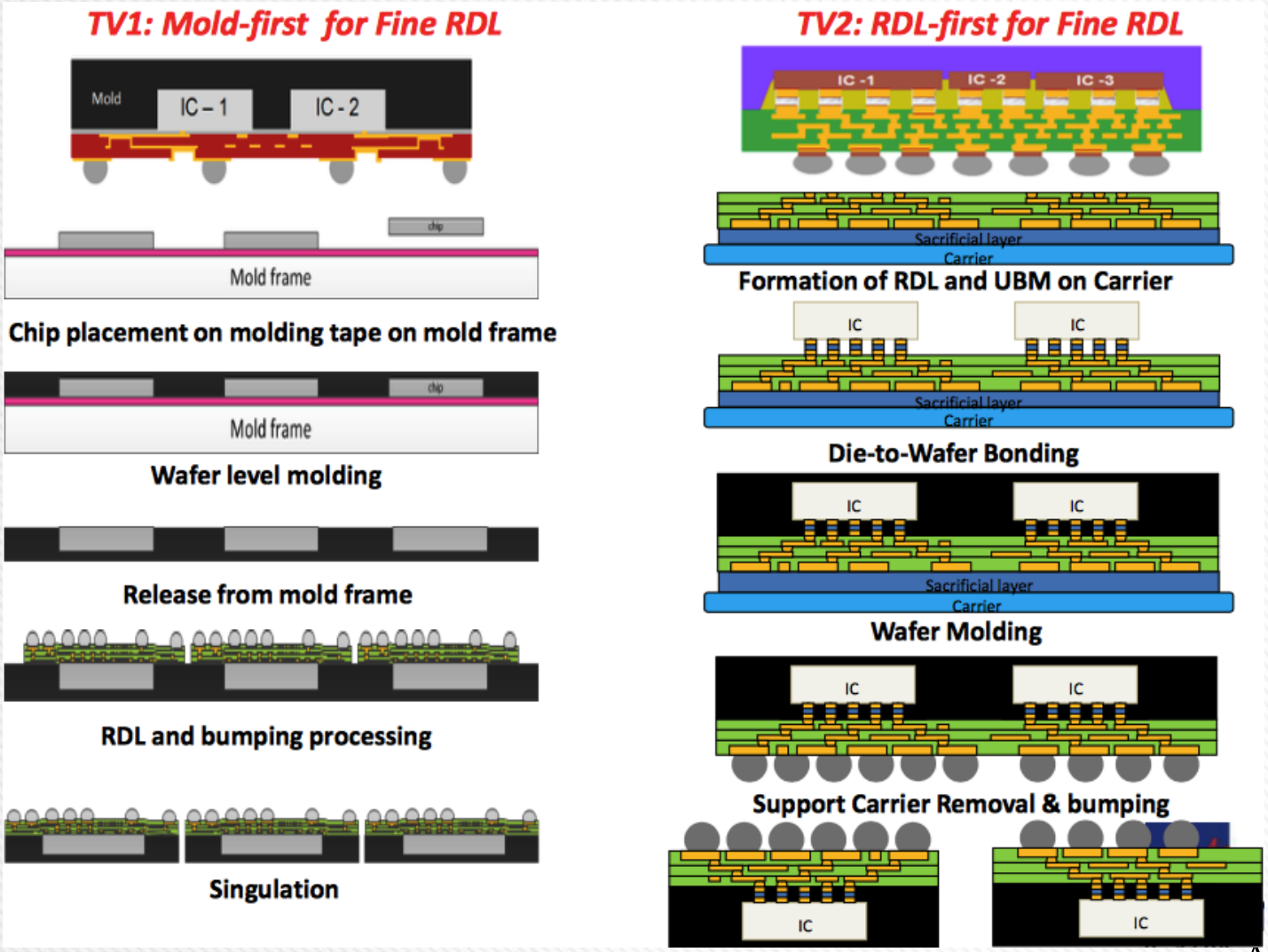
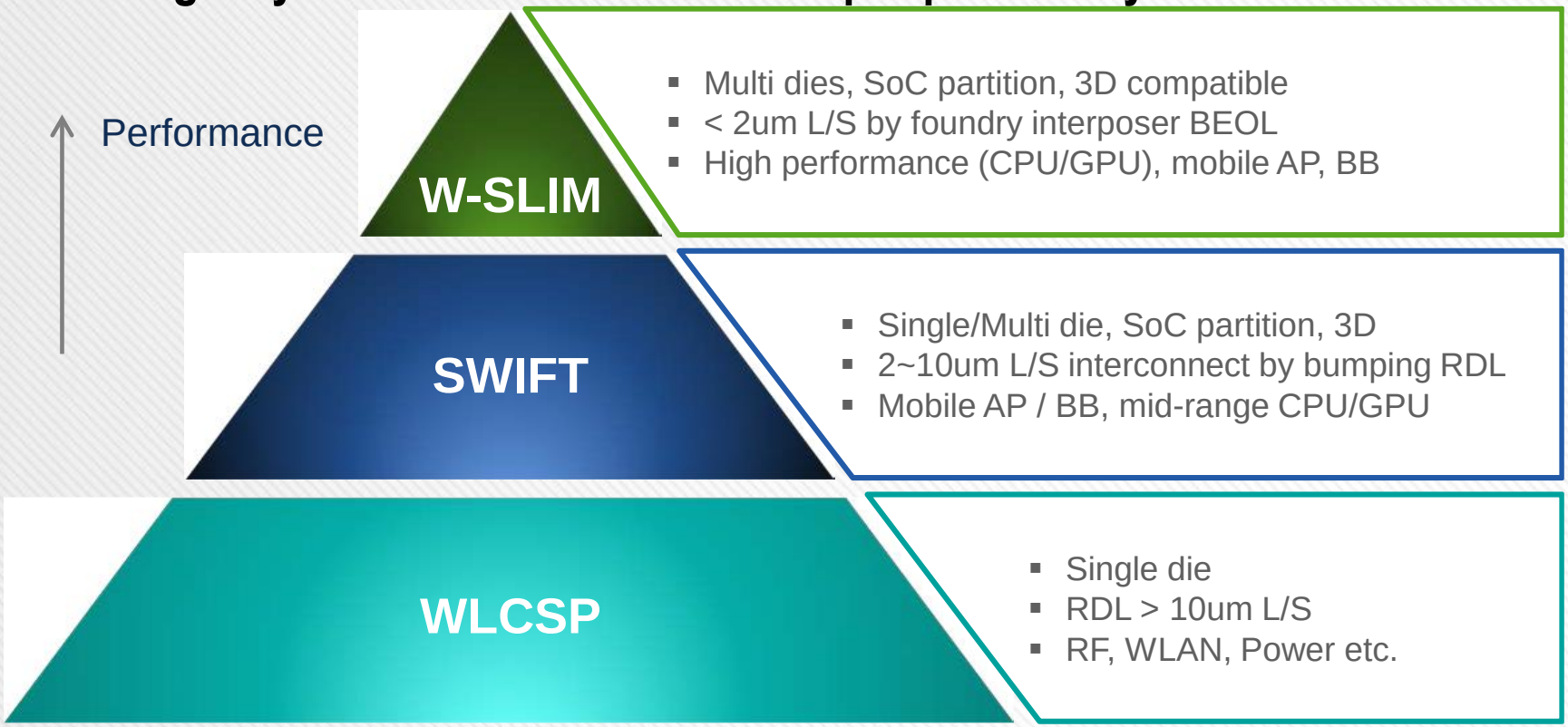
FOWLP Fabrication



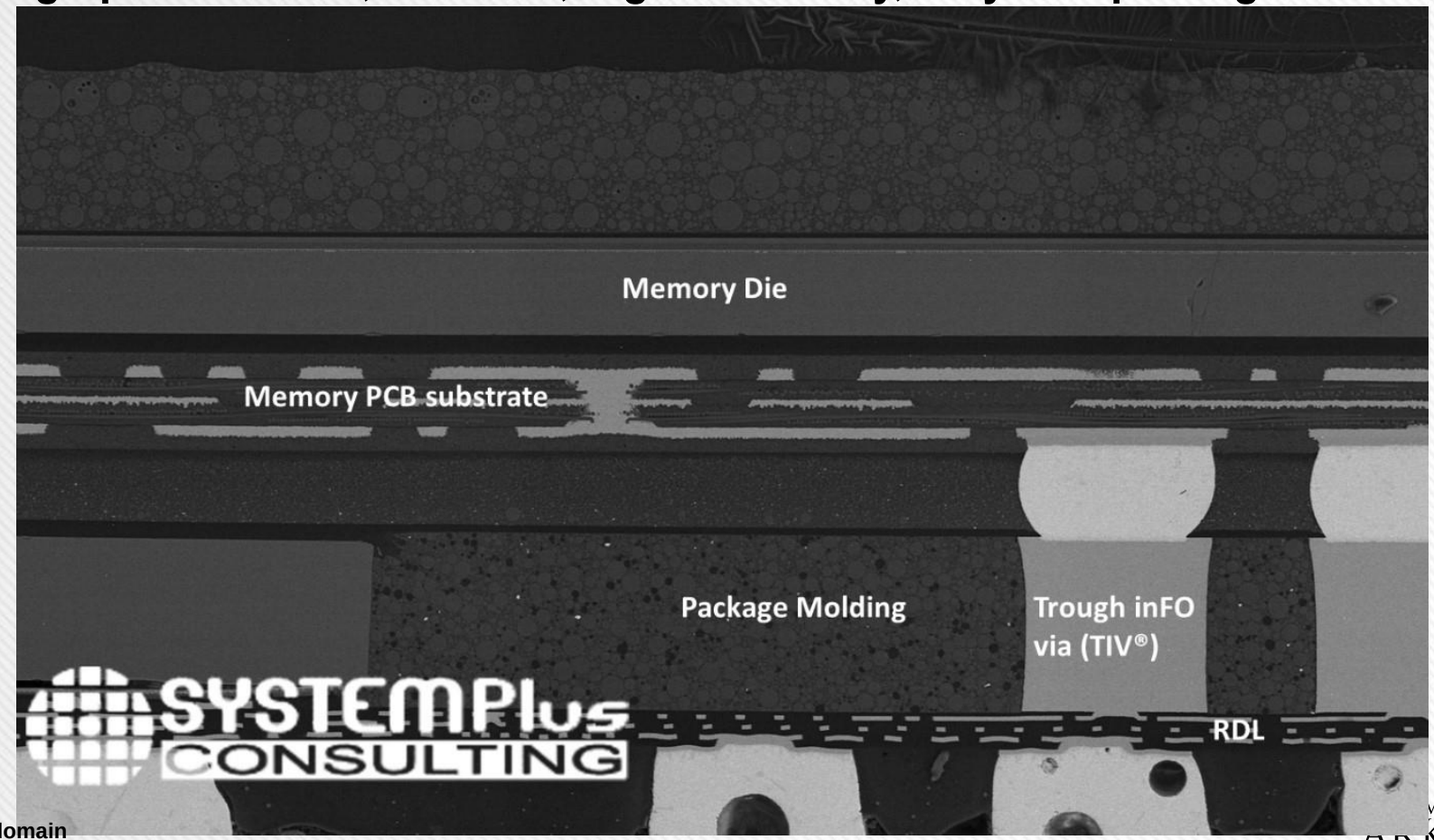
FOWLP Scales

- **Package chip dimension will keep scaling into 1um range using foundry BEOL process**
  - **Package layers becomes similar to chip top metal layers**



FOWLP is Here!

- **Apple A10, A11 processor in iPhones all used FOWLP**
  - **High performance, low cost, high IO density, very thin package**



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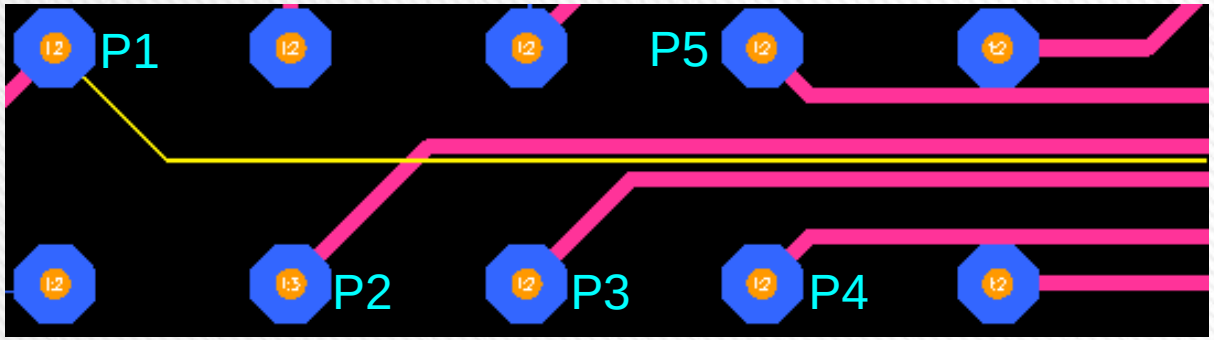
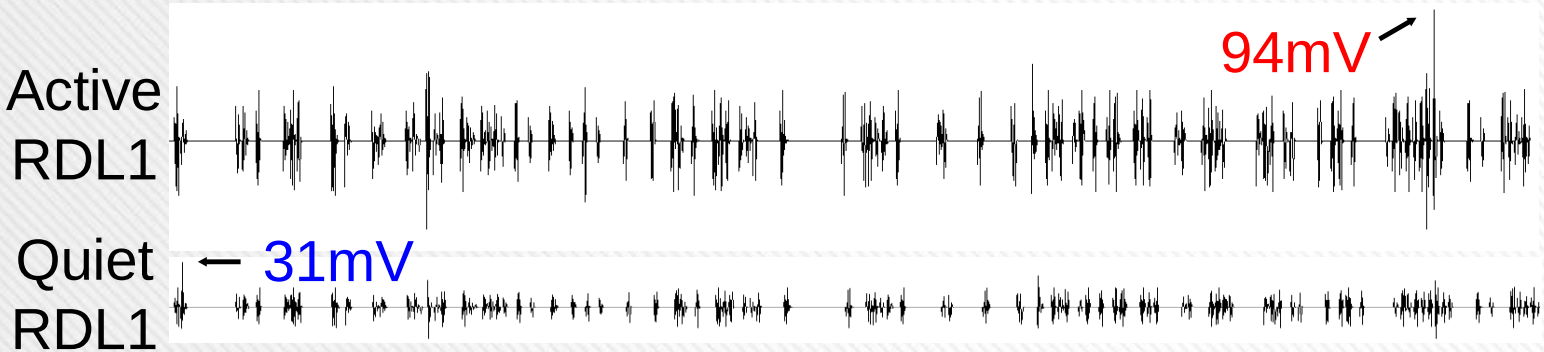
Motivation

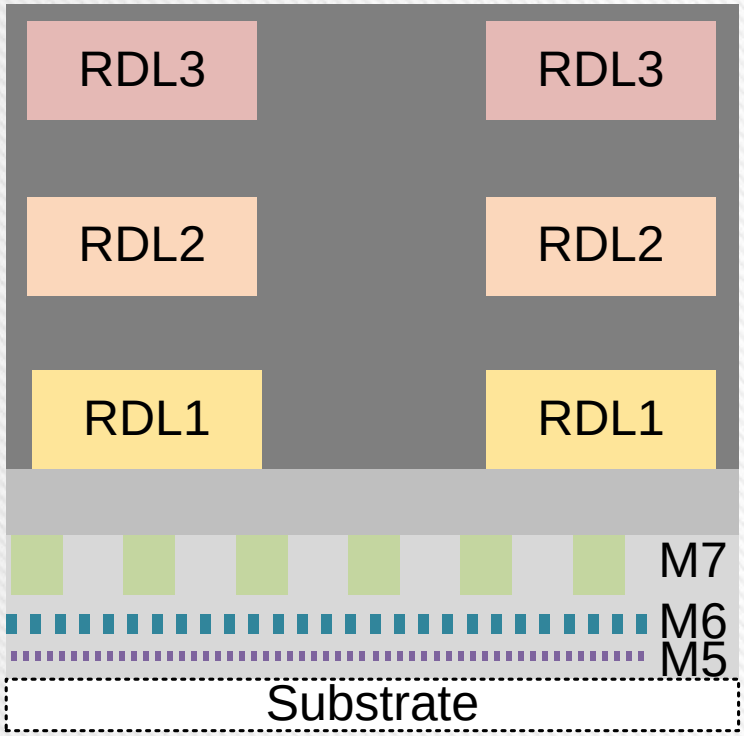
- **Pkg-to-die (P2D) coupling noises threaten signal integrity:**
  - **Significantly higher noise when both L and M elements are considered**
- **No parasitic extraction tool exists for P2D extraction**

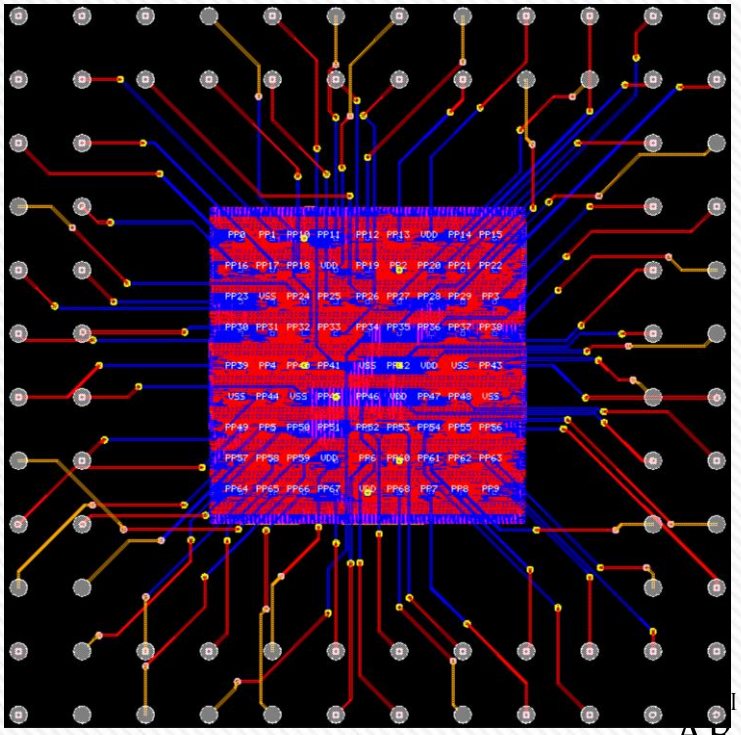




Our FOWLP Process Design Kit

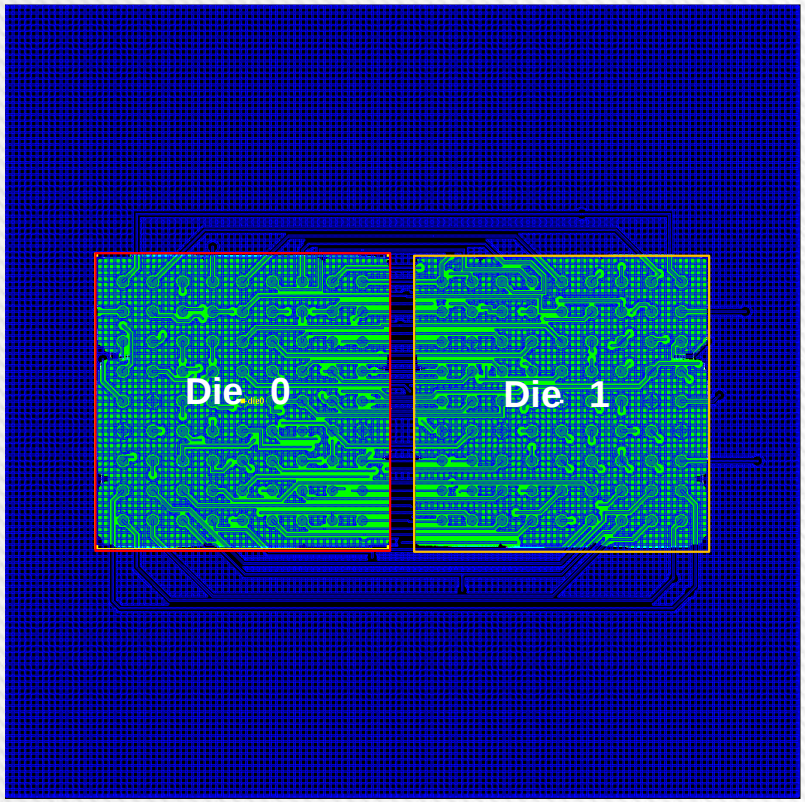
- **We designed a FOWLP PDK:**
  - **Chip: 45nm technology with seven metal layers**
  - **Package: 10/10/10μm W/S/T with 45° routing**
- **FFTx1 circuit contains 1.15 million cells in a 4mm square package**



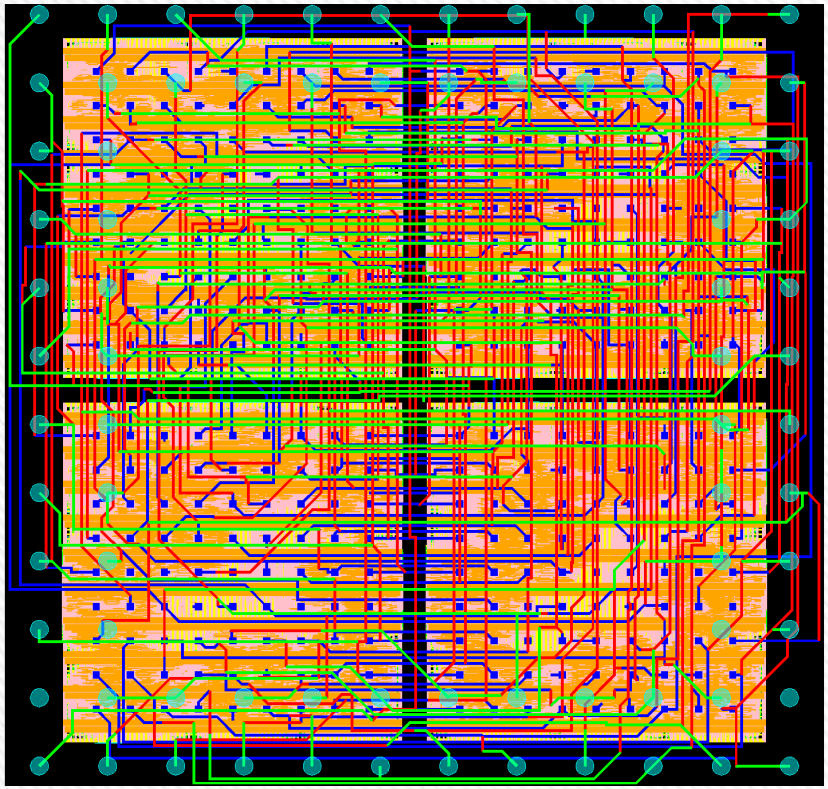


Our Benchmark 2D/2.5D Designs

- **Multi-chip 2.5D FFT256 Designs**
  - **Duplicated the base design to implement FFTx2 and FFTx4 2.5D designs**



FFTx2



FFTx4 (only signals)

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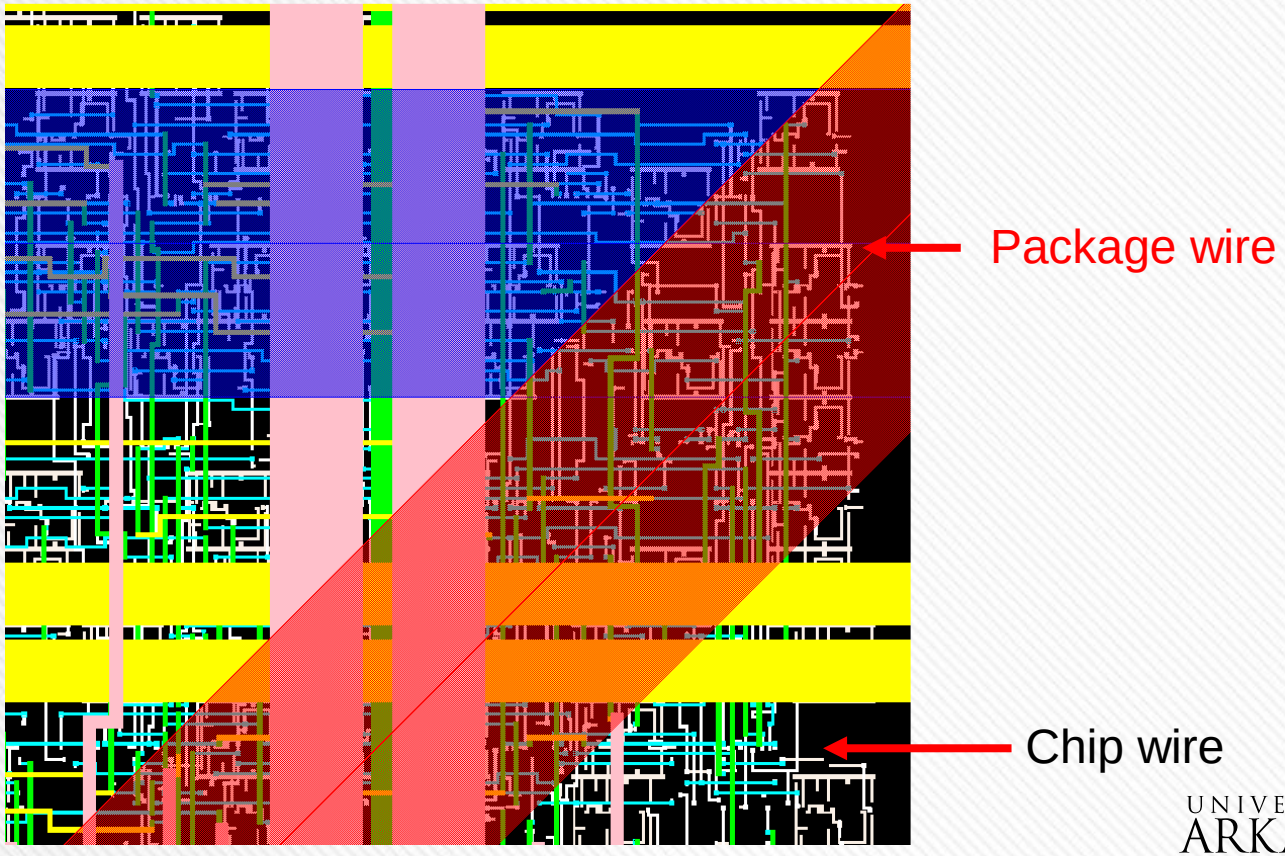
Our Benchmark 2D/2.5D Designs

- **Chip and package wires have significantly different dimensions**
  - **Difficult for general chip extraction tools to perform extraction efficiently**
  - **Irregular package routing increases extraction complexity**



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E-Field Shielding Impact

- **D2P coupling significantly increases with a closer D2P distance**

Top Layer	CCap (fF)	D2P distance (μm)			
		2	5	8	10
M7	M7-R1	15.06	7.155	4.746	3.880
	M6-R1	0.005	0.002	0.002	0.002
M6	M6-R1	4.330	3.319	2.691	2.388

- **E-field Shielding from RDL also affects D2P coupling**
  - **Using one RDL layer is good enough because of ground planes**

Total RDL#	1 RDL	2 RDL	3 RDL
M7-R1	7.155	6.960	6.953
M7-R2	-	0.201	0.195
M7-R3	-	-	0.005

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Ground Plane is NOT Enough

- **What if we model the chip as a ground plane?**
  - Compatible with most package tools (Allegro, Xpedition)
- **With only ground plane, D2P coupling is significantly overestimated**
  - Also, only lumped capacitance can be extracted

	CCap	Mtop	Via	rdl1	rdl2	rdl3
GND plane	Mtop	0	0	4.669	0.011	0.000
	RDL1	4.669	0	0.782	41.44	0.145
Real die	Mtop	60.92	2.793	1.019	0.075	0.055
	RDL1	1.019	0.006	0.710	42.65	0.056

Ccap(pF)	Mtop-Mtop	Mtop-Via	Mtop-R1	R1-R1
Real die	60.92	2.793	1.019	0.71
Ground plane	0	0	4.669	0.782
Err%	-100%	-100%	358%	10.2%

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Holistic Extraction

- **Traditionally, chip and package routings are extracted separately**
  - **D2P coupling is ignored completely**
- **Holistic extraction takes all metal layers from both chip and package into consideration**
  - **First, create a new metal stack configuration that includes all seven chip layers and three package layers.**
  - **Then, design a holistic die-package layout by merging the geometries from the die and the package.**
  - **Finally, run Calibre xACT on the holistic design to obtain all capacitance information**

Holistic Extraction Results

- **D2P coupling capacitance extraction using holistic extraction**
  - **Our GDS-level CAD tools can be used for complete D2P RCLM extraction**

Layer	M1	M2	M3	M4	M5	M6	M7	rdl1	rdl2	rdl3
Gcap	45856	24607	10502	6891.8	8429	2486.6	2316.7	17389	898.31	2833.8
Ccap	M1	M2	M3	M4	M5	M6	M7	rdl1	rdl2	rdl3
M1	19093	21827	10267	1785	60	2.22	0.02	0.07	0	0
M2	21827	27895	53198	17424	377	20.68	0.24	3.85	8.55	5.23
M3	10267	53198	28434	88343	5005	185	0.87	3.31	4.4	3.23
M4	1785	17424	88343	33021	56288	5337	359	12.13	8.23	4.57
M5	60.23	377	5005	56288	18016	51222	375	31.08	12.46	6.96
M6	2.22	20.68	185	5337	51222	18708	16623	354	410	2.71
M7	0.02	0.24	0.87	359	375	16623	257	2519	47.05	0.23
rdl1	0.07	3.85	3.31	12.13	31.08	354	2519	134	31207	11.57
rdl2	0	8.55	4.4	8.23	12.46	410	47.05	31207	461	46256
rdl3	0	5.23	3.23	4.57	6.96	2.71	0.23	11.57	46256	231
Ccap	53034	120759	185443	202582	131393	92865	20182	34277	78415	46522

Cap unit in fF

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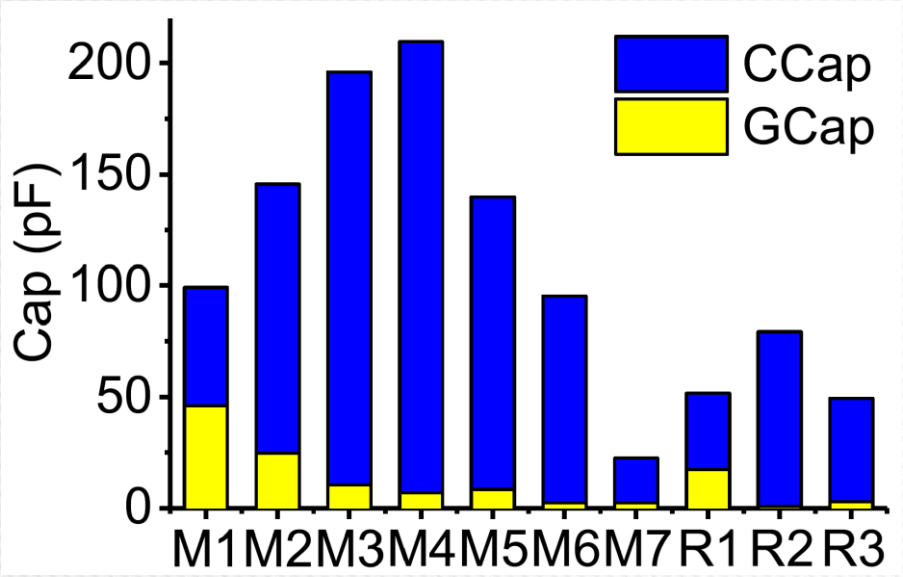
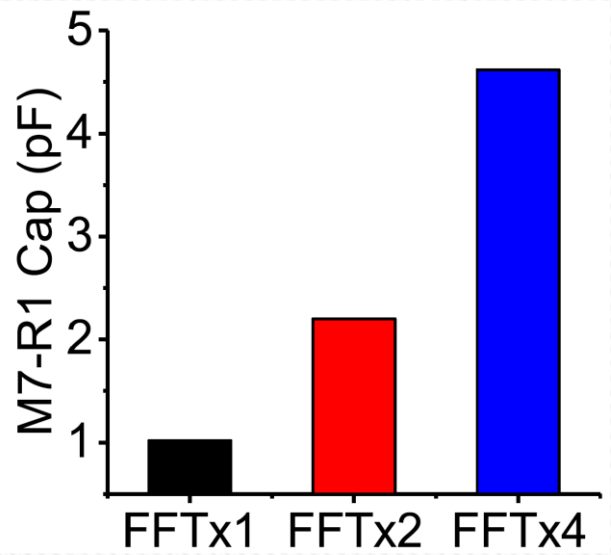
Coupling Cap Distribution

- Holistic extraction clearly captures all D2P coupling components
- With larger D2P overlapping area, D2P coupling increases significantly





Problem?

- **Holistic extraction is highly accurate but computationally expensive**
  - it contains all layers from both the die and the package
  - complicated structures on the package layers: hatch ground planes, pads, vias, 45° routing, circular shape routing
  - requires in a significant increase in both runtime and memory
- **For example**
  - two 10nm chip with 12 metal layers
  - a three-layer package (20mm-by-20mm)
  - 32-node (4 cores/node) computing grid
  - more than 700GB of DRAM space
  - more than three days

In-Context Extraction

- **In-Context Extraction reduces both computational time and memory**
  - In-Context extraction takes each chip separately
  - with a few interface layers from the neighboring component
- **With the same example,**
  - less than 150GB memory
  - less than 1.5 days
- **Reuse most of the existing 2D LVS rule decks**
  - Only some minor extensions are necessary for interface layers
- **Eliminates the need for sharing intellectual properties across different design houses**
  - Greatly simplifies the extraction procedure with heterogeneous designs

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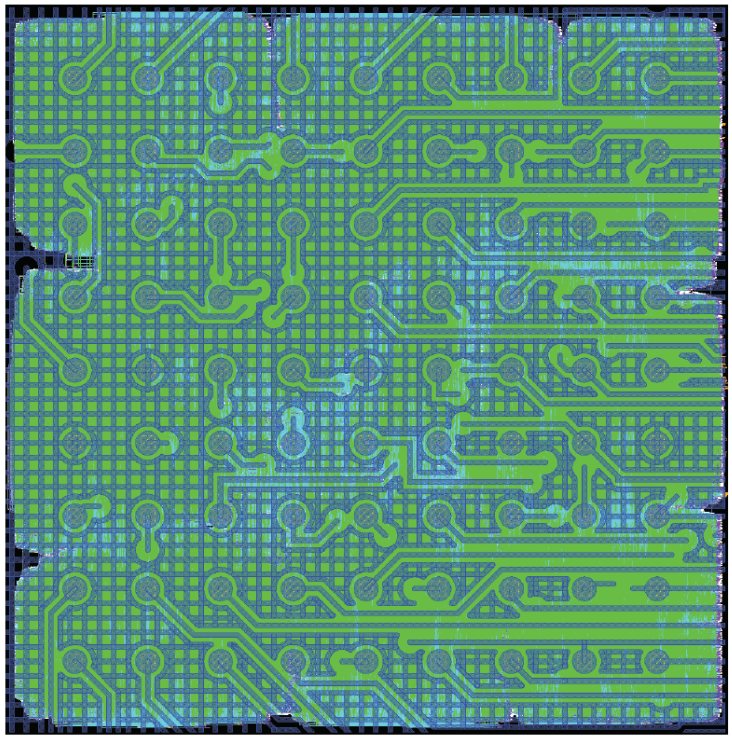
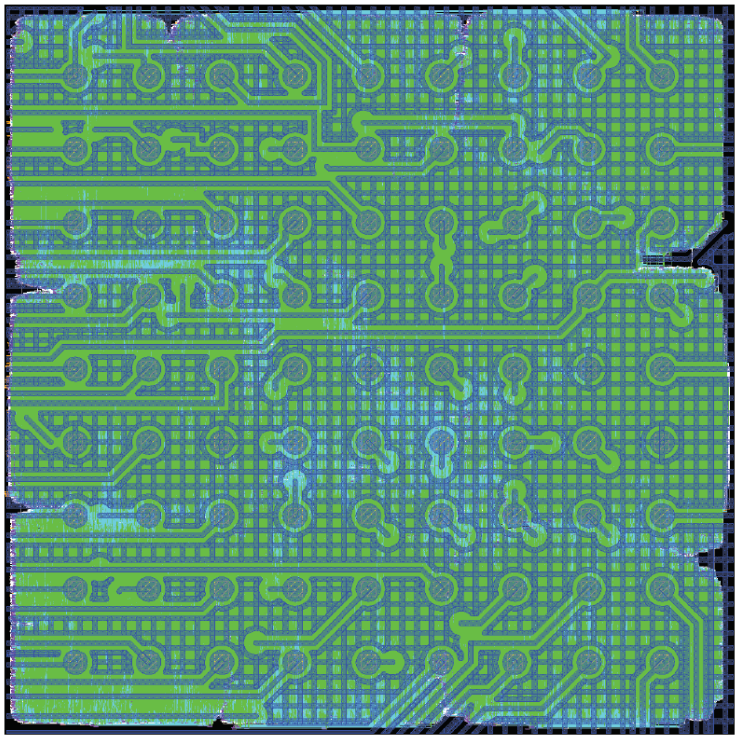
In-Context Design

- **Using one RDL layer and cut each chip with D2P overlapping region**
  - **Preserves all D2P coupling and the compatibility with chip tools**



die0



die1

In-Context Extraction Results

- **In-context extraction still captures all D2P coupling elements and is highly accurate compared with holistic extraction**
  - **R1 coupling is smaller because of Fan Out region is not included**

Method	Die0 + Die1 In-Context			Die0&Die1 Holistic		
Layer	M7	Via	R1	M7	Via	R1
GCap	29.87	3.529	5.726	29.78	3.454	28.124
CCap	M7	Via	R1	M7	Via	R1
M7	121.8	6.061	2.202	121.9	5.612	2.187
Via	6.061	0.000	0.000	5.612	0.000	0.000
R1	2.202	0.000	1.281	2.187	0.000	2.143

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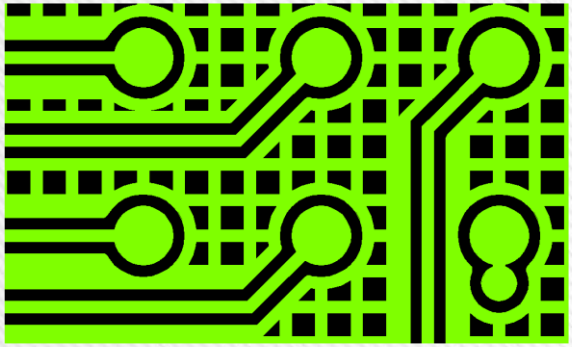
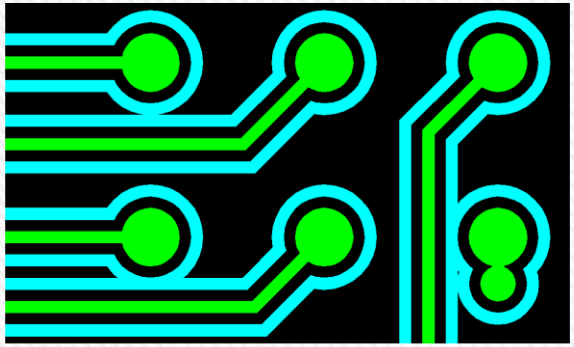
What about Inductance?

- **Halo-Ground Approximation**

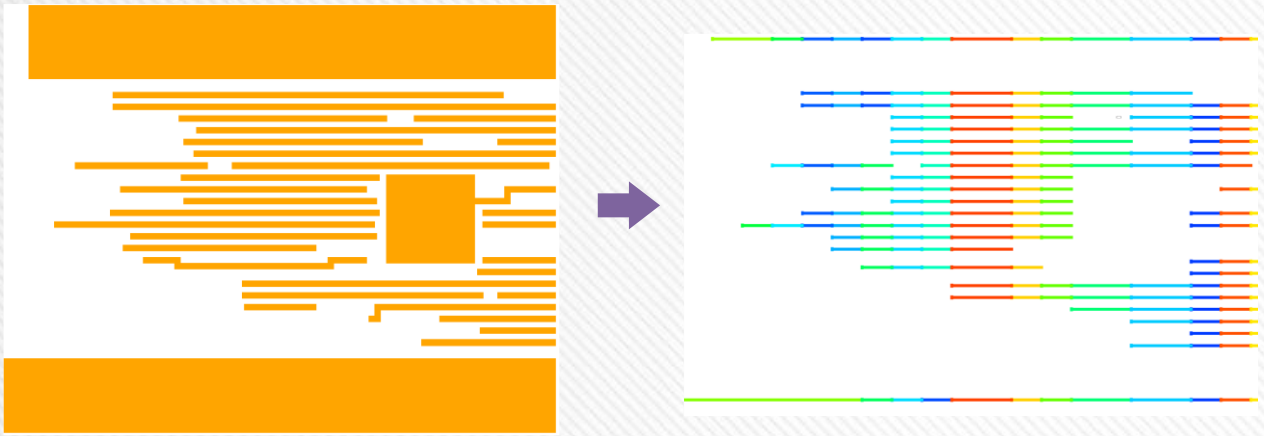


(a) Original layout



(b) Halo ground layout

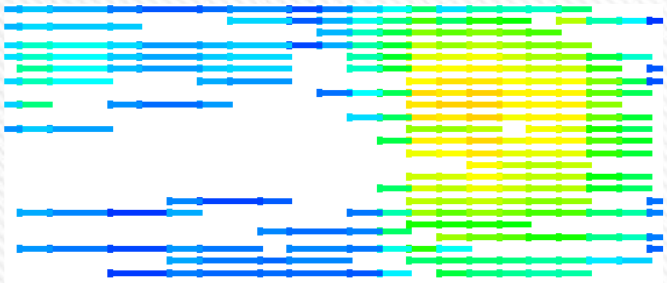
- **Bundle Creation**



[Yarui Peng](), Dusan Petranovic and Sung Kyu Lim, "Chip/Package Co-Analysis and Inductance Extraction for Fan-Out Wafer-Level-Packaging", *EPEPS, 201*

Package-to-Chip RLM Estimation

- **Less than 3s to compute more than 1000 package and chip wires**
  - **Accuracy verified against Fast Henry.**



	Fast Henry			Our method					
#	R	TotL	TotM	R	ERR%	TotL	ERR%	TotM	ERR%
1	0.52	34.3	94.8	0.52	-0.7%	35.3	2.8%	89.8	-5.3%
2	0.52	34.5	109.2	0.52	-0.6%	35.5	2.9%	104.6	-4.3%
3	0.42	27.5	106.3	0.41	-1.3%	26.8	-2.6%	96.4	-9.4%
4	0.52	34.8	121.1	0.51	-0.6%	35.8	3.0%	116.5	-3.8%
5	0.52	34.8	120.9	0.51	-0.6%	35.9	3.0%	116.3	-3.8%

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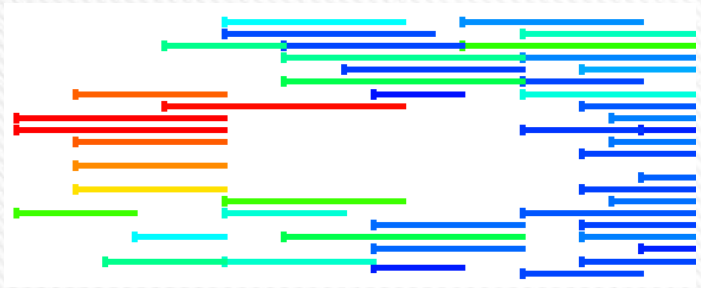
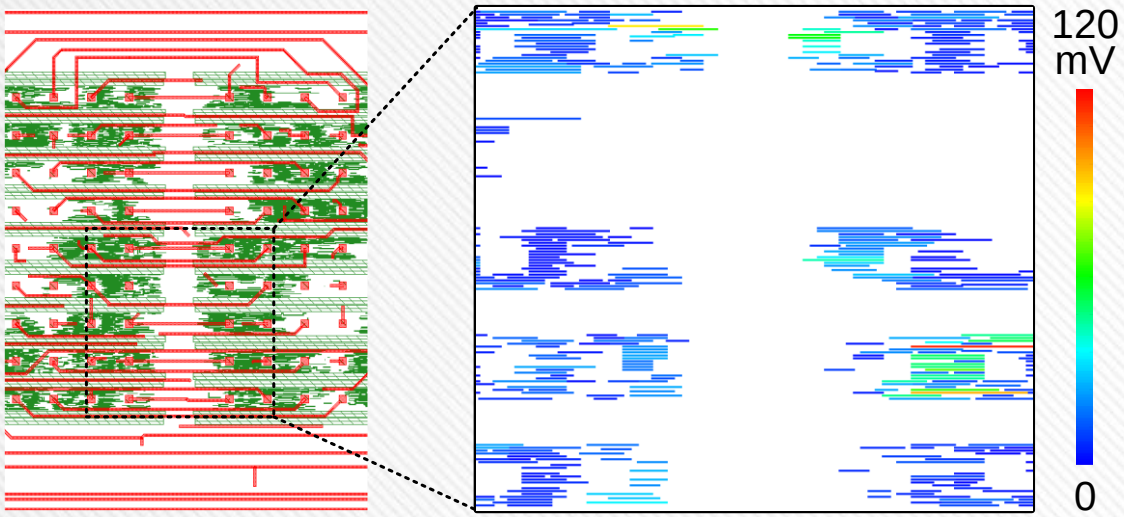
Package-to-Chip Noise Estimation

- **Our tool identifies any noise hot-spot on chip and provides fast estimation of package-induced signal integrity issues**

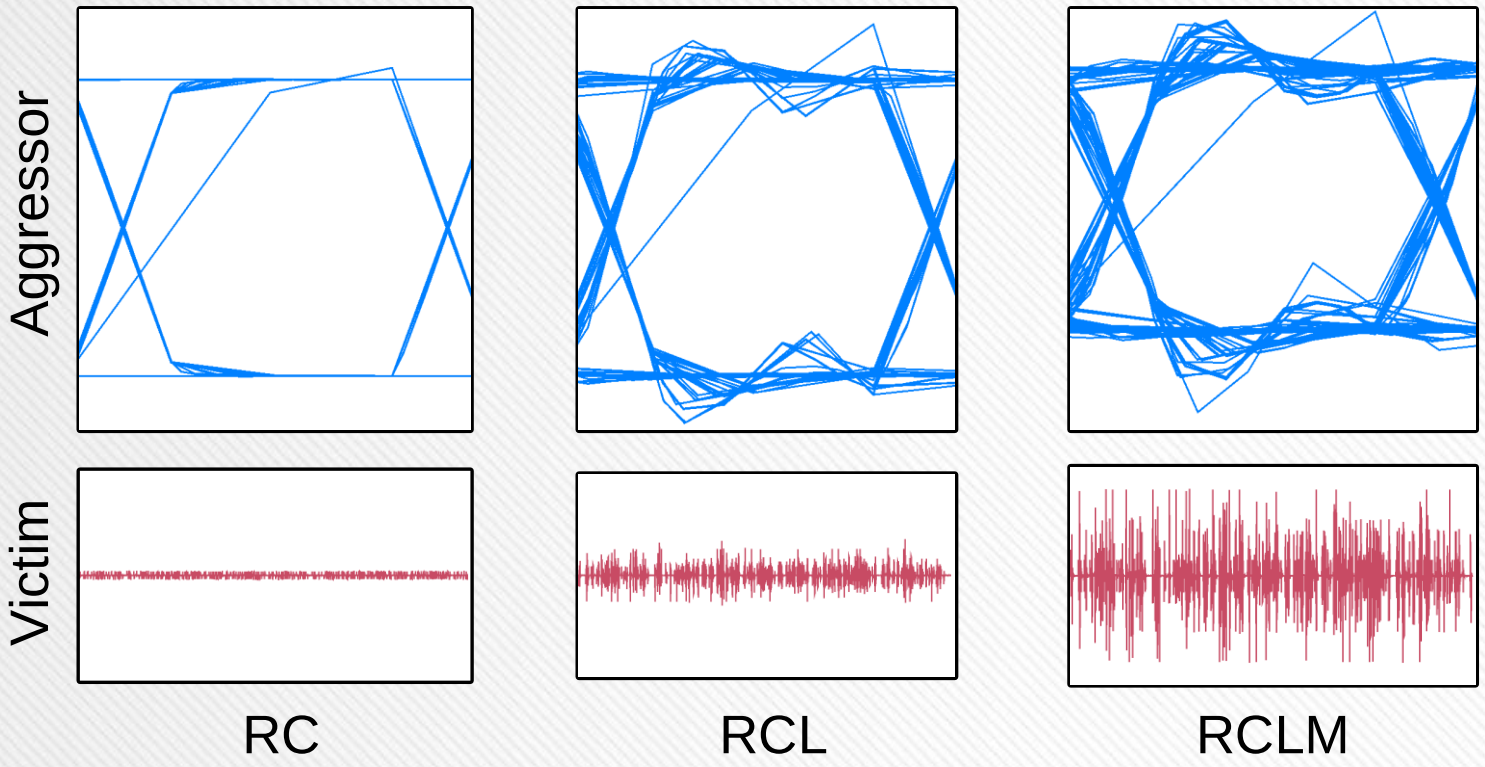




(a) Original interface (b) Estimated on-chip noise

Noise Analysis

- **P2D inductive coupling noises are dominating**
  - **RCLM netlist is required for accurate noise estimation**



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Conclusion

- D2P coupling is heavily affected by E-field Shielding. Using ground plane approximation is not accurate enough for FOWLP
- We propose holistic extraction with all metal layers and full geometries and demonstrate its maximum accuracy with high runtime and memory cost.
- We propose in-context extraction flows for reduced computational expenses and simplified flows for heterogeneous designs. In-context extraction is still highly accurate to capture D2P coupling.
- A comprehensive coupling extraction with RCLM netlist is needed for chip-package co-design, co-analysis, and co-optimization.