Chip/Package Co-Analysis and Inductance Extraction for Fan-Out Wafer-Level-Packaging

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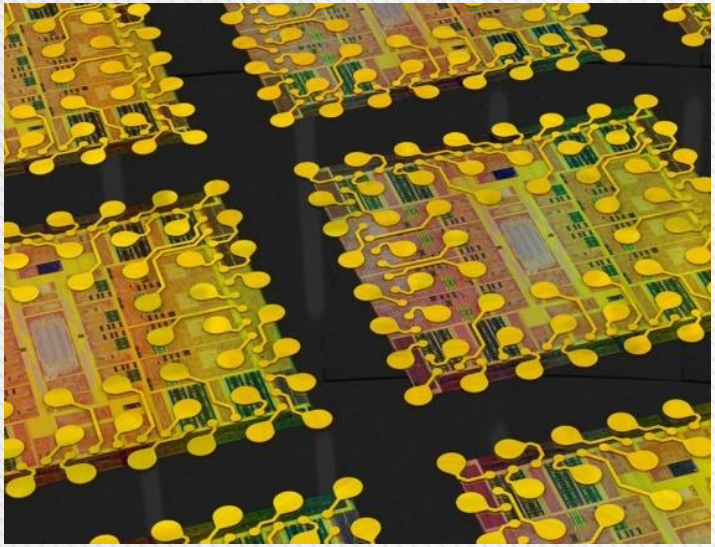
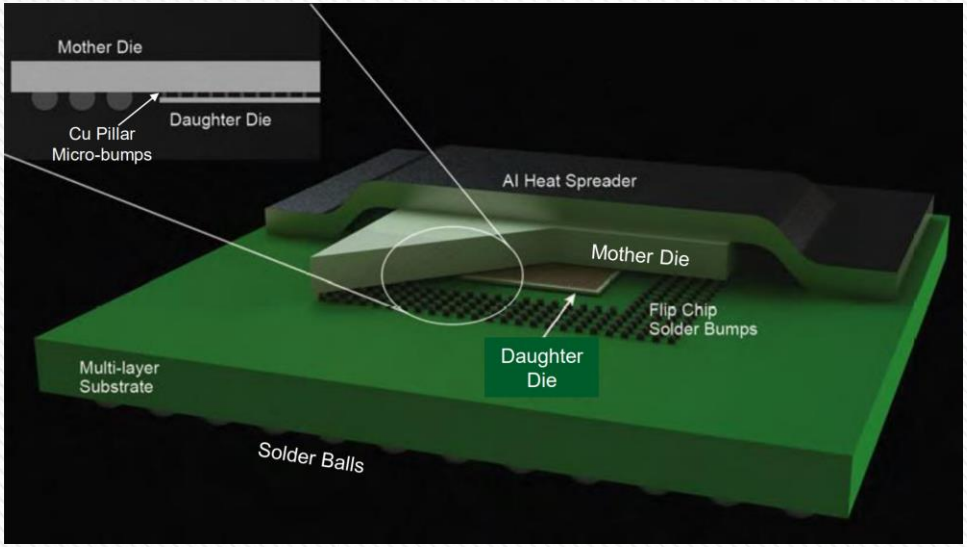
Introduction

- **Fan-out wafer-level-packaging (FOWLP)**
  - Low-cost multi-die solution with excellent thermal and RF properties
  - Allows multiple chip to be tightly integrated with package
  - New parasitics are introduced in the interface layers





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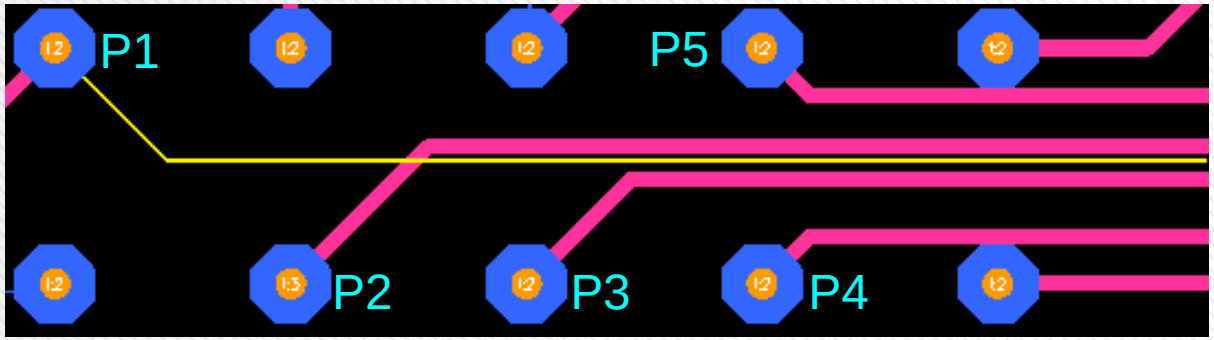
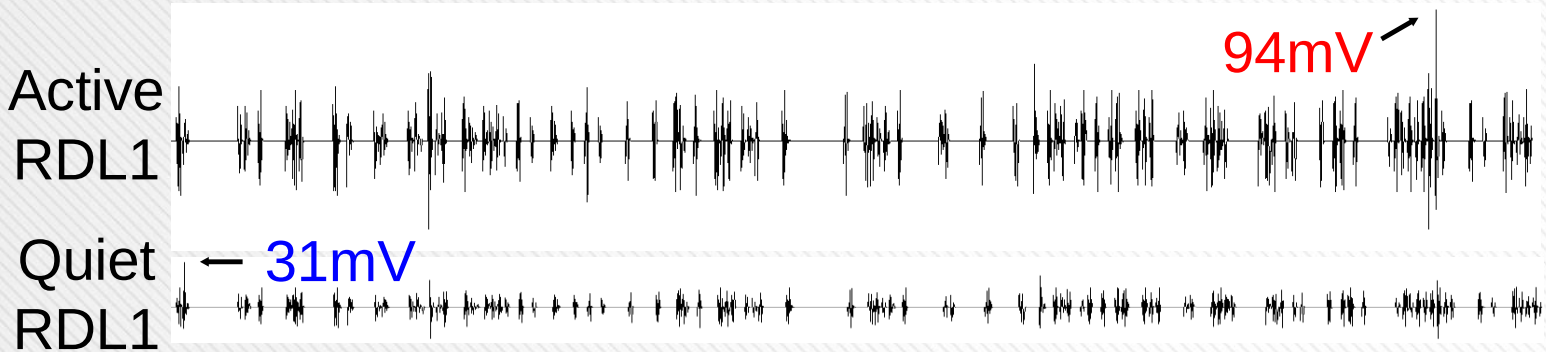
Motivation

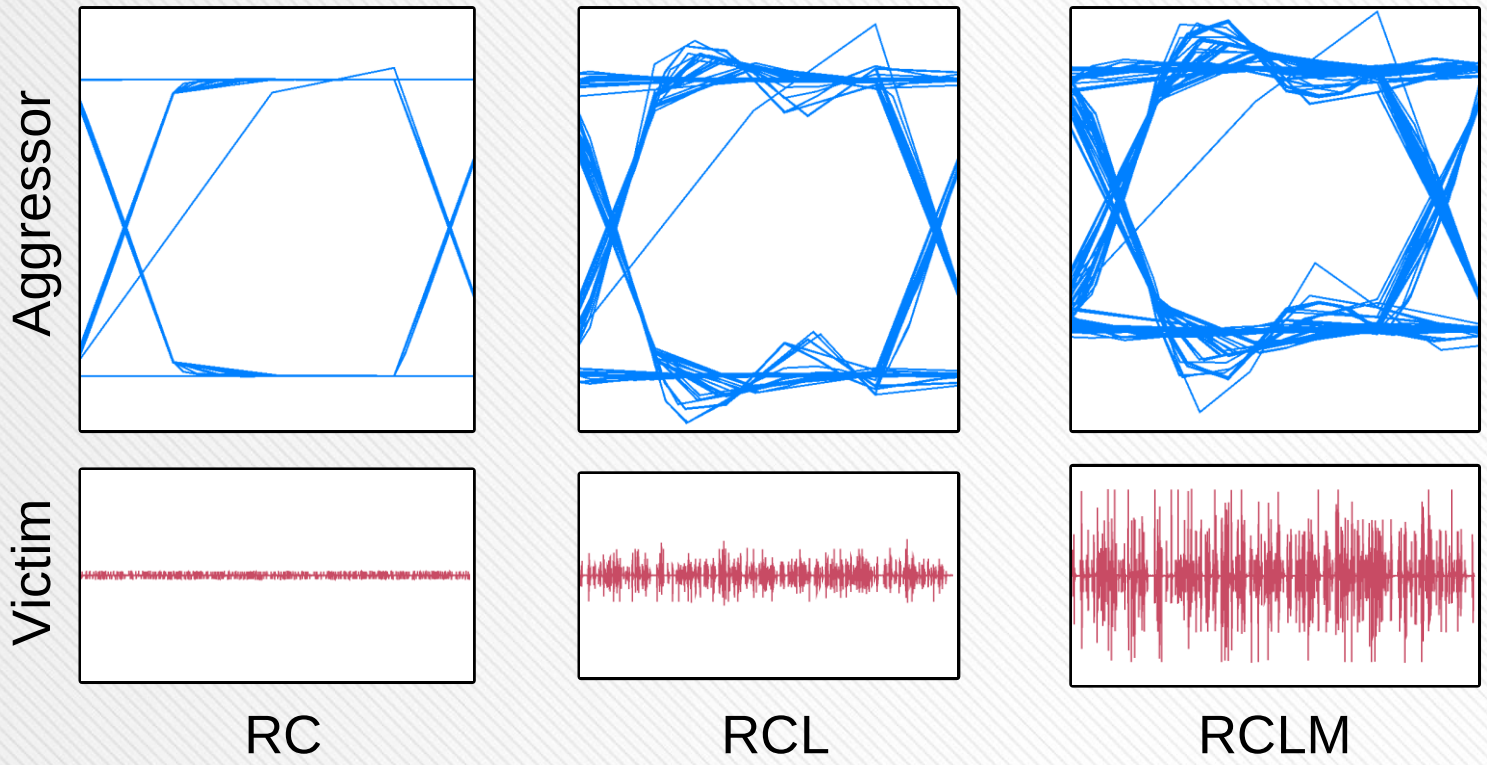
- **Pkg-to-die (P2D) coupling noises threaten signal integrity:**
  - **Significantly higher noise when both L and M elements are considered**
- **No parasitic extraction tool exists for P2D extraction**





Noise Analysis

- **P2D inductive coupling noises are dominating**
  - **RCLM netlist is required for accurate noise estimation**



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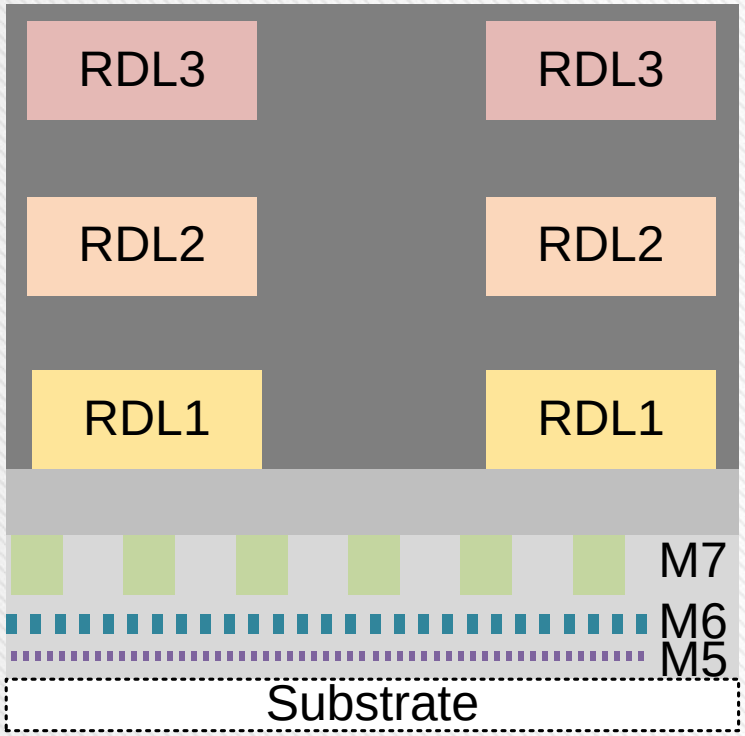
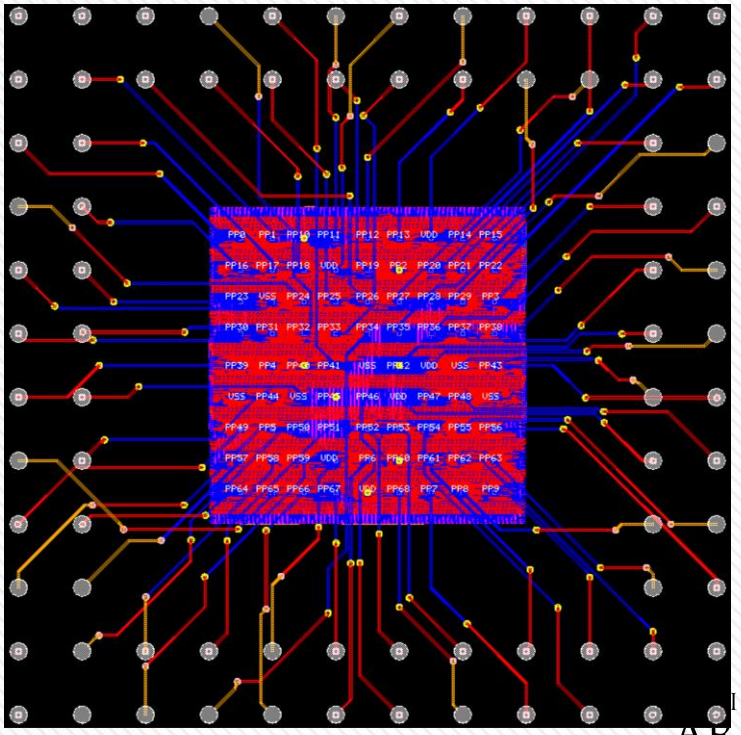
Our FOWLP Process Design Kit

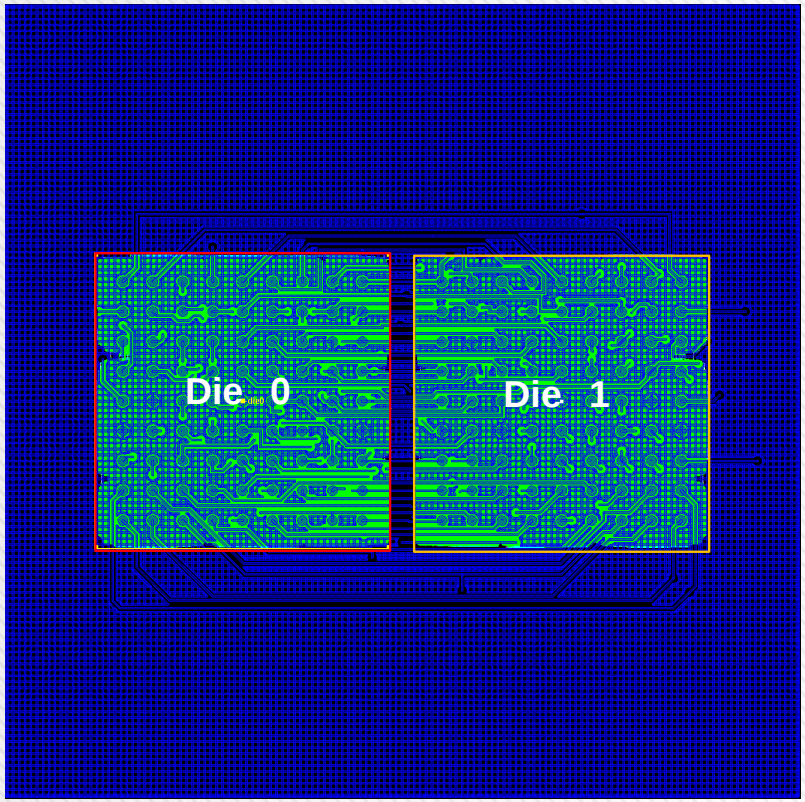
- **We designed a FOWLP PDK:**
  - Chip: 45nm technology with seven metal layers
  - Package: 10/10/10μm W/S/T with 45° routing
- **FFTx1 circuit contains 1.15 million cells in a 4mm square package**



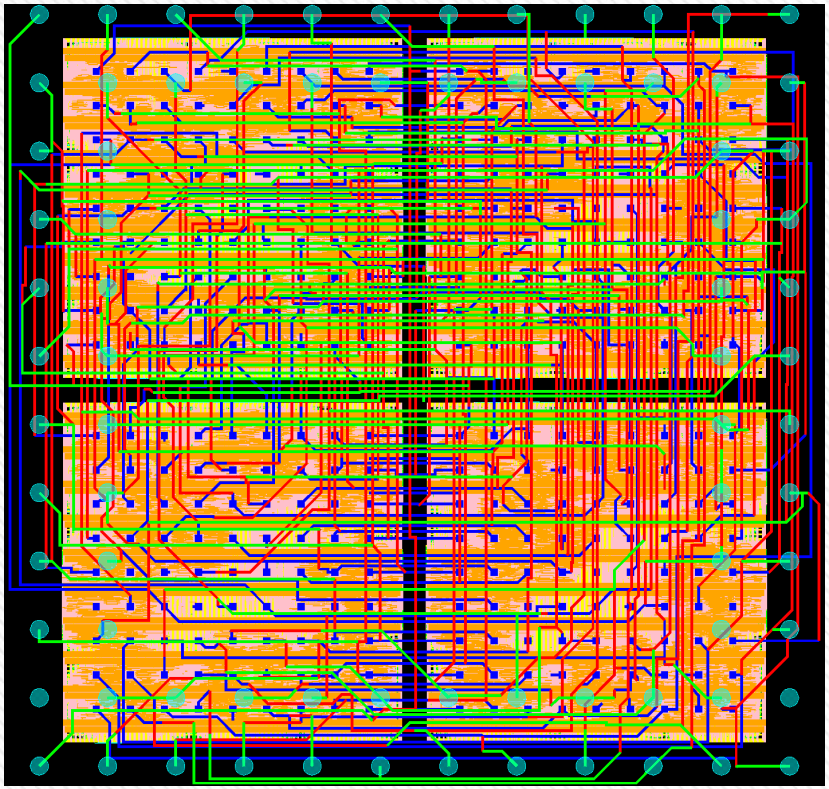


Our Benchmark 2D/2.5D Designs

- **Multi-chip 2.5D FFT256 Designs**
  - **Duplicated the base design to implement FFTx2 and FFTx4 2.5D designs**



FFTx2



FFTx4

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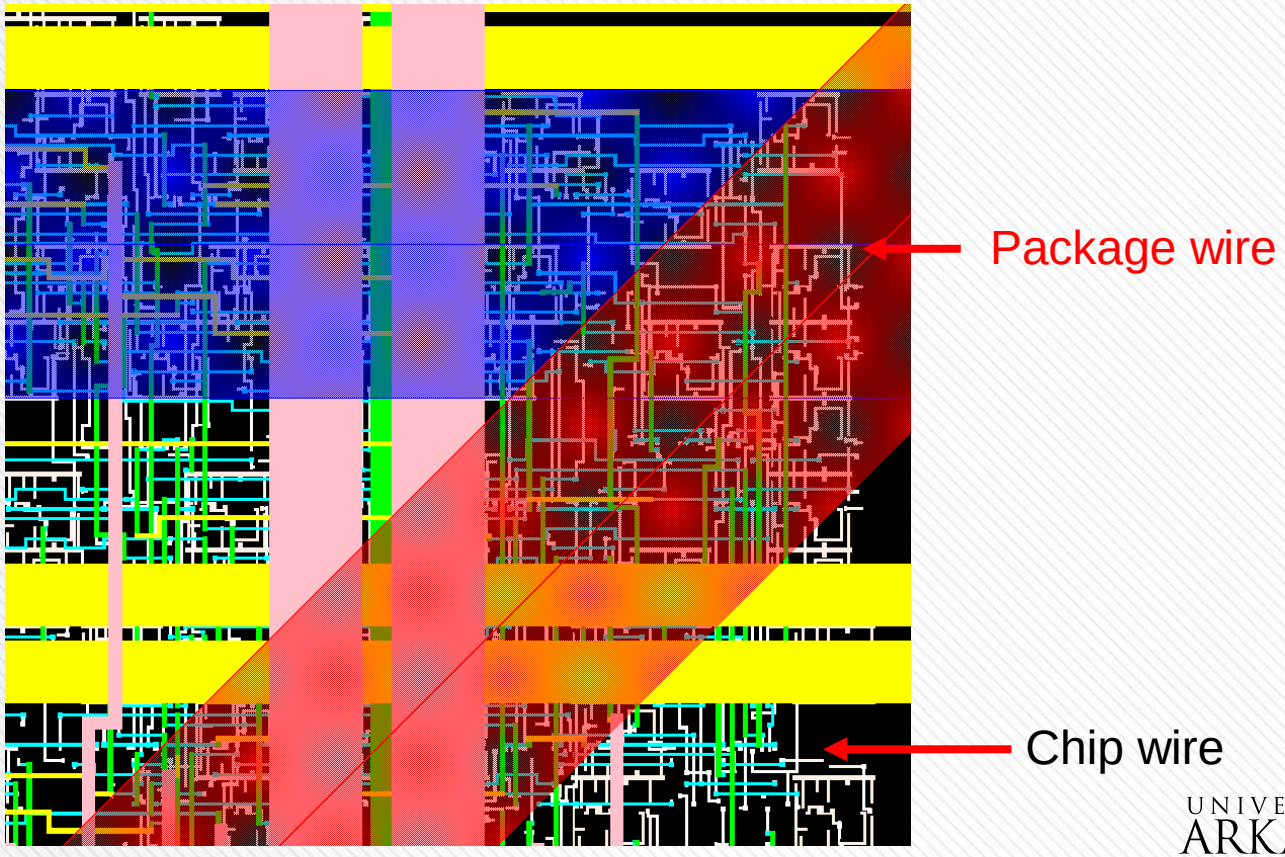
Our Benchmark 2D/2.5D Designs

- **Chip and package wires have significantly different dimensions**
  - **Difficult for general chip inductance tools to perform extraction efficiently**
  - **Full-wave solver are unable to extract chip wires**



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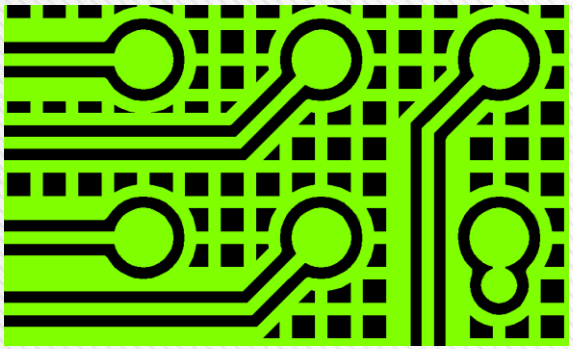
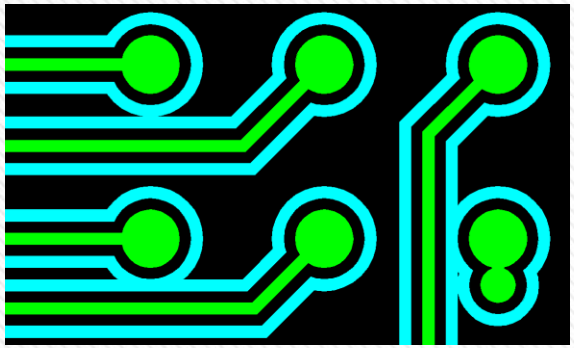
Halo-Ground Approximation

- **How to handle ground planes?**
  - It is challenging to perform extraction with large ground planes on the package layer, especially with hatched mesh ground plane
  - Most of the current are limited within areas close to the neighboring routing, because of the skin effects and proximity effects
  - Our approach: approximate the ground plane using 'halo-ground' around the signal traces.
  - It is effective in most of the frequency range higher than 1GHz, where inductance impact matters



(a) Original layout



(b) Halo ground layout

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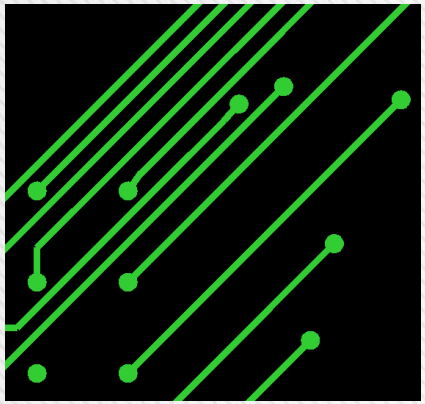
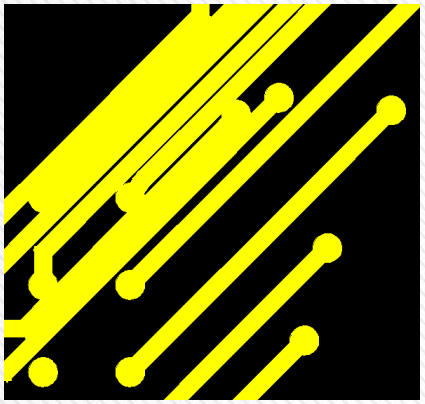
Layer Operations

- CAD flows to produce Halo-Ground layout using layer operations

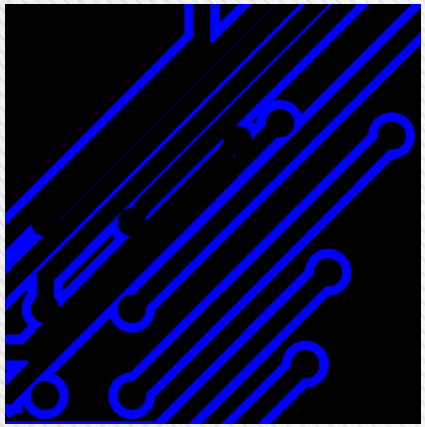


L1: Original

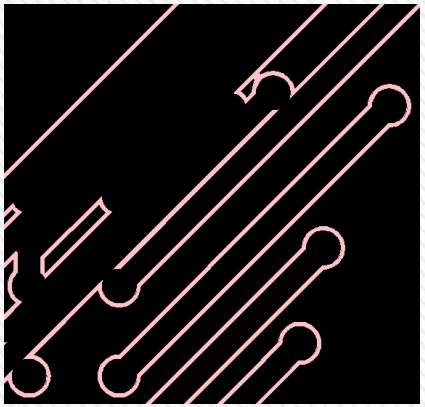


L2: L1 Expand by S

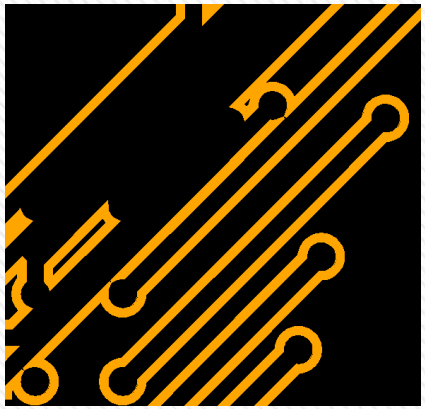
L3: L2 Expand by W



L4: L3 NOT L2



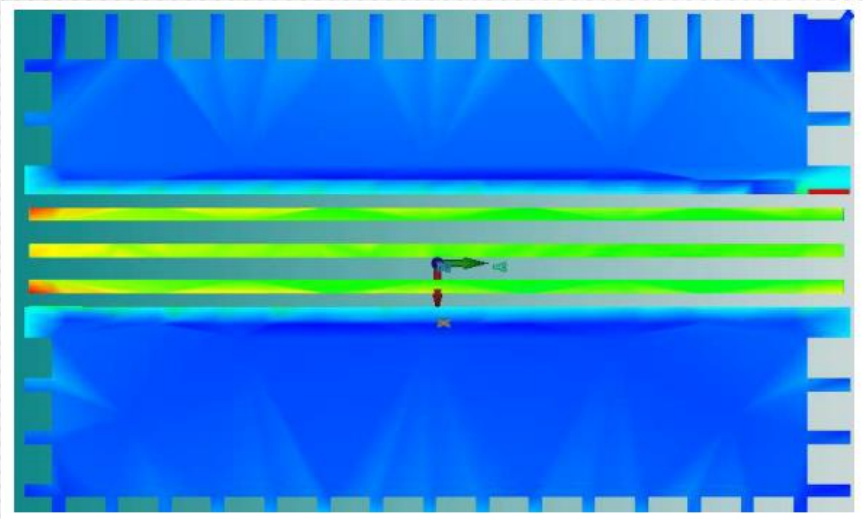
L5: L4 Shrink W/2



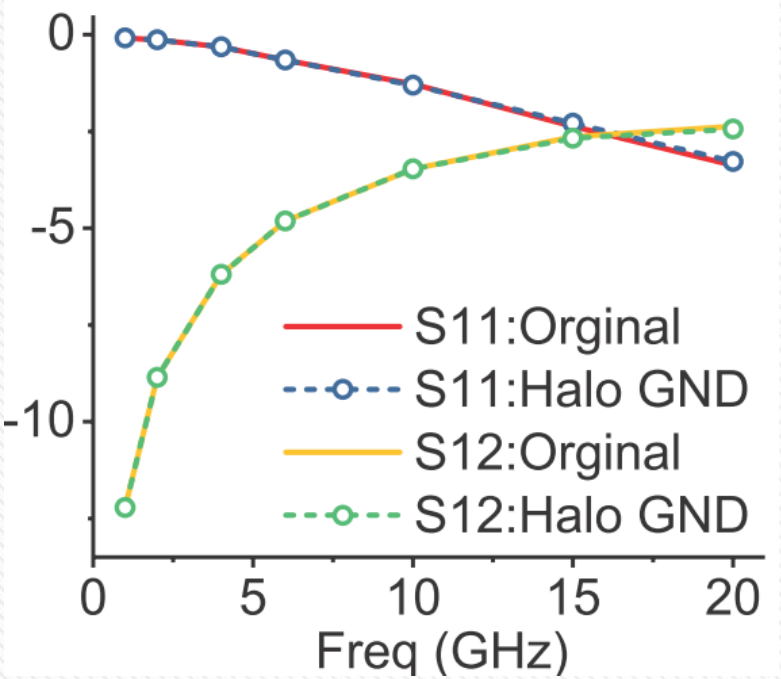
L6: L5 Expand by W/2

Halo Ground Verification

- High accurate compared to the original layout

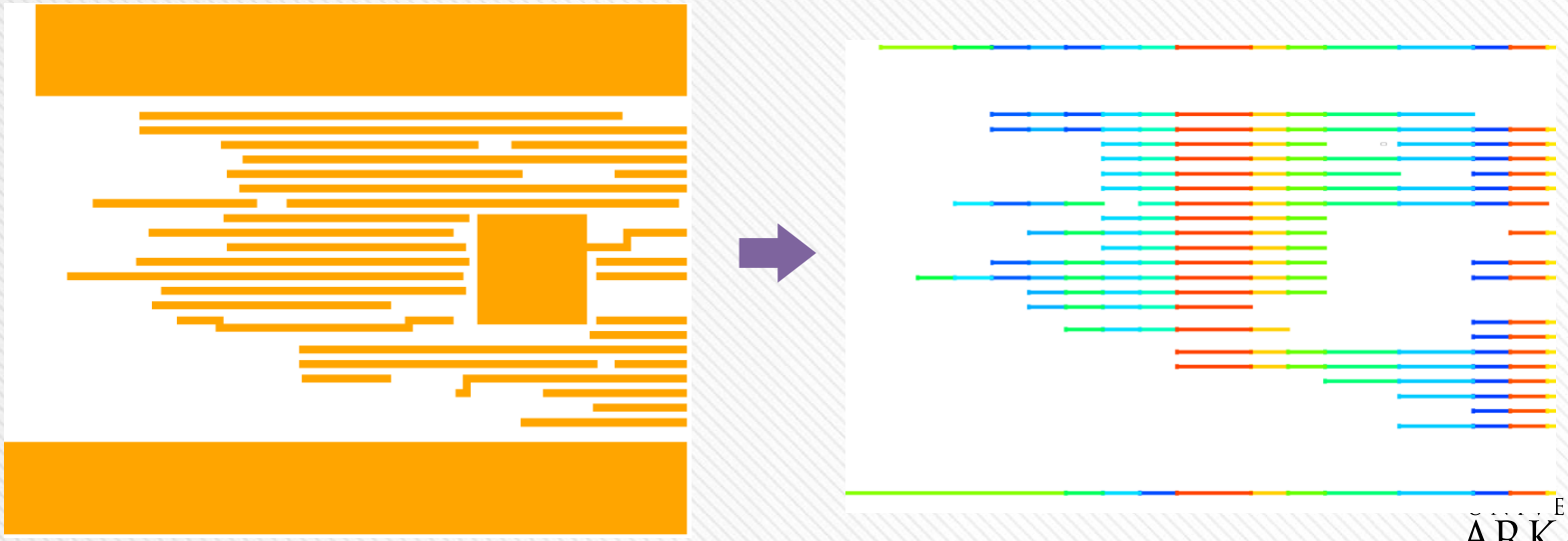


Current density with three signal wires



Bundle Creation

- **Create parallel signal bundles on chip with power and ground wires**
  - Allows efficient computation of partial inductance between any pair of wires, since the lengths of the wires are the same
  - Mutual partial inductance between wires in the same bundle is kept, while mutual inductance across different bundles are ignored.
  - This introduces slight underestimation in mutual inductance, but can achieve great runtime improvement



Loop-based Inductance Computation

- Partial inductance is calculated first for each wire

$$L_{l,k} = \frac{\mu_0 l}{2\pi}\left[\ln\left(\sqrt{k^2+1}+k\right) - \sqrt{k^{-2}+1} + \frac{0.9054}{k} + 0.25\right]$$

- Partial mutual inductance is derived for non-overlapping wires

$$M_{\delta,m,n,k} = \left(L_{\delta+m+n,k} + L_{\delta,k} - L_{\delta+m,k} - L_{\delta+n,k}\right)/2$$

- Then two linear systems are solved with given:
  - Partial inductance matrix P
  - Mesh matrix M
  - Citation vector u

$$\mathbf{Pa=u}$$

$$\mathbf{PB=M}$$

Loop-based Inductance Computation

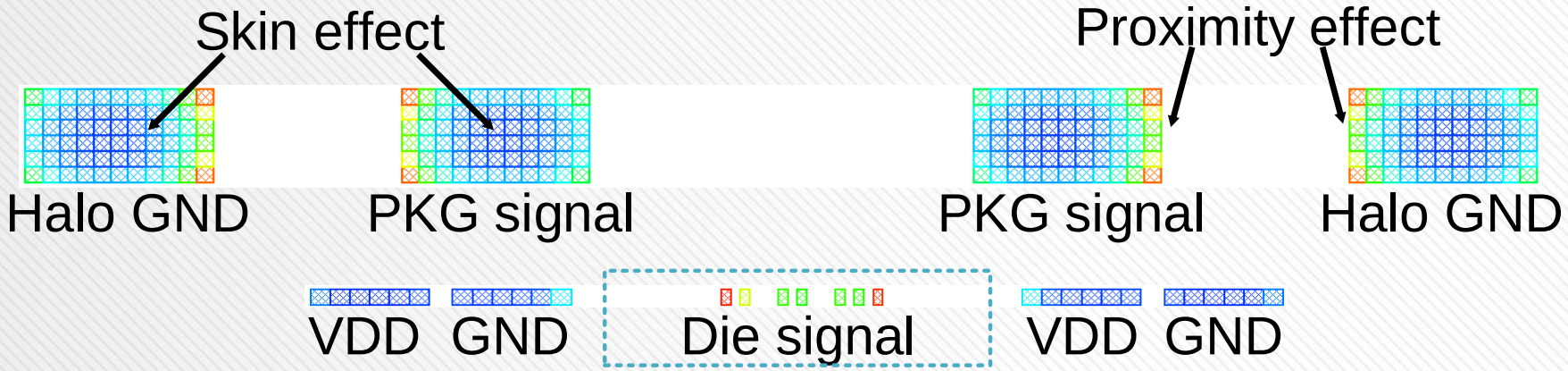
- After return paths are identified, partial inductance matrix P is inversed through LDLT decomposition for fast loop inductance computation

$$Z = (M^T \times I)^{-1}$$

- Current density of each filaments are computed during this process

$$I(j) = B(j) - \Sigma B(i,j) \times a$$

- Full package and all dies on the package are considered together to capture any P2D mutual inductance



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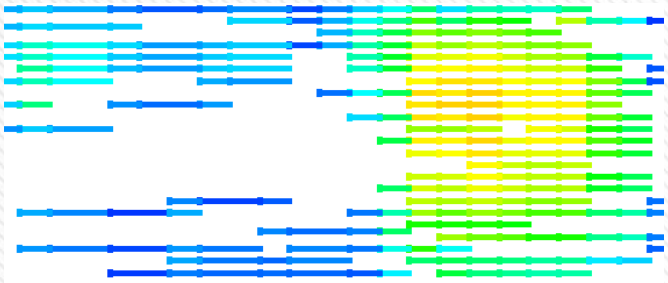
Accurate Extraction

- Our method is then verified against Fast Henry. Accuracy is high and we only need less than 3s to compute more than 1000 package and chip wires



	Fast Henry			Our method					
#	R	TotL	TotM	R	ERR%	TotL	ERR%	TotM	ERR%
1	0.52	34.3	94.8	0.52	-0.7%	35.3	2.8%	89.8	-5.3%
2	0.52	34.5	109.2	0.52	-0.6%	35.5	2.9%	104.6	-4.3%
3	0.42	27.5	106.3	0.41	-1.3%	26.8	-2.6%	96.4	-9.4%
4	0.52	34.8	121.1	0.51	-0.6%	35.8	3.0%	116.5	-3.8%
5	0.52	34.8	120.9	0.51	-0.6%	35.9	3.0%	116.3	-3.8%

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Fast and Parallel Computation

- Each bundle is decoupled during computation, this allows a massive parallel computing to accelerate the extraction process
  - Takes only 2.63s on a single core
  - Computation time reduces from 0.48s to 0.063s if 12 cores are used
  - Includes all M7 and RDL1 routings

Threads #	1	2	4	8	12
ReadGDS	2				
CreateBundle	0.15				
Compute	0.48	0.241	0.138	0.088	0.063
Speed Up	1	1.99	3.48	5.45	7.62
Efficiency	100%	99.6%	87.0%	68.2%	63.5%

Time unit in s

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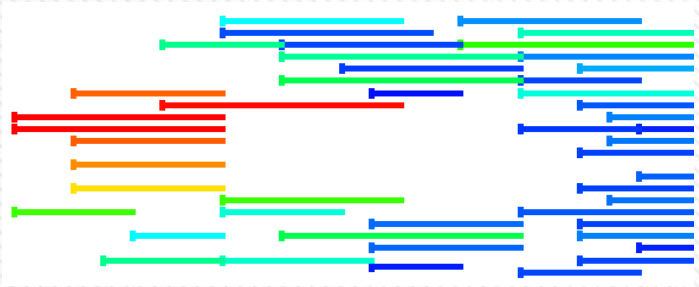
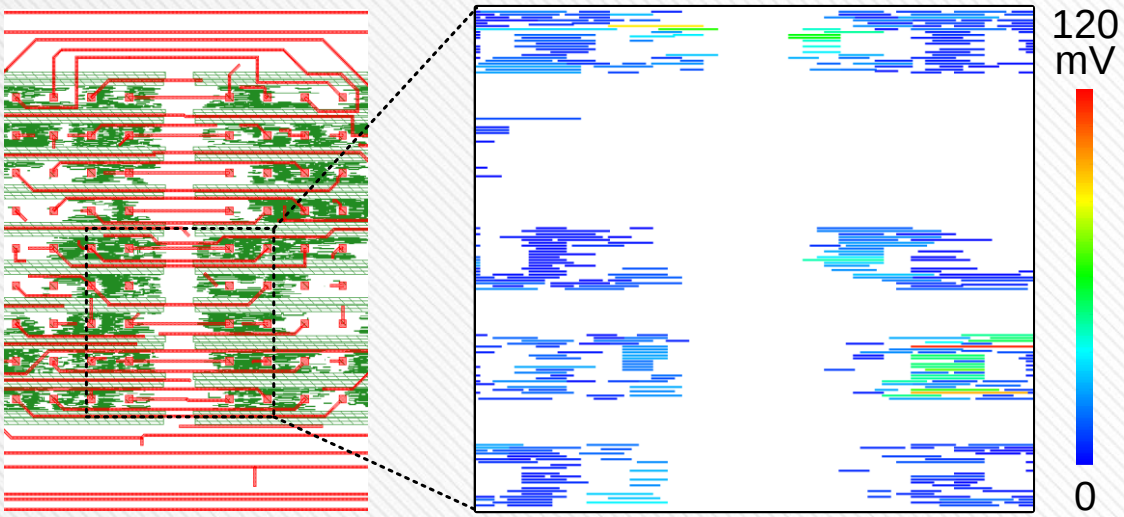
Package-to-Chip Noise Estimation

- **Our tool identifies any noise hot-spot on chip and provides fast estimation of package-induced signal integrity issues**





(a) Original interface (b) Estimated on-chip noise

Package-to-Chip Noise Optimization

- **Optimized PDN routing with finer pitch:**
  - **Average signal wires inside a single bundle is reduced from 19 to 7**

(a) Original PDN

(b) Noise Optimized PDN

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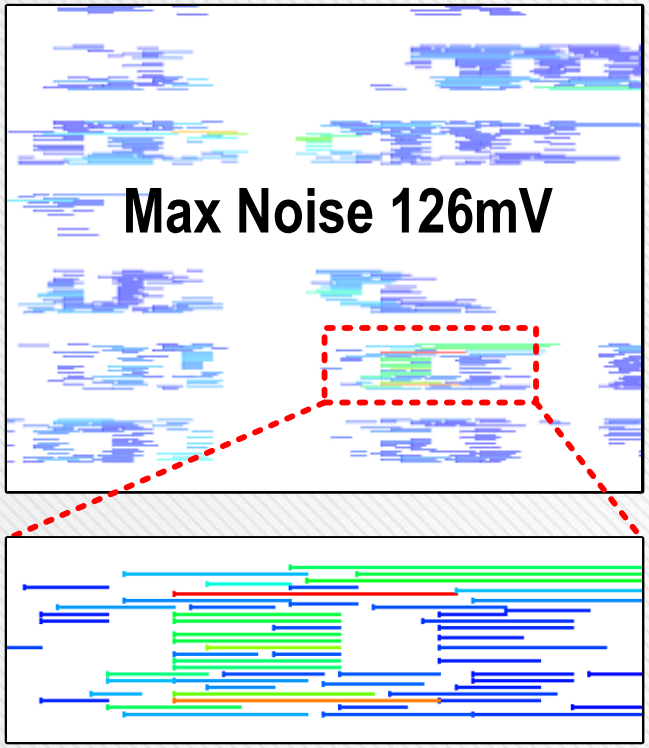
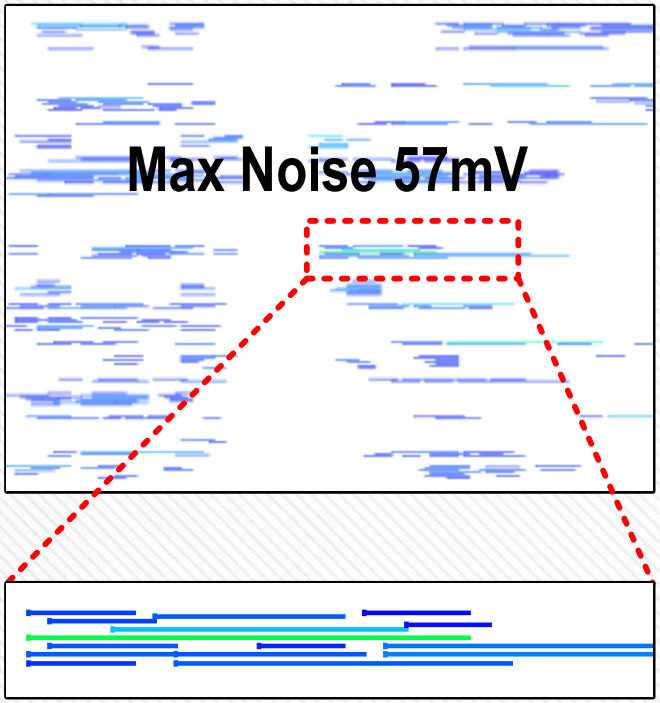
Package-to-Chip Noise Optimization

- **Signal buses are better protected by return paths**
  - **Significantly reduces maximum noise by 54.8%**



(a) Original PDN



(b) Optimized PDN

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Update: P2D Coupling Cap Extraction

- **Our latest research effort includes D2P coupling capacitance extraction using holistic extraction and in-context extraction**
  - GDS-level CAD tools for complete D2P RCLM extraction

Layer	M1	M2	M3	M4	M5	M6	M7	rdl1	rdl2	rdl3
Gcap	45856	24607	10502	6891.8	8429	2486.6	2316.7	17389	898.31	2833.8
Ccap	M1	M2	M3	M4	M5	M6	M7	rdl1	rdl2	rdl3
M1	19093	21827	10267	1785	60	2.22	0.02	0.07	0	0
M2	21827	27895	53198	17424	377	20.68	0.24	3.85	8.55	5.23
M3	10267	53198	28434	88343	5005	185	0.87	3.31	4.4	3.23
M4	1785	17424	88343	33021	56288	5337	359	12.13	8.23	4.57
M5	60.23	377	5005	56288	18016	51222	375	31.08	12.46	6.96
M6	2.22	20.68	185	5337	51222	18708	16623	354	410	2.71
M7	0.02	0.24	0.87	359	375	16623	257	2519	47.05	0.23
rdl1	0.07	3.85	3.31	12.13	31.08	354	2519	134	31207	11.57
rdl2	0	8.55	4.4	8.23	12.46	410	47.05	31207	461	46256
rdl3	0	5.23	3.23	4.57	6.96	2.71	0.23	11.57	46256	231
Ccap	53034	120759	185443	202582	131393	92865	20182	34277	78415	46522

Cap unit in fF

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Conclusion

- Inductive coupling is the major portion of field interaction within P2D interface layers and contributes significantly to package-induced noises on chip wires.
- Our novel inductance extraction methodology based on halo ground, bundle creation, and loop-inductance calculation is highly fast and accurate and allows for chip placement and routing optimization
- Our inductive noise estimation method with optimized PDN routing is highly effective in P2D noise reduction
- P2D coupling is critical for accurate chip-package co-design and signal integrity co-analysis.

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Thank you

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