RESPONSE SURFACE MODELING FOR PARASITIC EXTRACTION FOR MULTI-OBJECTIVE OPTIMIZATION OF MULTI-CHIP POWER MODULES (MCPMS)

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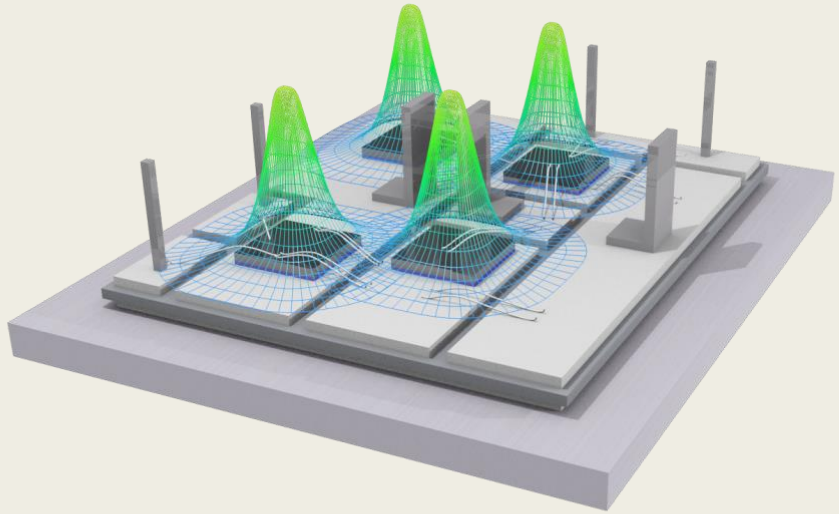
Outline



- Background and Purpose
- Motivation – Response Surface Modeling
- Model Formulation
- Validation Results
- Optimization
- Conclusion and Future Works

BACKGROUND AND PURPOSE

Background and Purpose

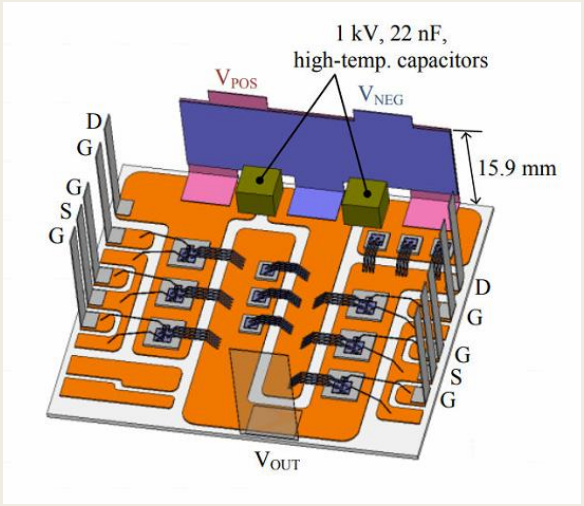
- Recent advances in wide band gap devices allow high voltage, high frequency power module applications ranging from 100 kHz – MHz
- To achieve the best WBG devices performance, attention needs to be paid to electronic packaging and integration
- Interconnect parasitic inductance is one of the main challenges since it results in:
  - *High voltage overshoot ($L\frac{di}{dt}$) [1]*
  - *Increased device switching losses [2]*
  - *Imbalanced current sharing between devices [3]*
  - *Electromagnetic interference and compatibility issues [4]*

→ Minimization of interconnect parasitics during design will mitigate some of the problems above

[1] Y. Ren *et al.*, “Voltage Suppression in Wire-bond Based Multichip Phase-leg SiC MOSFET Module using Adjacent Decoupling Concept,” *IEEE Trans. Ind. Electron.*, vol. 46, no. c, pp. 1–1, 2017
[2] Y. Shen *et al.*, “Parasitic inductance effects on the switching loss measurement of power semiconductor devices,” in *IEEE International Symposium on Industrial Electronics*, 2006, vol. 2, pp. 847–852.
[3] H. Li, S. Munk-Nielsen, S. Bęczkowski and X. Wang, "A Novel DBC Layout for Current Imbalance Mitigation in SiC MOSFET Multichip Power Modules," in *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8042-8045, Dec. 2016.
[4] A. Domurat-Linde and E. Hoene, “Analysis and Reduction of Radiated EMI of Power Modules,” in *Integrated Power Electronics Systems (CIPS), 2012 7th International Conference on*, 2012, vol. 9, pp. 1–6.

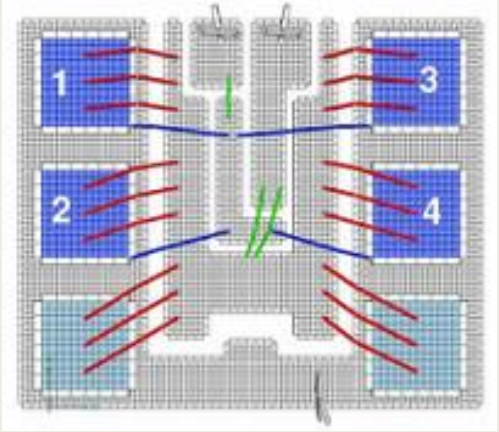
Background and Purpose

- State of the art methods:
  - Finite element method (FEM)
  - Partial Element Equivalent Circuit (PEEC)



ANSYS-Q3D [1]

MCPM Layout



FastHenry [2]

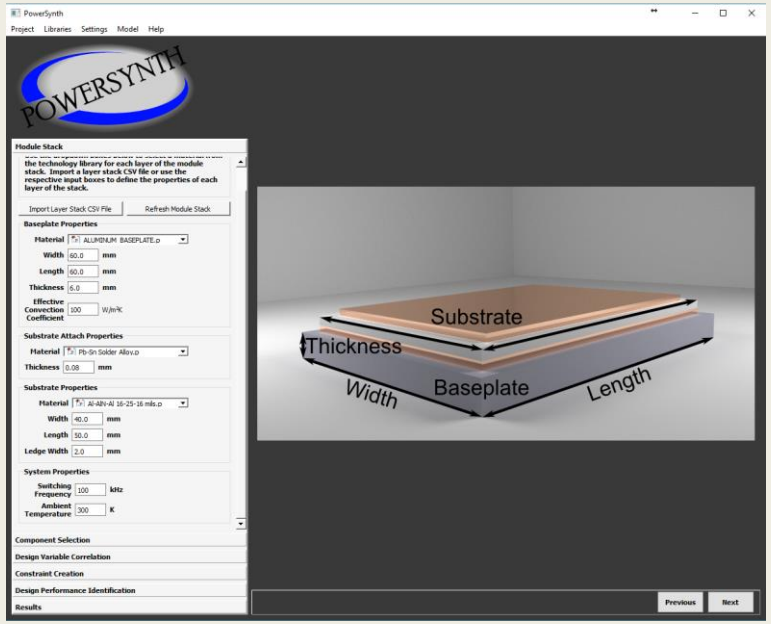
- While ensuring high fidelity, these numerical methods are usually computationally expensive

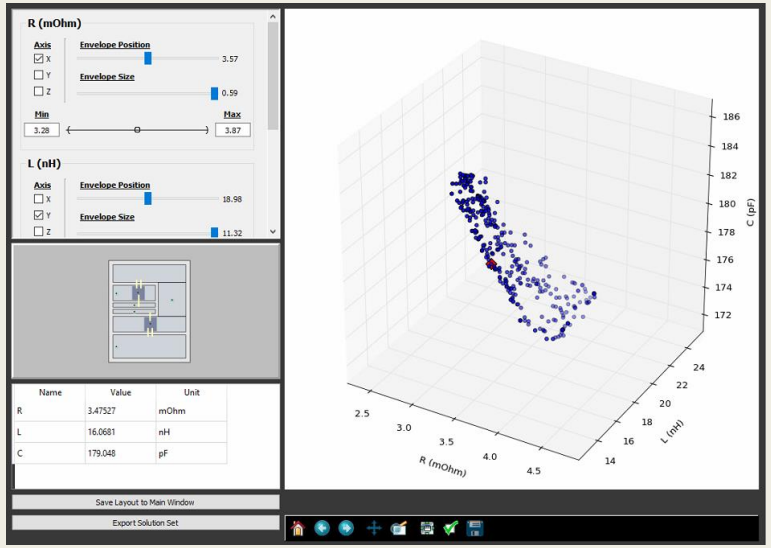
→ Reduce designer flexibility, hard to search for an optimized design

[1] Z. Chen *et al.*, "A 1200-V, 60-A SiC MOSFET multichip phase-leg module for high-temperature, high-frequency applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2307–2320, 2014.

[2] D. Cottet, S. Hartmann and U. Schlapbach, "Numerical Simulations for Electromagnetic Power Module Design," *2006 IEEE International Symposium on Power Semiconductor Devices and IC's*, Naples, 2006, pp. 1-4.

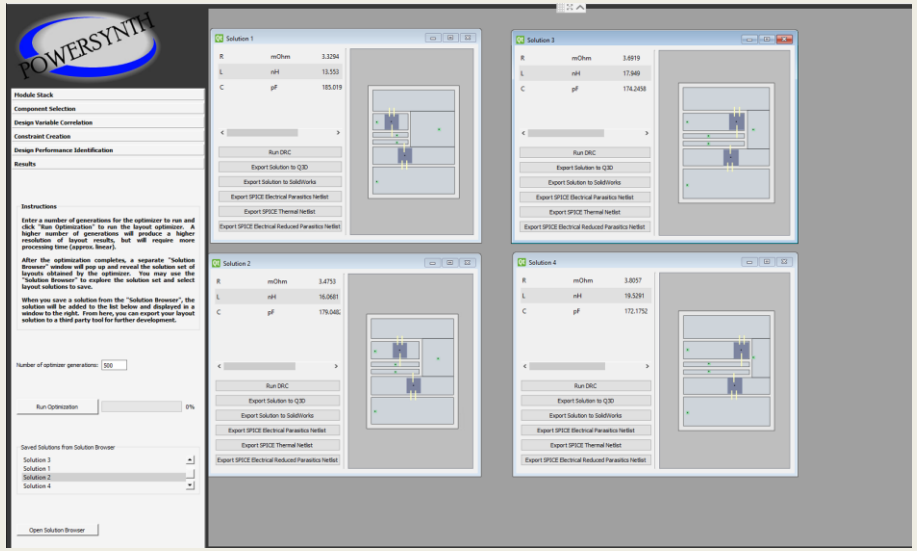
PowerSynth - an MCPM Design Tool





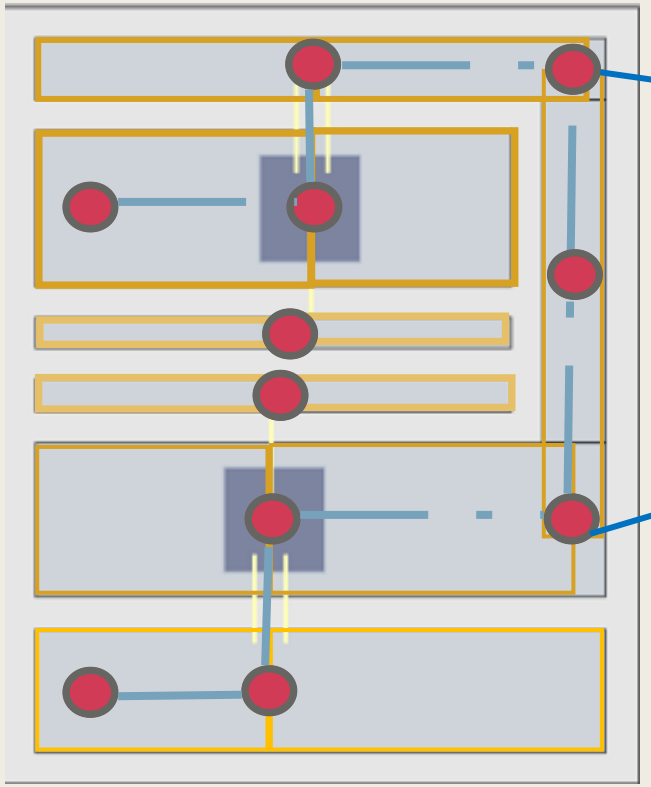
- Developed in the MSCAD group at the University of Arkansas, it is the first design tool that can quickly synthesize and optimize MCPMs layouts
- Analytical formulas along with reduced order models are used to quickly assess thermal and electrical performance

→ Multiple layout solutions are generated in a few minutes to an hour



MOTIVATION

PowerSynth Electrical Model

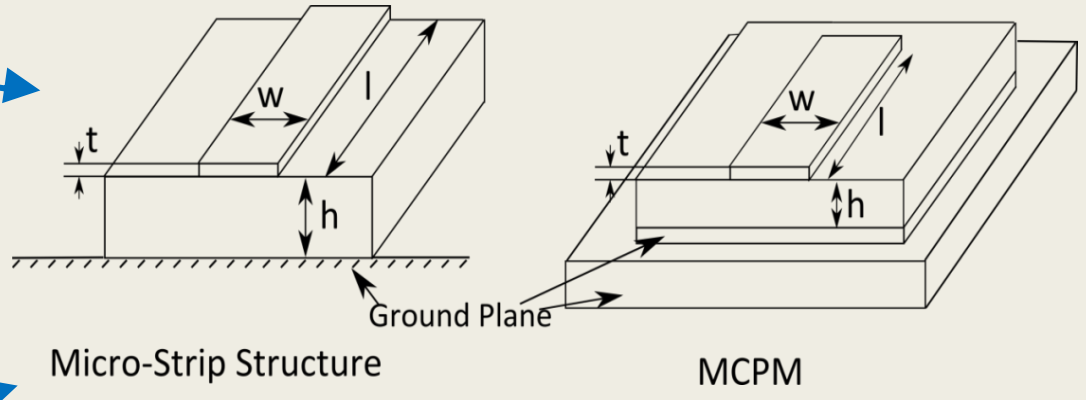


Graph Representation

Connection Nodes

Rectangular Splits

Current Path



Microstrip vs MCPM Structure

→ Convert a layout to a graph based problem, where each edge of the graph stores parasitic information (lumped equivalent network)

→ Analytical formulas (microstrips) are used to approximate the parasitic result

→ Laplacian Matrix can then be used to solve for the effective impedance

PowerSynth Electrical Model

Advantages:

- Mathematical equations are fast → good for parasitic optimization cost function
- Much faster than numerical methods (PEEC, FEM)
- Lumped electrical networks allow fast and easy parasitics analysis between any two nodes

Limitations:

- Equations are designed for a fixed frequency range and aspect ratio → Accuracy is traded off for faster analysis
- Assumption of an unitary current through the layout
- Inductance equations are not frequency dependent

Motivation – Response Surface Modeling

- *Replacing analytical model for **higher prediction accuracy** of trace self-inductance and resistance*
- *Improved accuracy **with faster prediction time***
- *Adaptive method for parasitic prediction of both simple and complex layout geometry (in the future)*
- *Capture the frequency dependent effect accurately*

RESPONSE SURFACE MODEL FORMULATION

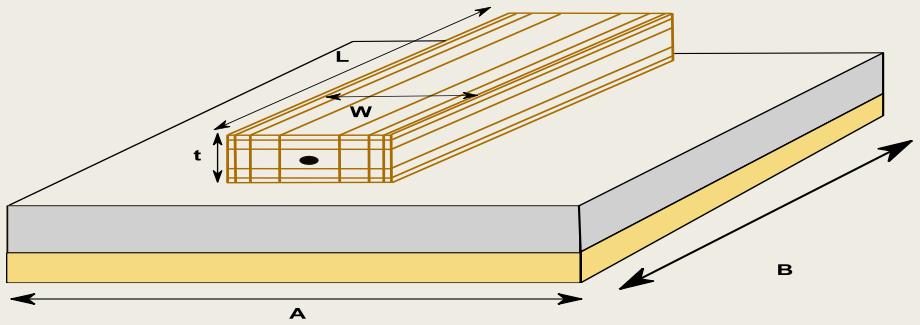
Response Surface Model Formation Steps

Model Formulation

- Skin depth equation is used to compute the skin-depth of the highest frequency input

$$\delta = \sqrt{\left(\frac{2}{\omega\mu\sigma}\right)}$$

- The skin-depth value is used to create the mesh in FastHenry

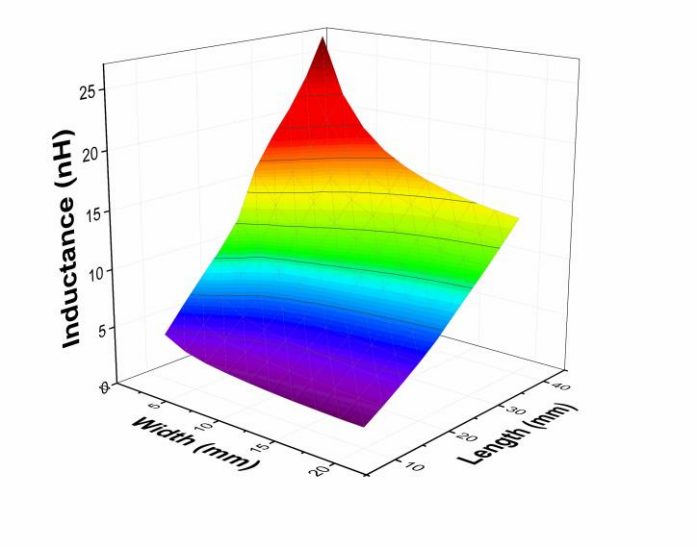


Mesh Setup in FastHenry

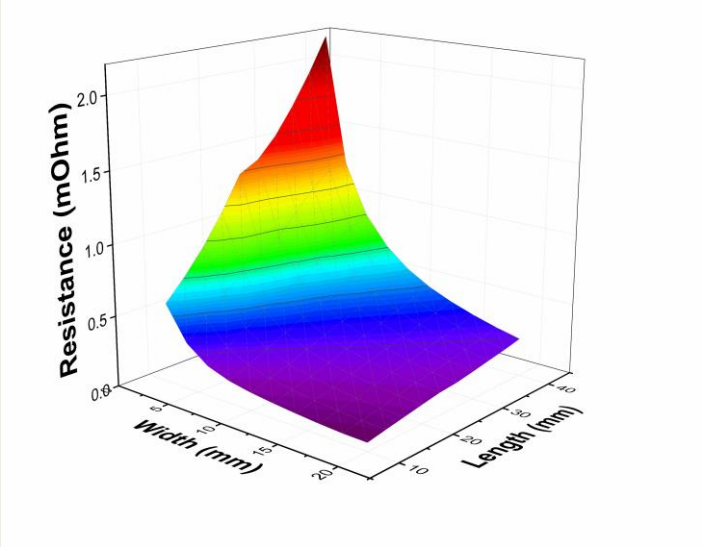
- Design parameters are set based on the DBC sizes and design rules given by user

Parameter	Range (mm)
W	Design rule minimum to max (A, B)/2
L	max (A, B)/4 to max (A, B)

- Simulation batches in FastHenry are run for each different design parameter configuration
- Kriging method is used to find the relationship between design parameters and parasitic results

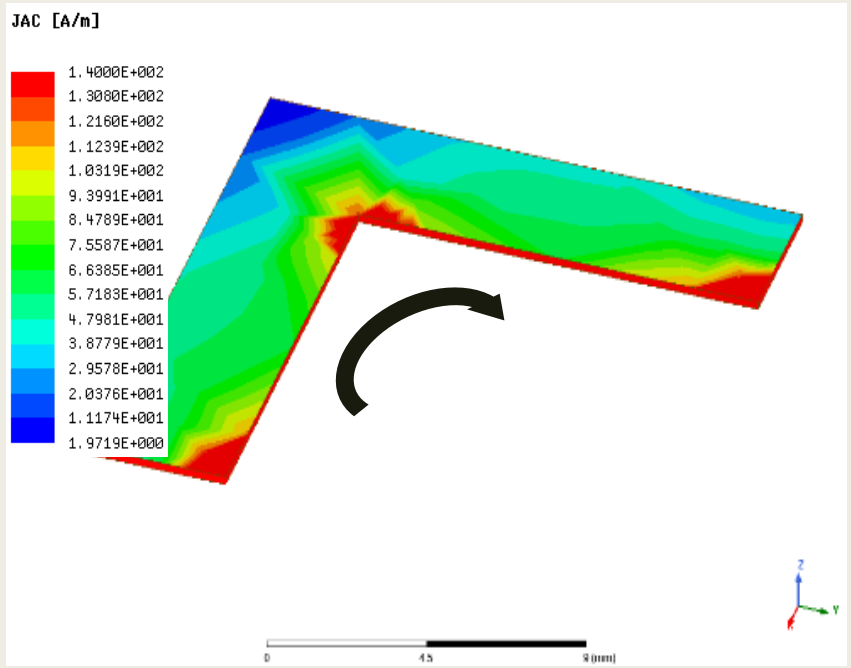


Inductance Response Surface



Resistance Response Surface

90-Degree Corner Correction Model



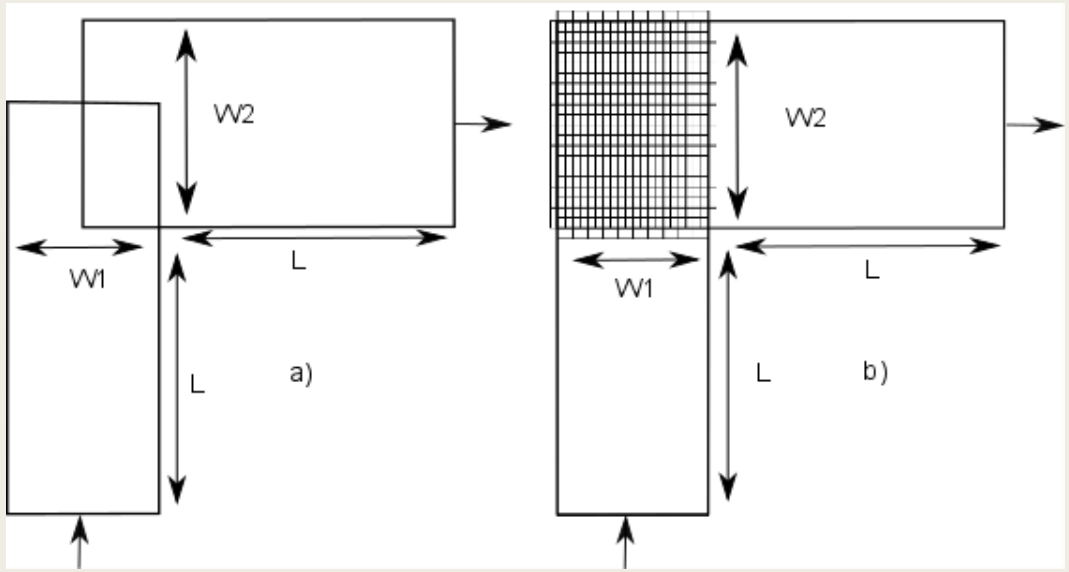
Current Crowding Effect

- A common practice is using lumped element circuits to simply add the inductance values of perpendicular traces
- Due to the current crowding effect, current usually concentrates at the inner corner

→ The current loop is therefore smaller

→ Overestimation in inductance calculation

90-Degree Corner Correction Model



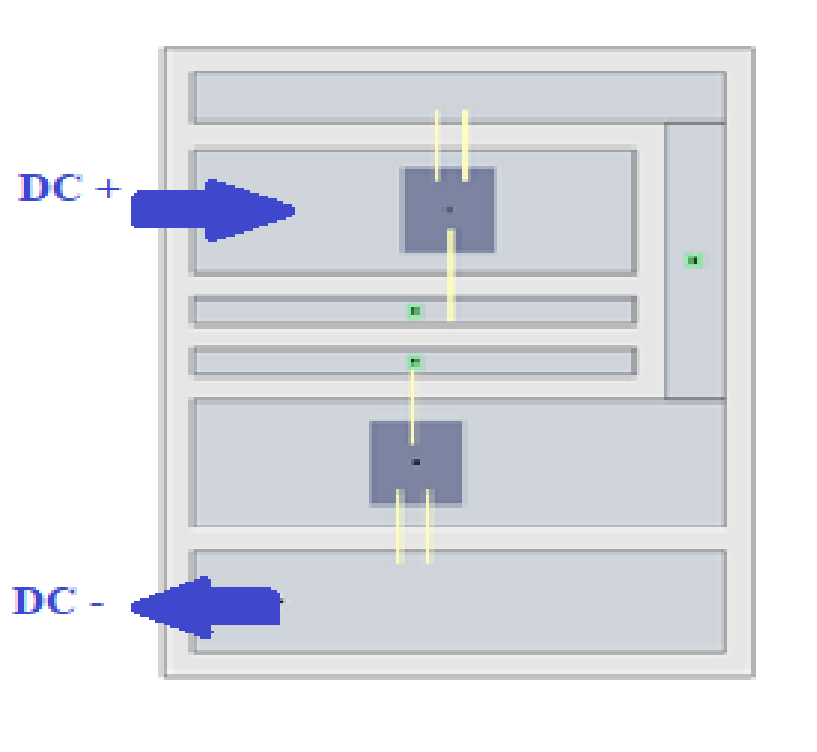
(a) 90-degree corner approximation in PowerSynth,
(b) 90-degree corner simulation in FastHenry

- A simulation is run in FastHenry (right) the result is subtracted from the addition of 2 rectangular pieces
- The inner Length of the corner is fixed while the Widths (W1 , W2) are varied
- A response surface is built to map W1 and W2 with the result of the overestimation
- This can be used to quickly evaluate the overestimation result later

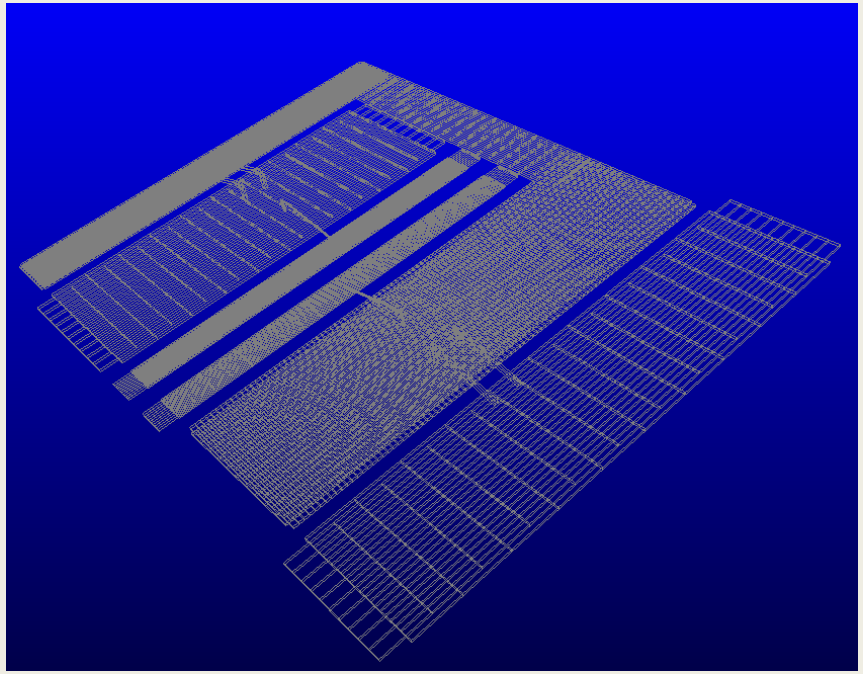
VALIDATION

Validation to FastHenry

- A simple 2-position half bridge layout is created in PowerSynth. The parasitic result is measured from DC+ to DC- terminals
- Response surface models are used to replace analytical formulas in PowerSynth
- The layout is extracted to FastHenry for response surface parasitic extraction from 10kHz to 1MHz



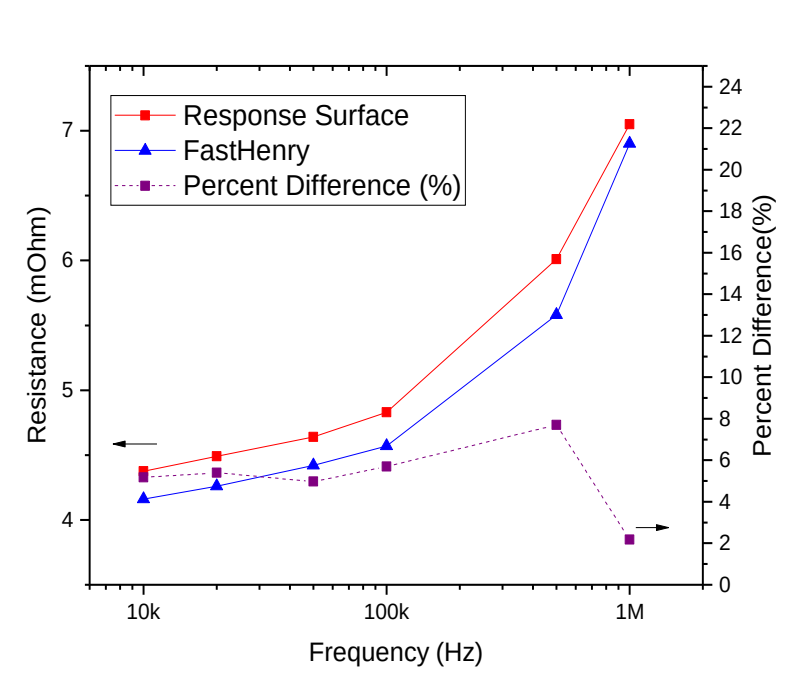
Half-bridge layout in PowerSynth

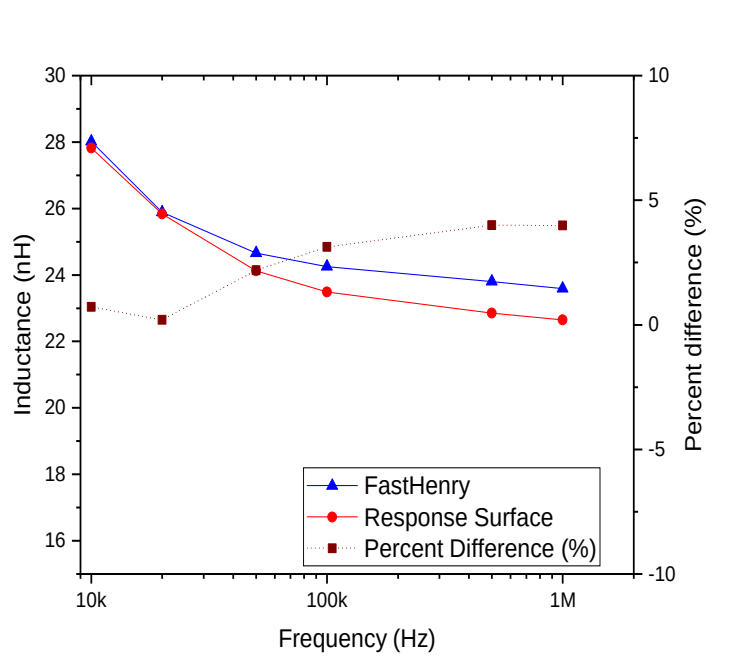


Exported layout to FastHenry

Validation to FastHenry

- Simulation results show less than 8 % error for both inductance and resistance extractions



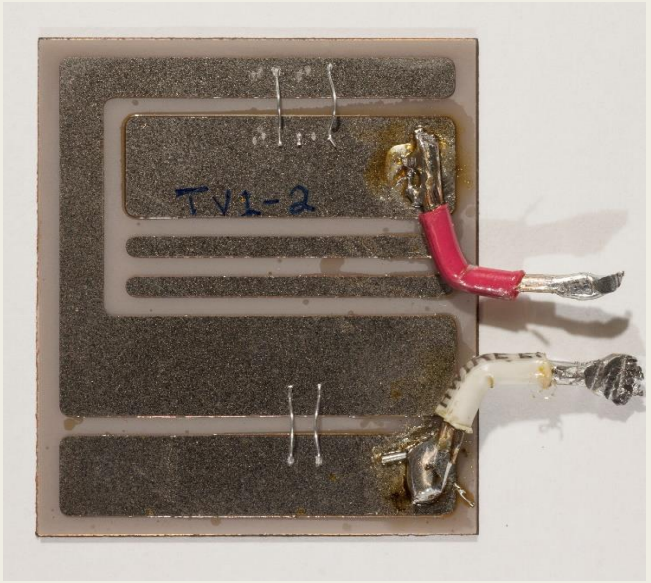


Simulation time comparison

	FastHenry	Response Surface	Speed up
Extraction Time	~300 s	~50 ms	x6000

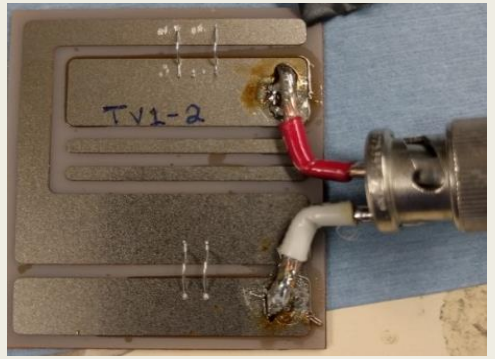
Measurement Setup

- The test vehicle is built upon an aluminum nitride DBC substrate
- Measurements are performed using an LCR meter from 10kHz to 1MHz
- Time Domain Reflectometry (TDR) is also performed to validate the inductance result at high frequency



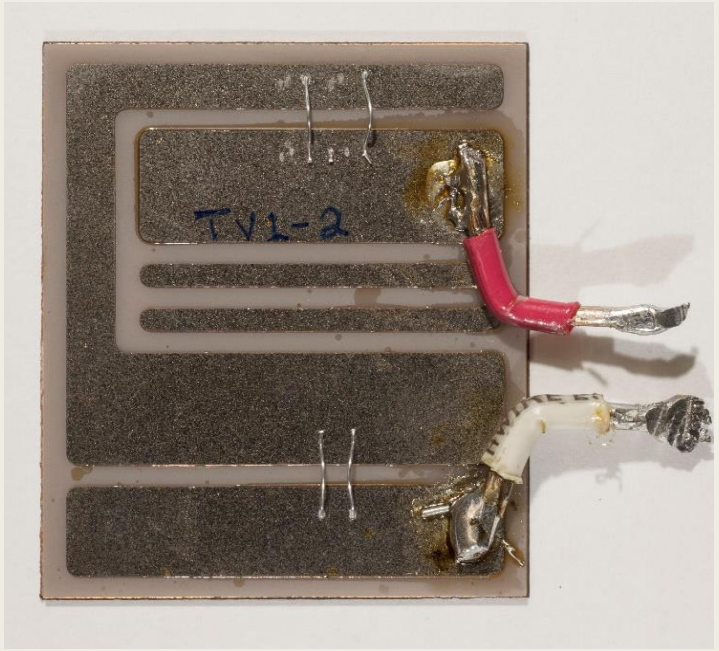
Fabricated Test Vehicle

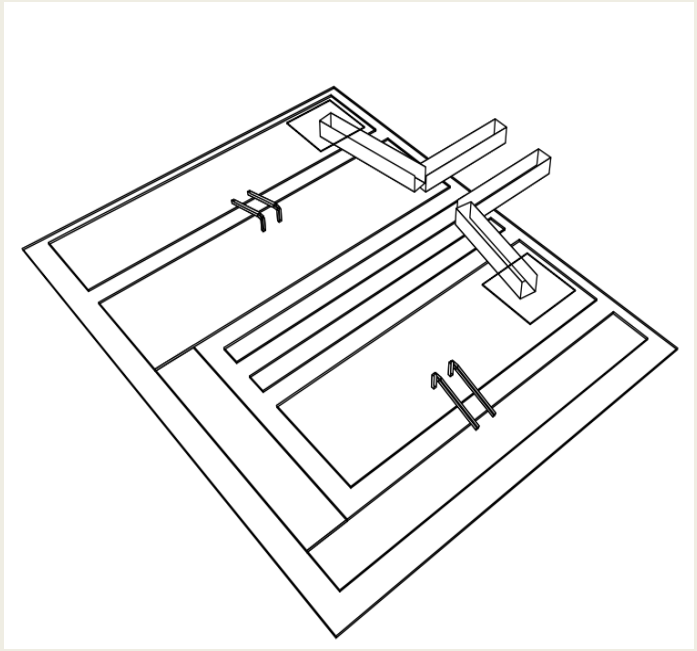
LCR Measurement Setup



Coax Cable Connection for TDR

Validation to Measurement



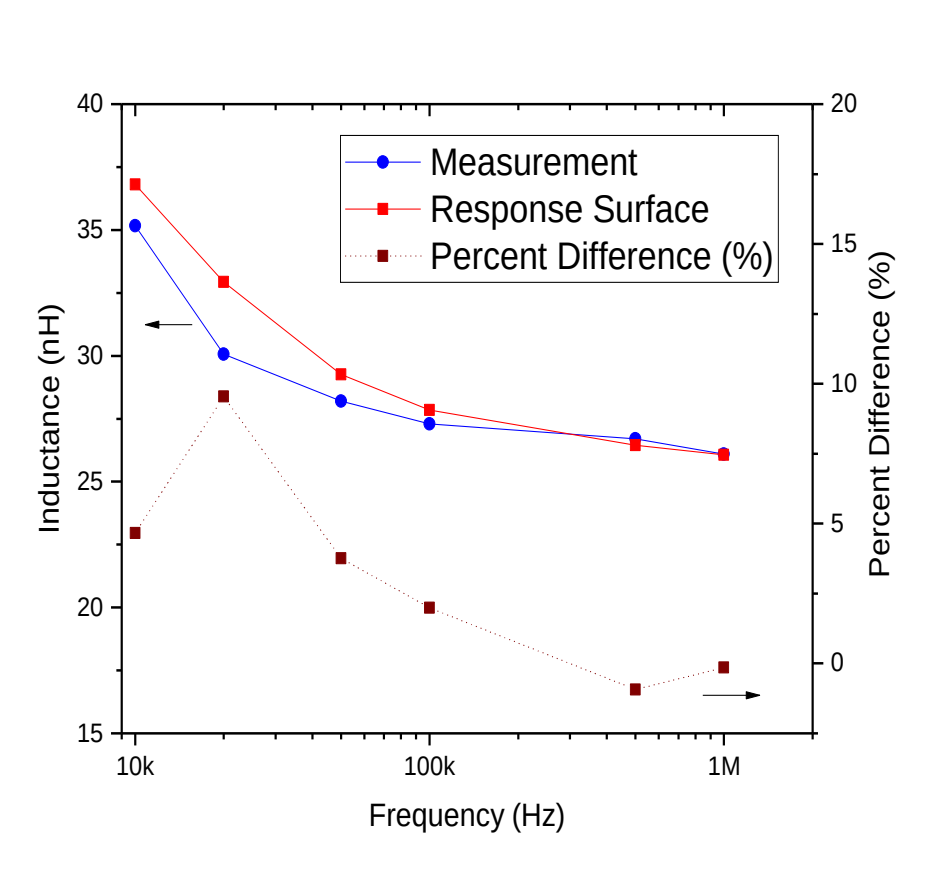


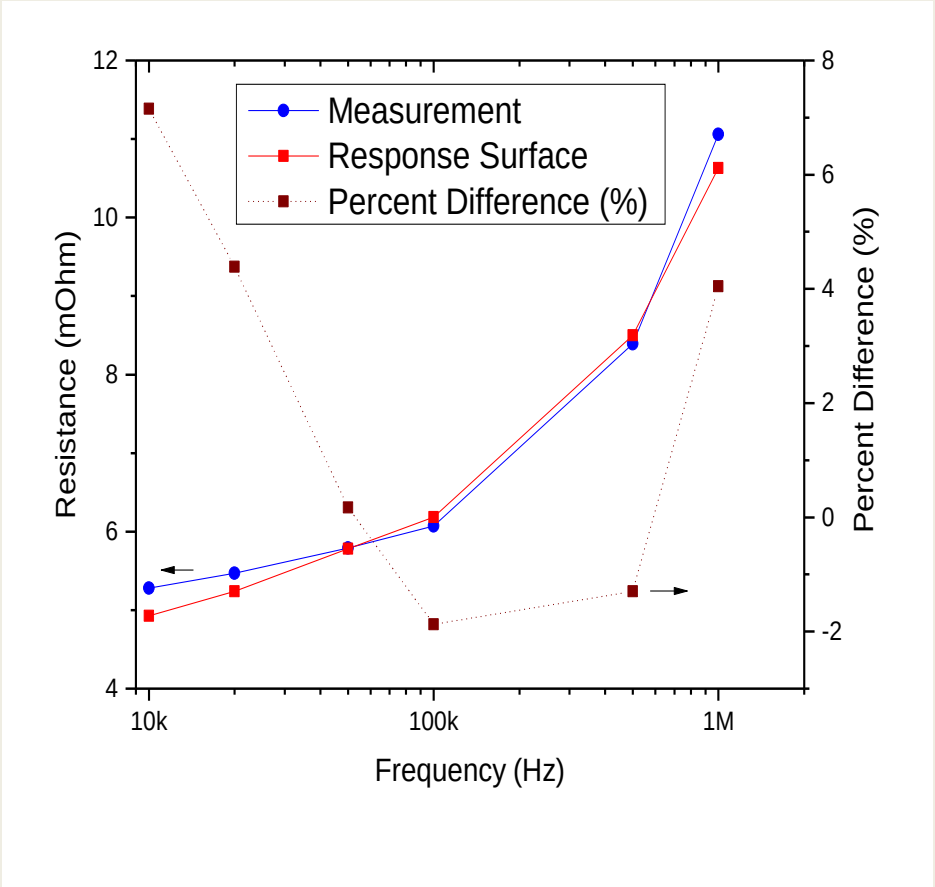
Fabricated Test vehicle

FastHenry with Connection Wires

- Another FastHenry simulation is made to take into account the connection wires at DC+ and DC- terminals
- The connection wires inductance and resistance contributions are then added to the results from PowerSynth

Validation to Measurement (LCR)

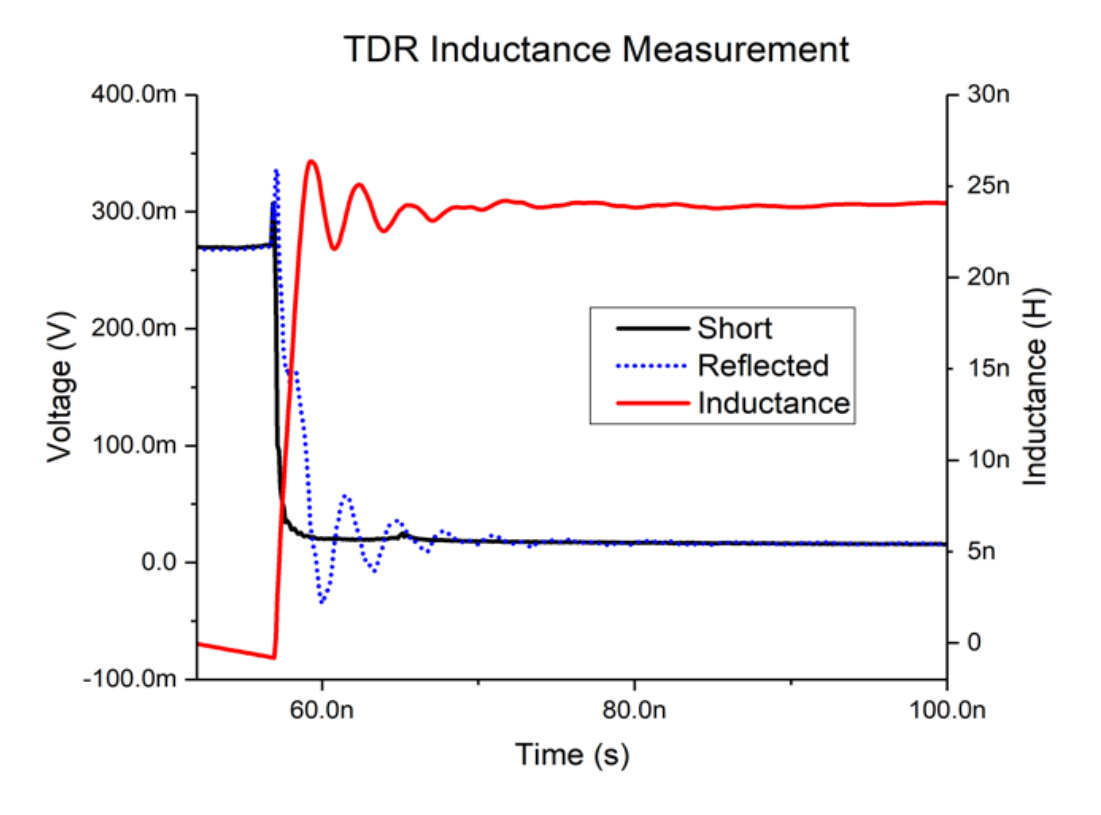




- A maximum error of 7.5% was found for resistance and 10% was found for inductance

Validation to Measurement (TDR)

- Measurement result from TDR shows 24.86 nH. This is very close to the PowerSynth extracted result at 1MHZ (26.1 nH)

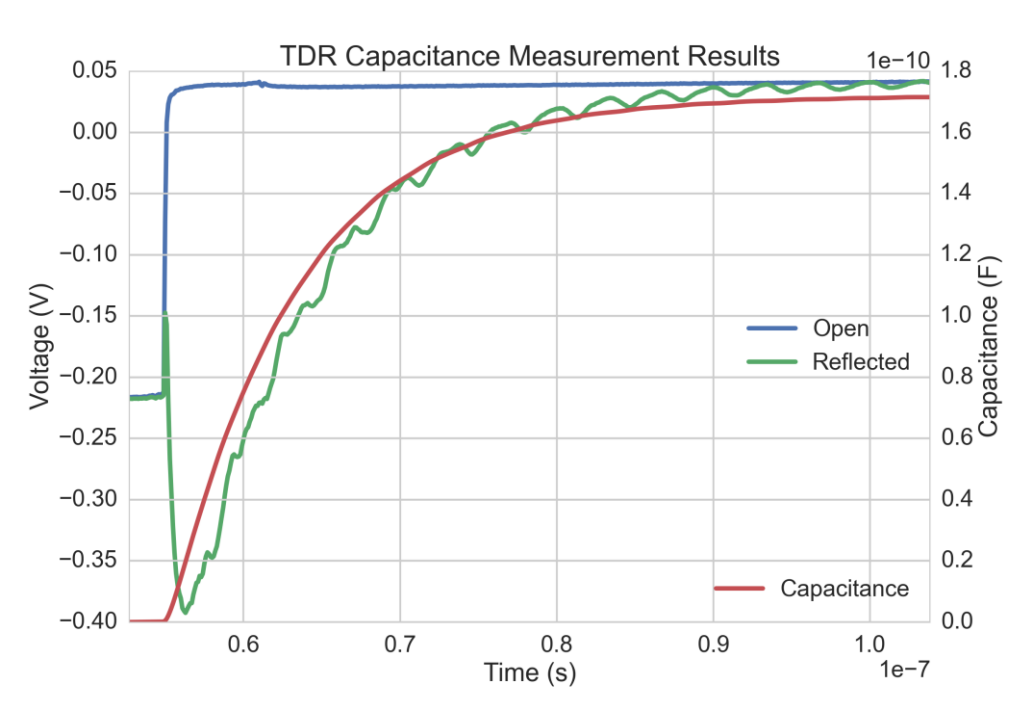


PowerSynth Ind (1MHz)	Measurement (TDR)	Measurement (LCR @ 1MHz)
26.1 nH	24.86 nH	25.58 nH

- This has shown only 4.98% and 2.03% error against TDR and LCR measurements, respectively

Validation to Measurement (TDR)

- In addition, the capacitance measurement is also performed to validate the capacitance extraction from PowerSynth



PowerSynth Cap	Measurement (LCR)	Measurement (TDR)
169.5 pF	160.8 pF	170.95 pF

- This has shown only 5.41% and 0.85% error against LCR and TDR measurements, respectively

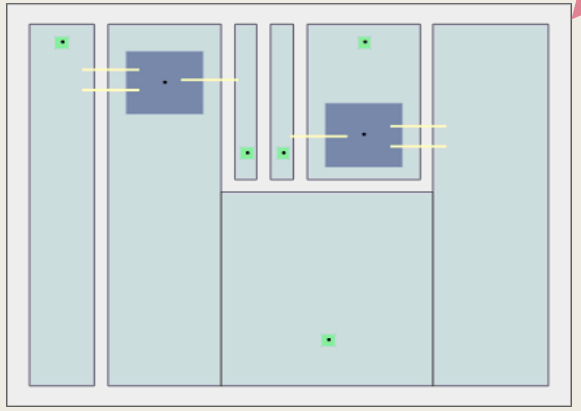
OPTIMIZATION

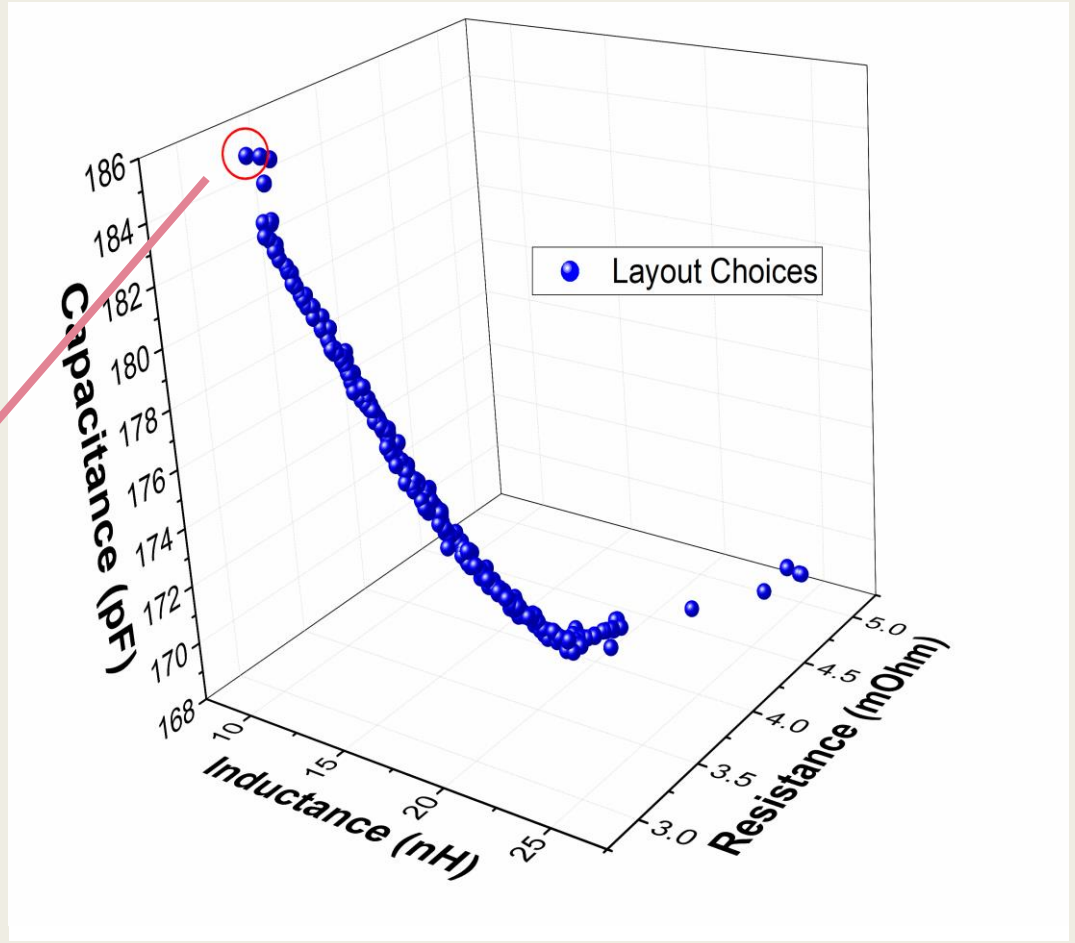
Layout Optimization

Optimized Layout RLC Extraction Results at 100 kHz

	R (mOhm)	L (nH)	C (pF)
Example Layout	4.83	23.49	169.5
Optimized RL	3.06	10.69	185.79
Improvement (%)	36.6	54.5	-9

- To compensate for the 9% increase in C, the best layout has shown parasitic L and R reductions of 54.5% and 36.6%, respectively





Pareto Front Representation in PowerSynth

CONCLUSIONS AND FUTURE WORK

Conclusion

- Response surface models ensure high prediction accuracy while thousands times faster than numerical methods
- Optimization using response surface effectively improve design performance
- Frequency dependent effects can be captured accurately
- Response surface for corner correction captures the non-uniform current distribution

Future Work

- More complicated layout structures will be analyzed and validated

Collaboration

- Micro-channels heatsink modeling (Howard University)
- New optimization methodologies (UIUC)

Q & A