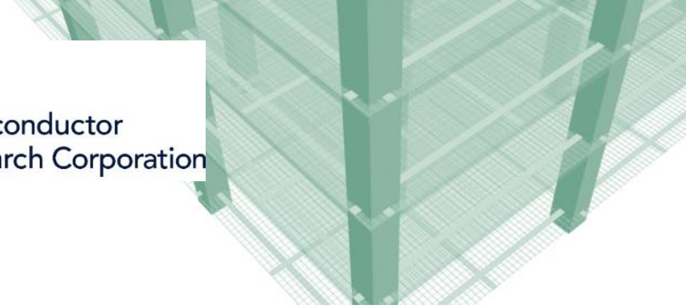
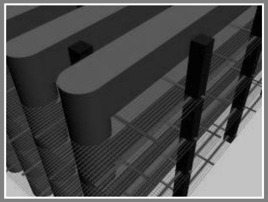
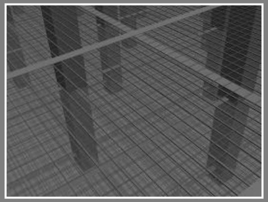
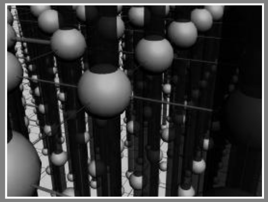


Fast and Accurate Full-chip Extraction and Optimization of TSV-to-Wire Coupling

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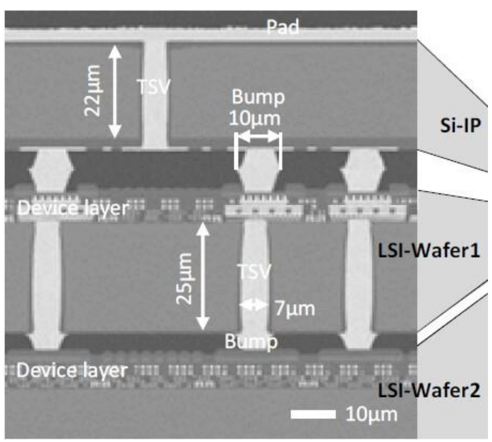
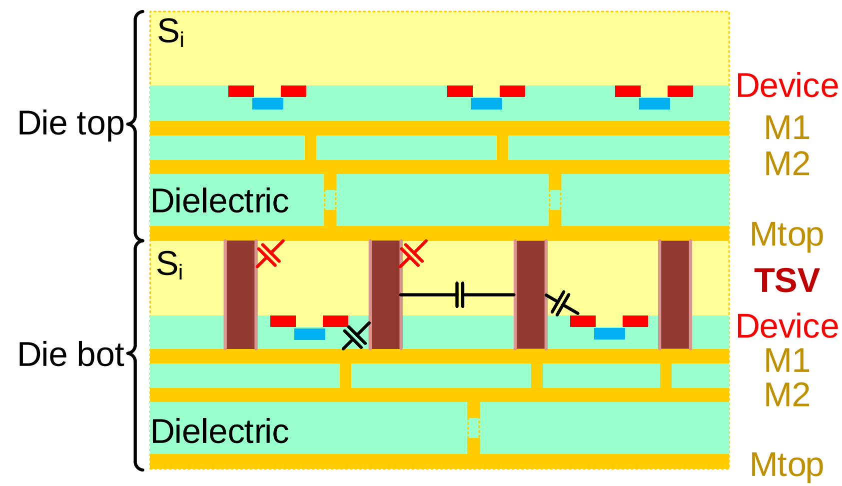
[2]Mentor Graphics, Fremont, CA

Introduction

- 3D IC: a solution to alleviate interconnect delay and power
- New parasitics exist in 3D IC
  - TSV-to-TSV, TSV-to-wire coupling, μbump parasitics etc.
  - Need 3D interconnection extraction tool for TSV-to-wire coupling
  - Affect performance, power, noise[1]



SEM of a via-last die-stacking technology[2]

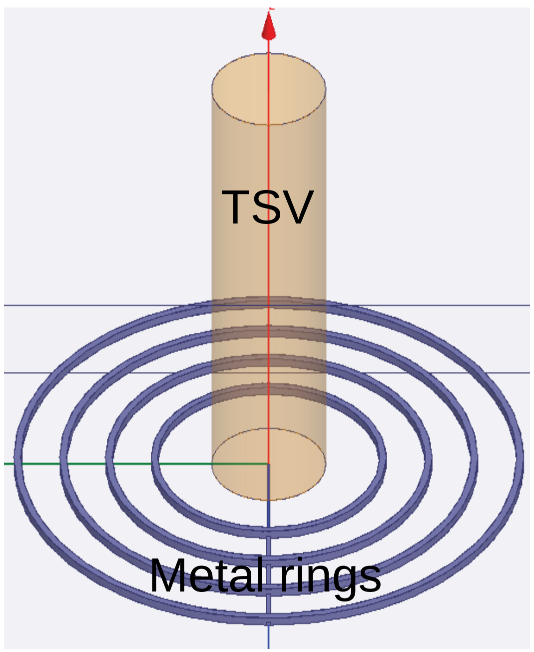


TSV related coupling elements

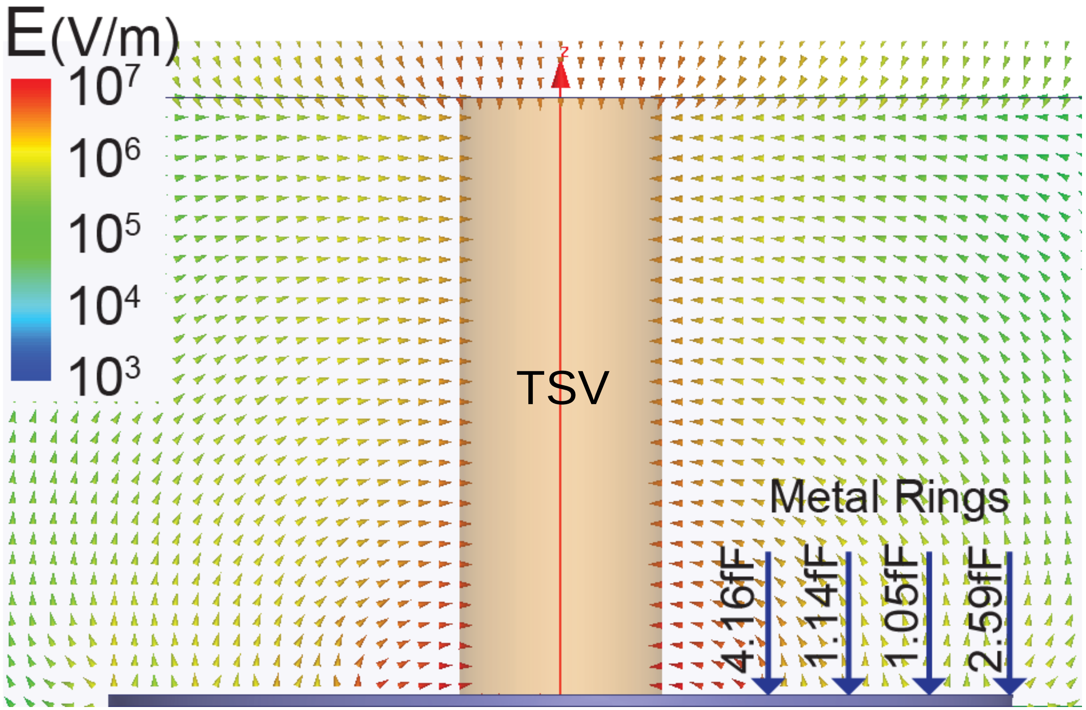
[1] C. Liu et al., "Full-chip TSV-to-TSV coupling analysis and optimization in 3D IC," DAC11
[2] Aoki, M. et al, "Fabricating 3D integrated CMOS devices by using wafer stacking and via-last TSV technologies, IEDM13

Multiple Wire Effect

- **A TSV structure with 4 wire rings are simulated in HFSS**
- **Much smaller coupling cap to TSV on Middle rings**



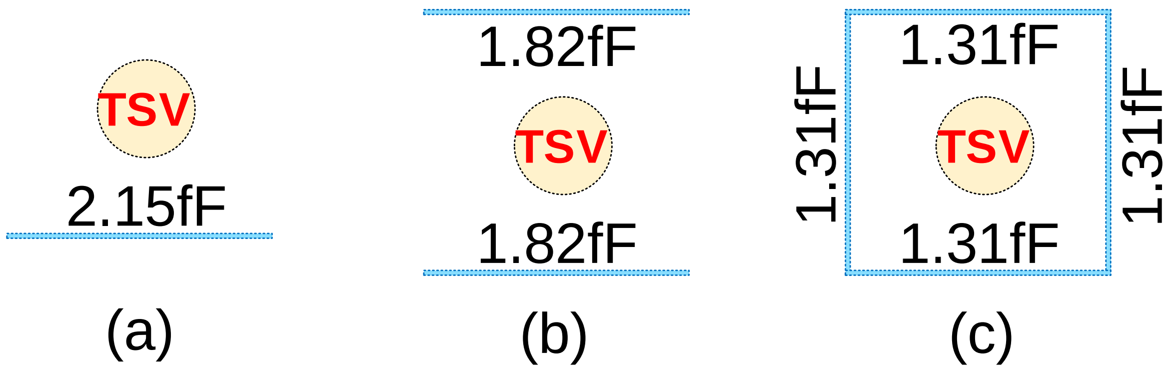
TSV-ring structure



E-field distribution and extracted capacitance

Wire Coverage Effect

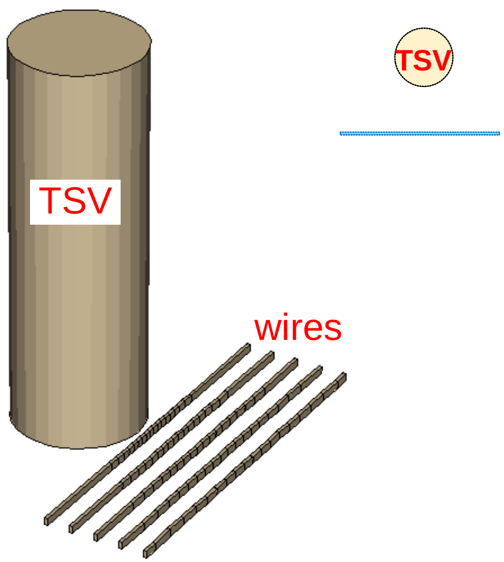
- **More wire covering leads to heavier E-field sharing around TSV**
  - **Reduces the coupling capacitance per each wire surrounding TSV**
  - **The total coupling capacitance to TSV still increases**



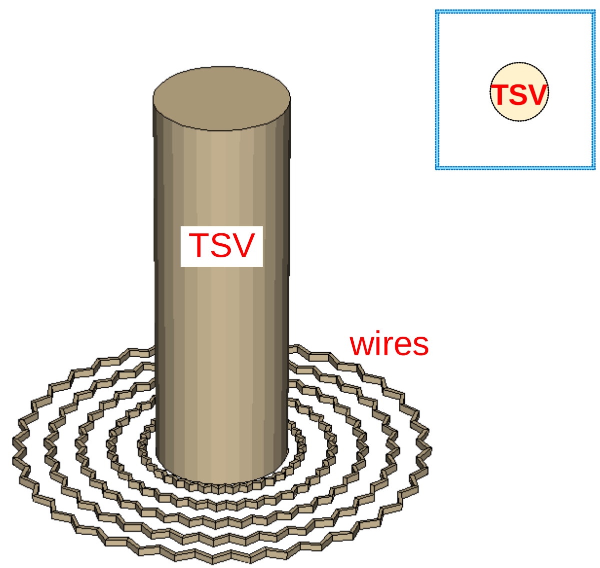
Three case studies of wire coverage effect

TSV-to-wire Libraries Generation

- **Two libraries are built to handle E-field sharing effects:**
  - **Line library: used for cases when wire coverage is low**
  - **Ring library: used for cases when wire coverage is high**



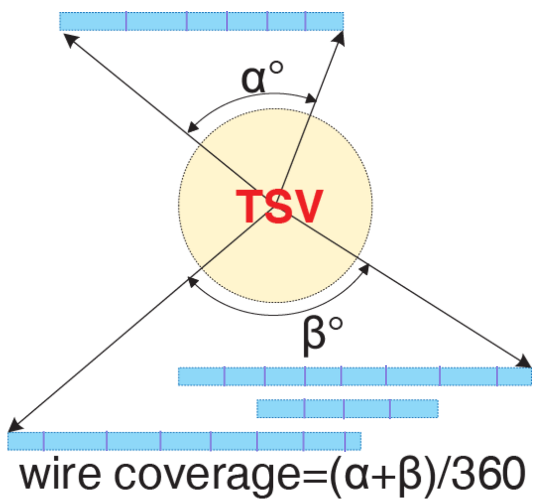
Line library

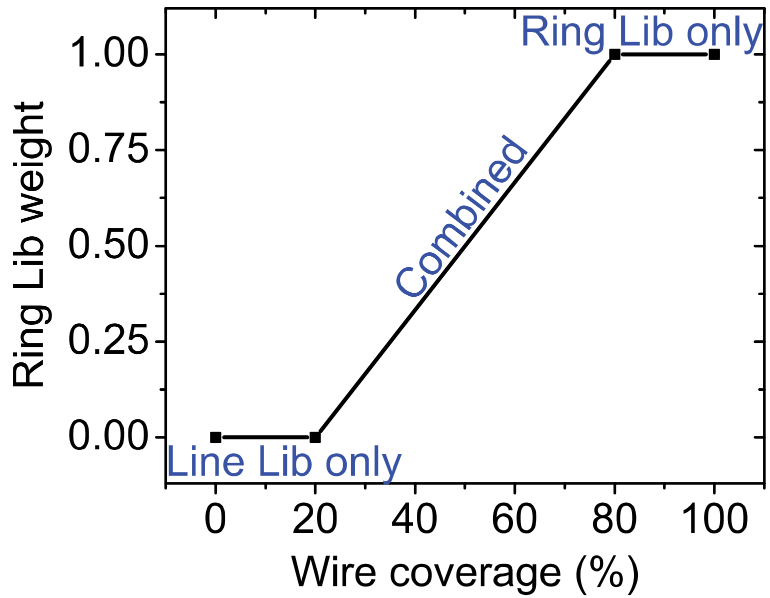


Ring library

Pattern Matching Algorithm

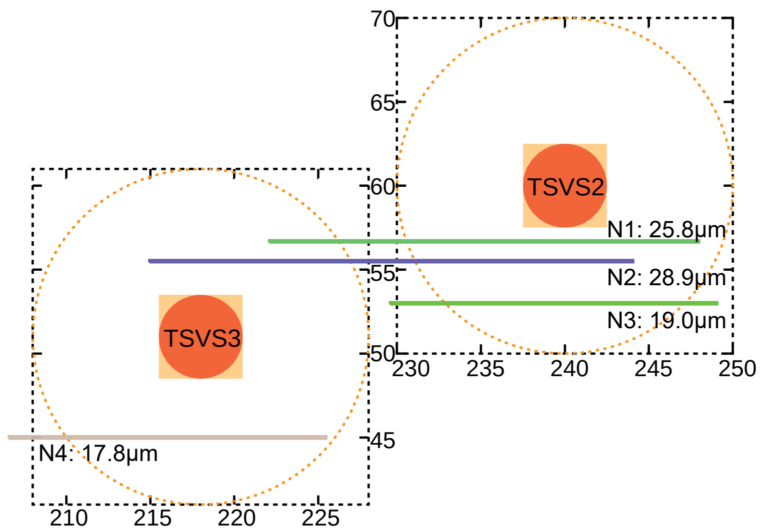
- **Extract TSV-to-wire capacitance on the nearest metal layers**
- **Divide wire into segments**
  - **finer grid sizes are given to near-TSV region**
- **Segment capacitances extraction based on wire coverage and neighbor segments**





Validation with Sample Layout

- **We validate the extraction result against Synopsys Raphael on a sample layout from a 3D design**



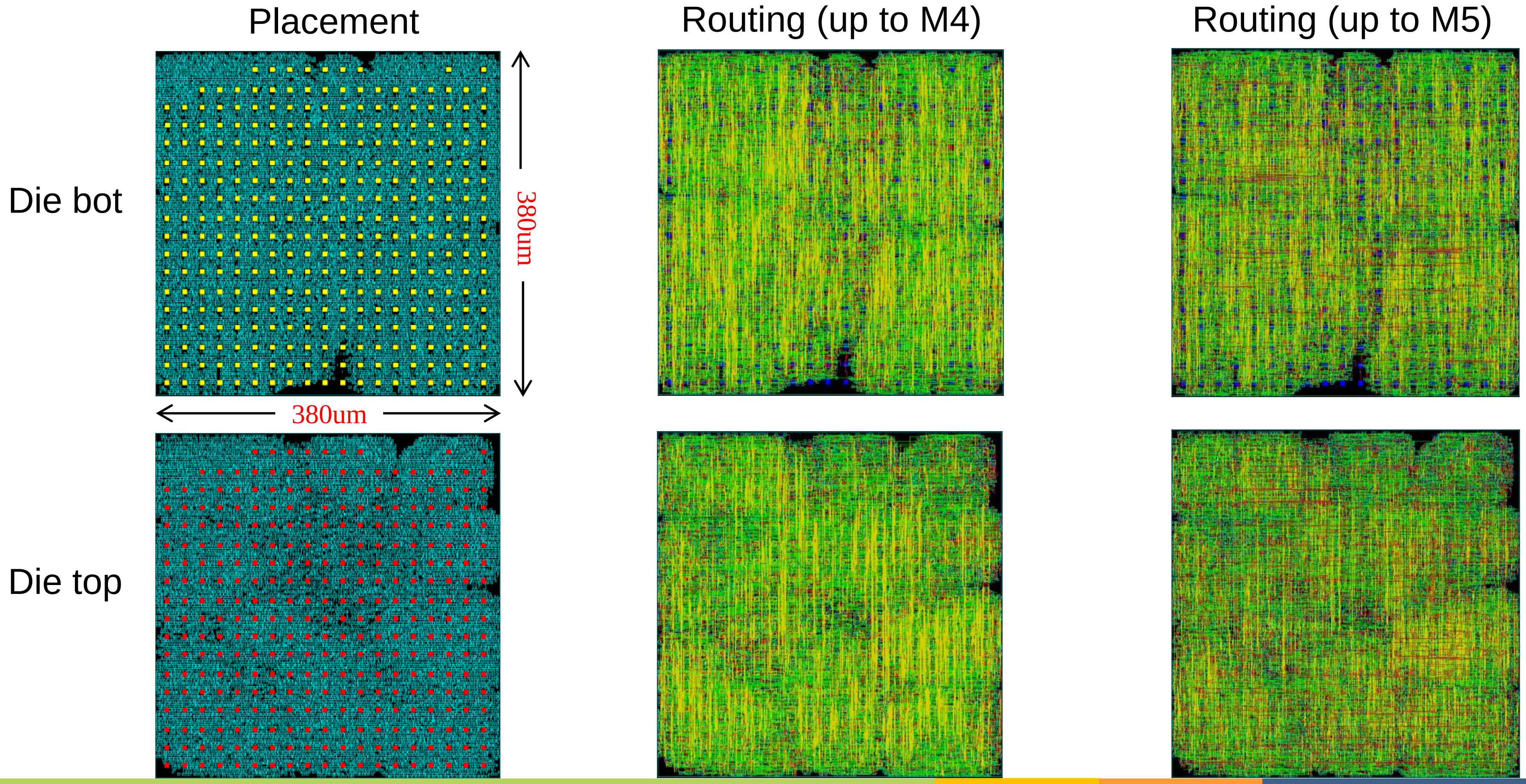
Sample Layout

TSV	Wire	Raphael	Our method		
			Ring lib	Combined	Line lib
S2	N1	**1.76**	1.49	1.93	2.07
S2	N2	**0.76**	0.68	0.76	0.78
S2	N3	**0.81**	0.86	0.81	0.79
S3	N1	**0.31**	0.29	0.31	0.34
S3	N2	**1.38**	1.28	1.33	1.37
S3	N4	**1.62**	1.49	1.53	1.57

Extraction results

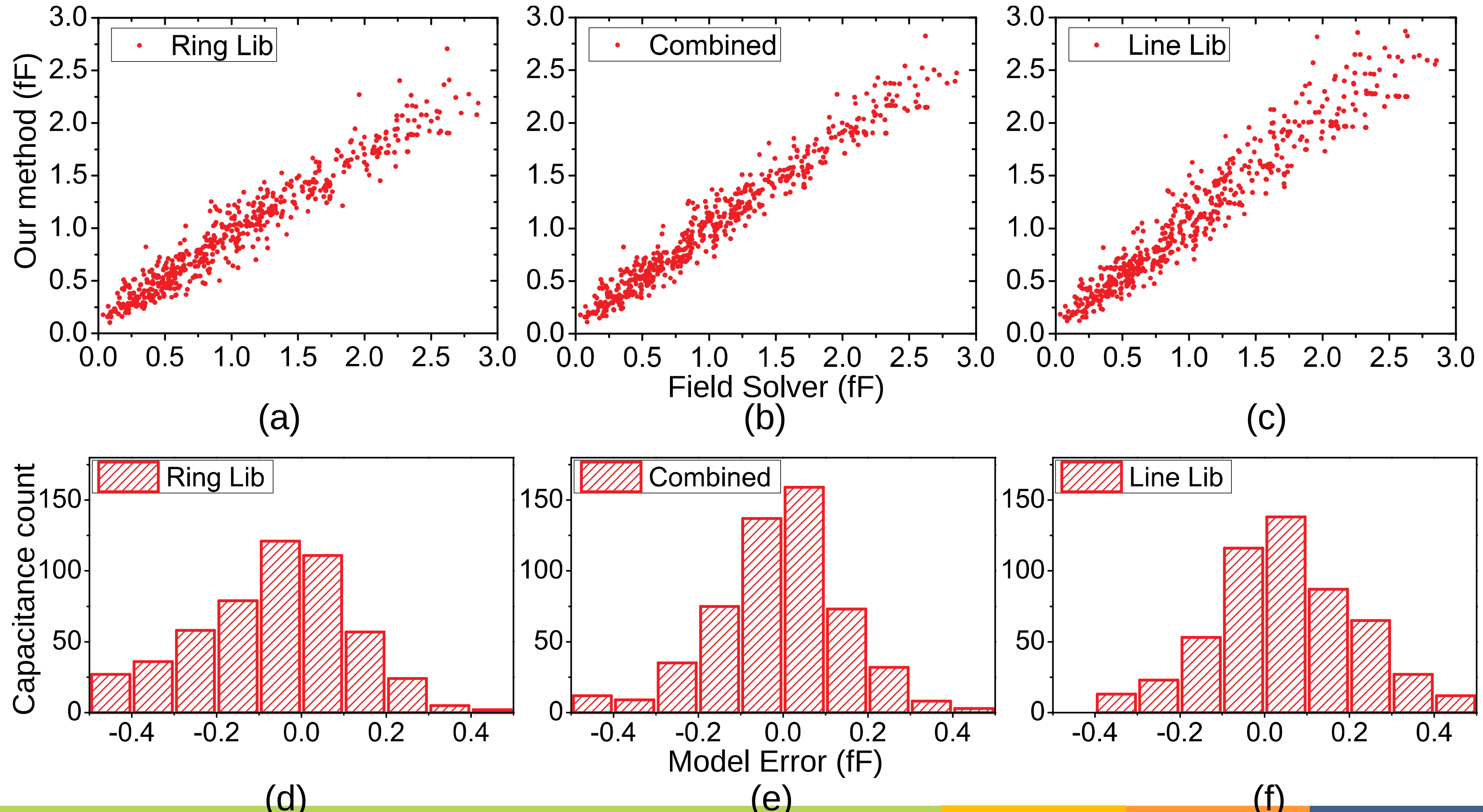
3D IC Design

- **64-point FFT, 47K gates**
- **330 TSVs: 2µm radius, 5um landing pad width, 0.5µm KOZ**



Validation with Full-chip Layout

- **A 2-die FFT64 design (380μm×380μm, 330 TSVs) is used for extraction validation, and the results show that combining both line and ring library is fast and highly accurate**



Validation on Full-chip Layout (cont.)

- **Highly fast and accurate on the full-chip level**
  - **Error is computed against the field solver**

	Field solver	Ring lib	Combined	Line lib
Total cap (fF)	590	538	579	618
Total cap error	-	-8.3%	-1.9%	+5.3%
Correlation coefficient	-	0.971	0.981	0.966
Average error (fF)	-	0.171	0.112	0.163
	Field solver	**Line lib**	**Corner lib**	**Ring lib**
Library generation time	-	8h	9h	18h
Runtime	7.5h		5.8s	
Memory space	>500MB		20MB	

Full-chip TSV-to-wire Impact

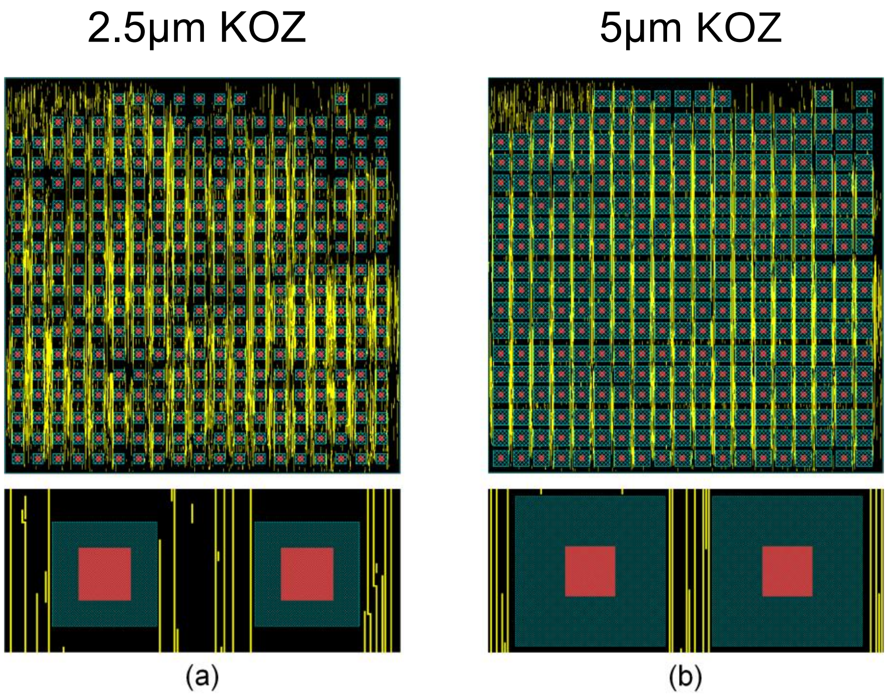
- Multi-TSV models are built for TSV-to-TSV coupling[1]
- STA and statistical power calculation: Primetime
- Worst-case total TSV noise calculation: HSPICE

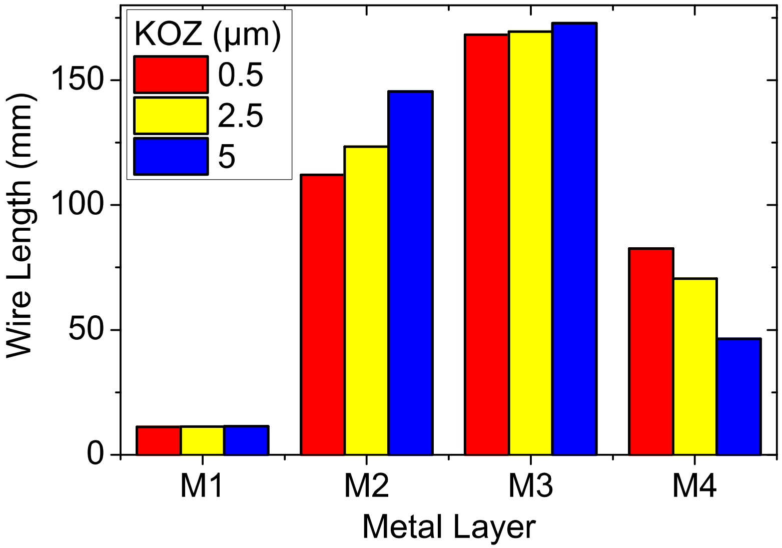
With TSV-to-wire cap?	No	Yes
Total TSV MOS cap (pF)	4.47	
Total TSV-to-TSV coupling cap (pF)	0.74	
Total TSV-to-wire coupling cap (pF)	2.01	
Longest path delay (ns)	4.48	5.08 (+13.4%)
Total TSV net power (mW)	0.303	0.356 (+17.6%)
Total net switching power (mW)	2.42	2.50 (+3.3%)
Total power (mW)	22.9	23.0 (+0.43%)
Total worst-case TSV noise (V)	32.5	78.2 (+104%)

[1] Y. Peng et al, "On Accurate Full-Chip Extraction and Optimization of TSV-to-TSV Coupling Elements in 3D ICs", ICCAD13

Increasing Routing KOZ

- Increase minimum distance allowed for the nearest wire
  - Decrease the number of coupling wires
  - Increase routing congestion on other layers
  - No silicon area overhead

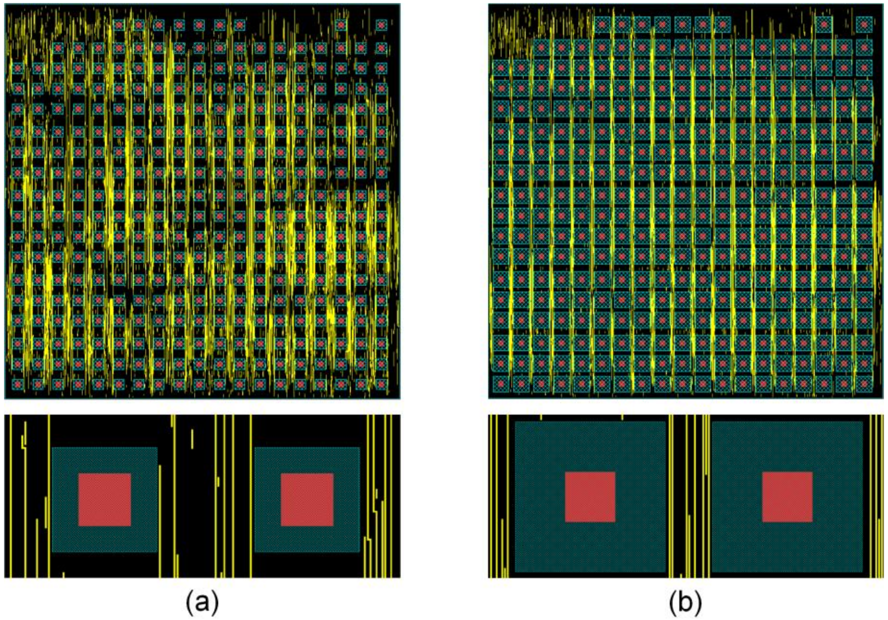




Increasing Routing KOZ (cont.)

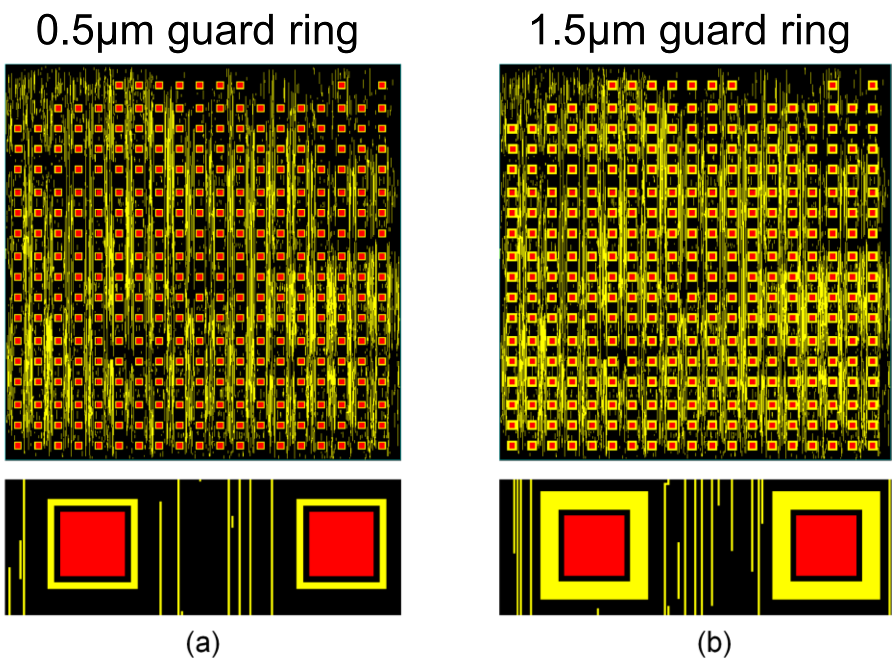
Routing KOZ size (µm)	0	2.5	5
Longest path delay (ns)	5.08	4.95 (-2.6%)	4.77 (-6.1%)
Total TSV net power (mW)	0.356	0.342 (-3.9%)	0.327 (-8.1%)
Total net switching power (mW)	2.50	2.47 (-1.2%)	2.45 (-2.0%)
Total noise on TSV net (V)	78.2	67.0 (-14.3%)	42.9 (-45.1%)

2.5µm KOZ 5µm KOZ



Guard Ring protection

Guard ring width (μm)	0	0.5	1.5
Longest path delay (ns)	4.95	4.98 (+0.6%)	5.01 (+1.2%)
Total TSV net power (mW)	0.342	0.351 (+2.6%)	0.358 (+4.7%)
Total net switching power (mW)	2.47	2.475 (+0.2%)	2.479 (+0.4%)
Total noise on TSV net (V)	67.0	58.0 (-13.4%)	53.6 (-20.0%)



Tech Transfer

- This work is a collaboration with Mentor Graphics
- The project is extended and planned for further technology transfer and we have regular meeting with Mentor Graphics
- This work is first published in DAC14, San Francisco
- It is demonstrated to Mentor, Cadence, Synopsys during company visits
-

Conclusion

- E-field sharing effects need to be considered for accurate TSV-to-wire extraction
- TSV-to-wire coupling has non-negligible impact in full-chip timing, power and TSV noise
- Increasing routing KOZ and using wire guard ring can reduce TSV-to-wire coupling effectively

Thank you!