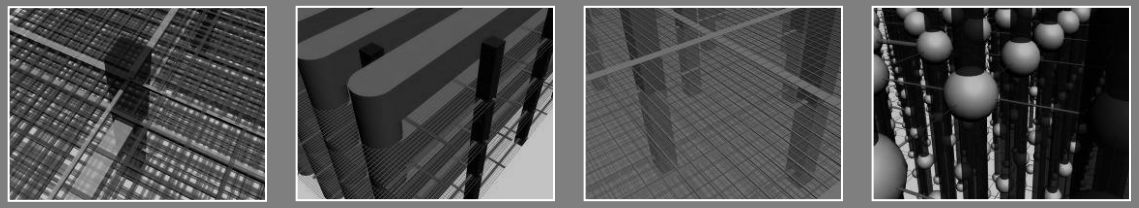
On Accurate Full-Chip Extraction and Optimization of TSV-to-TSV Coupling Elements in 3D ICs



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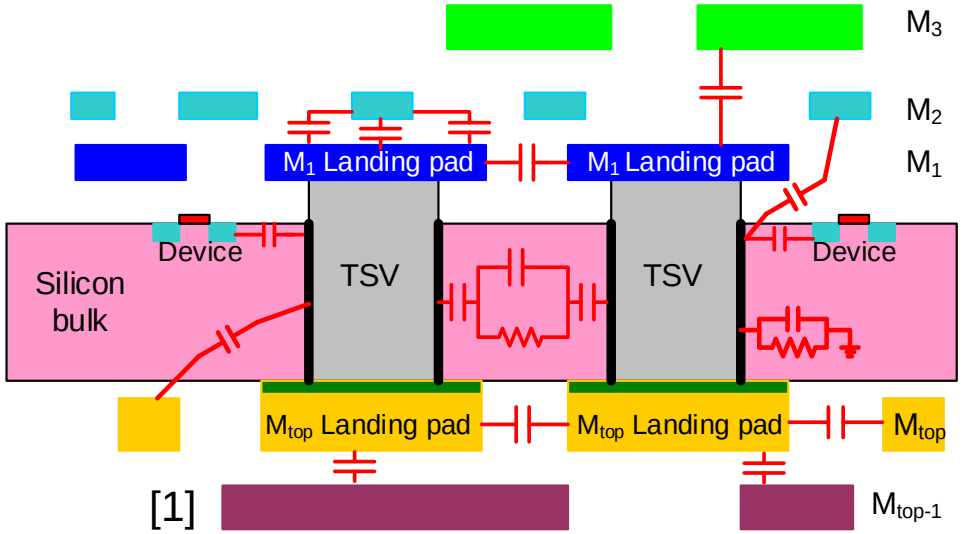
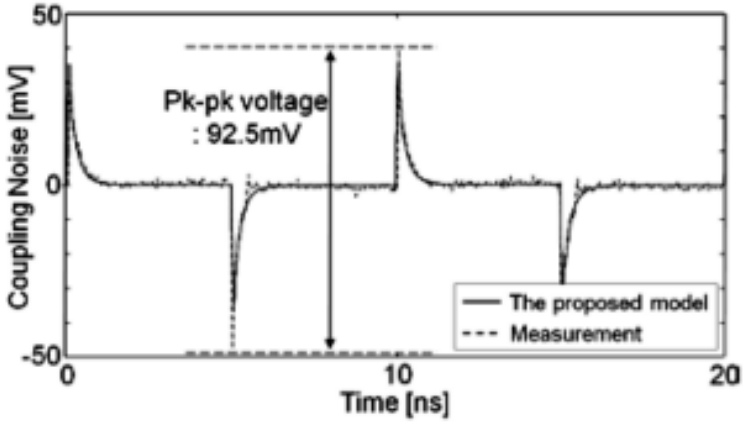
Introduction

- 3D IC using TSV is a potential solution to alleviate interconnect delay and power problems
  - Power and performance benefits from footprint & wirelength reduction
- Previous studies shown that TSV nets have SI issues
  - Large delay, power consumption and noise compared with regular wires
- We need an accurate model for TSV coupling!





Measured TSV coupling noise [2]

[1] C. Liu et al., "Full-chip TSV-to-TSV coupling analysis and optimiza-tion in 3D IC," DAC11
[2] J. Cho et al, "Modeling and Analysis of Through-Silicon Via (TSV) Noise Coupling and Suppression Using a Guard Ring," *CPMT 2011*

Contribution

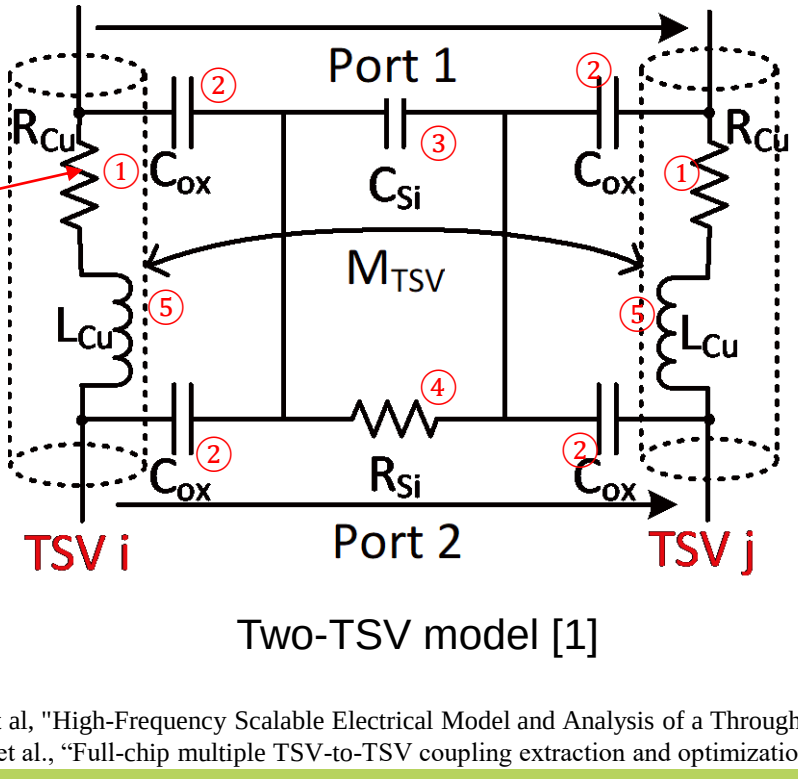
1. Accurate multi-TSV model
   - considers the silicon depletion region, silicon substrate, and E-field distribution effects with minimum components
2. We propose two coupling analysis methods and perform a detailed extraction and analysis on the full-chip design using our multi-TSV model
   - worst-case and average case analysis
3. We studied all the silicon and E-field effects on full-chip level showing impact on TSV coupling
4. We propose a guard-ring protection for TSV coupling noise reduction and study its impact on full-chip design

Traditional Two-TSV Model

First, we introduce the traditional 2-TSV model for TSV-to-TSV coupling used in many previous works

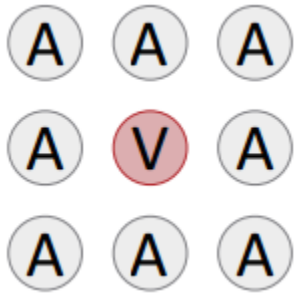
- **Traditional TSV coupling model considers physical TSV structure and its parasitic components**
- **Accurate in two-TSV cases, but not enough for multiple-TSV**

This model is accurate in a TSV pair case compared to the measurement data. But they lack accuracy in multiple TSV case.



Two-TSV model [1]

2-TSV model = 1x ⑥



Field-solver =1.99x ⑦
2-TSV model = 8x [2]

[1] J. Kim et al, "High-Frequency Scalable Electrical Model and Analysis of a Through Silicon Via (TSV)," CPMT 11
[2] T. Song et al., "Full-chip multiple TSV-to-TSV coupling extraction and optimization in 3D ICs," DAC13

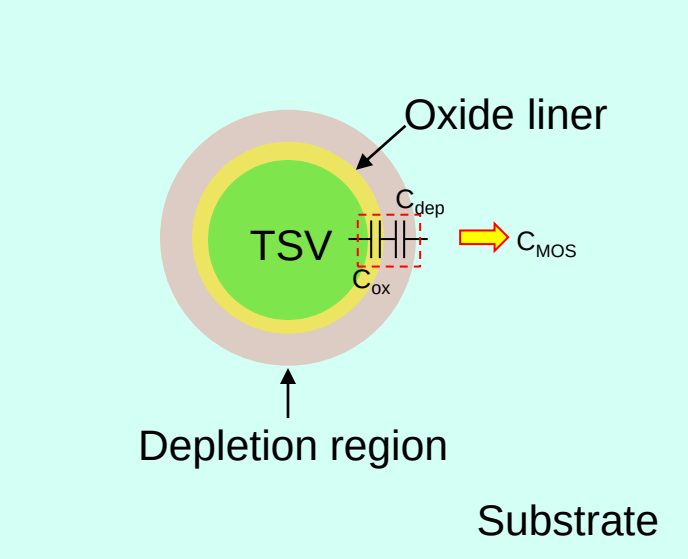
TSV-induced Silicon and Field Effects

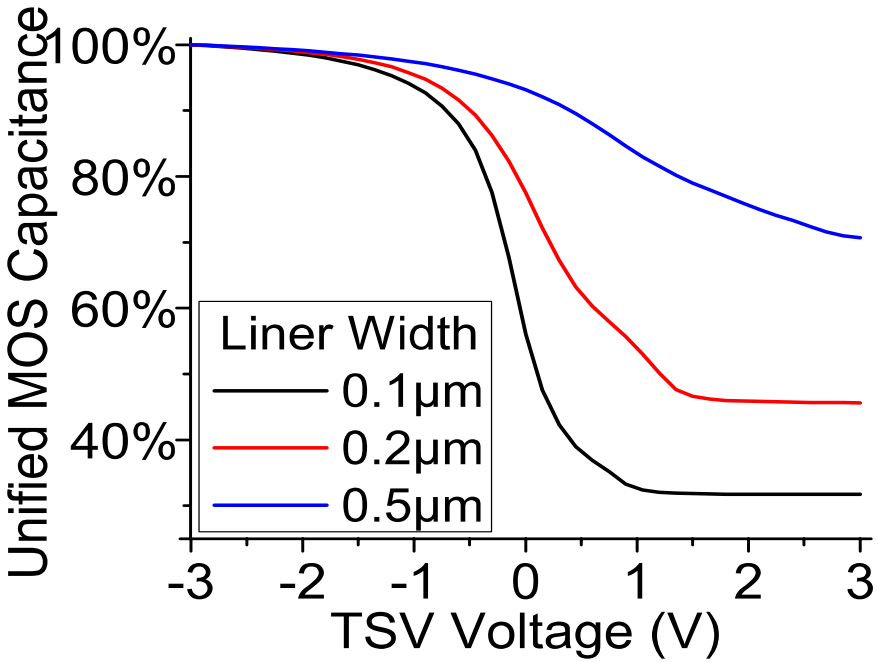
- **Traditional model failed to consider some important TSV impacts**

- **Silicon effects**
  - **TSV-induced depletion region**
  - **Finite silicon substrate capacitance and resistance**
- **Field effects**
  - **Electrical field (E-field) distribution**

TSV Depletion Region Effects

- **TSV-liner-silicon form a MOS capacitor which introduces a voltage-dependent capacitor**

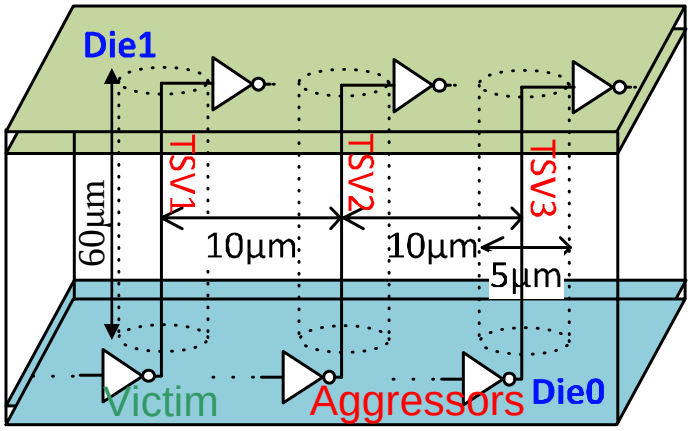




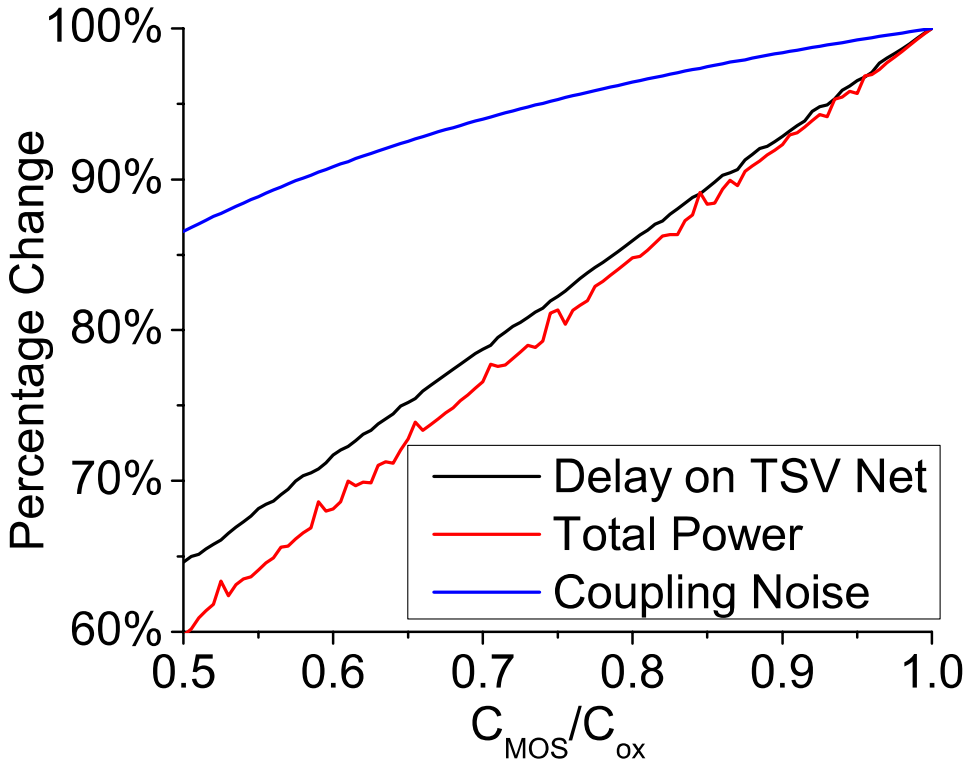
High-frequency CV curve of TSV, with substrate doping of $10^{15}/cm^3$

TSV Depletion Region Effects (cont.)

- **Ignoring the depletion region introduces over-estimation on TSV-induced delay, power and noise**



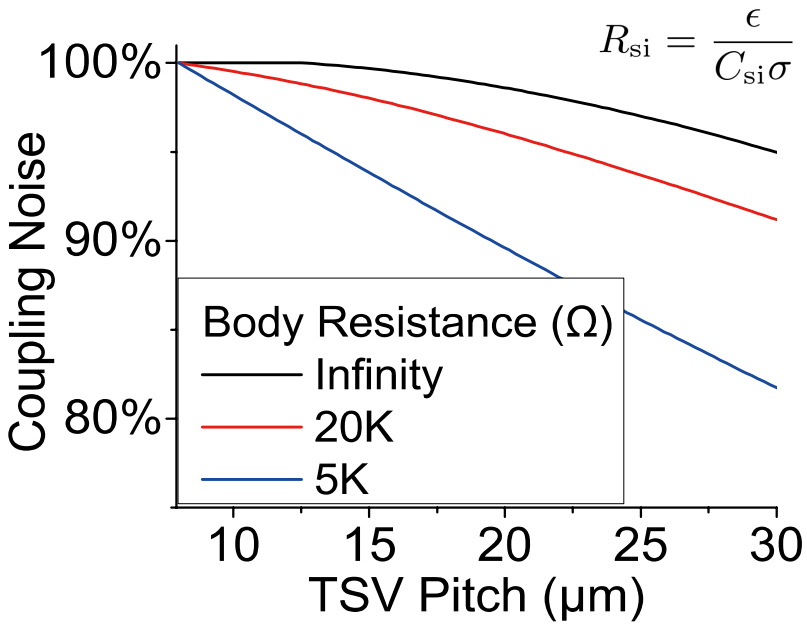
3-TSV Test Structure

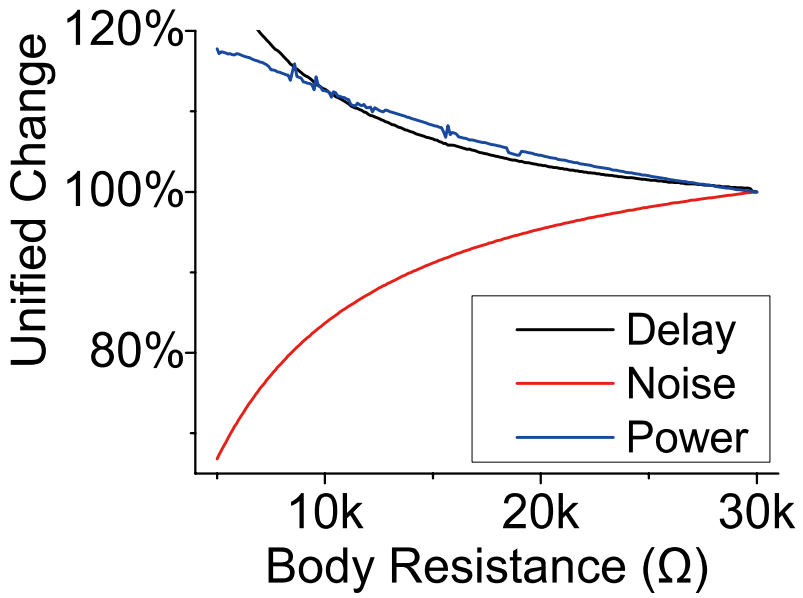


Impact of depletion capacitance (Sentaurus)

Silicon Substrate Effects

- **Doped silicon substrate introduces finite resistance and capacitance from TSV to the ground**
- **Ignoring substrate effects over-estimates the coupling noise while under-estimates TSV induced delay and power**

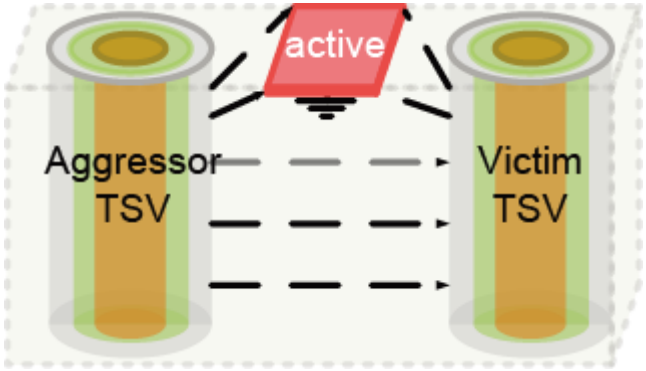




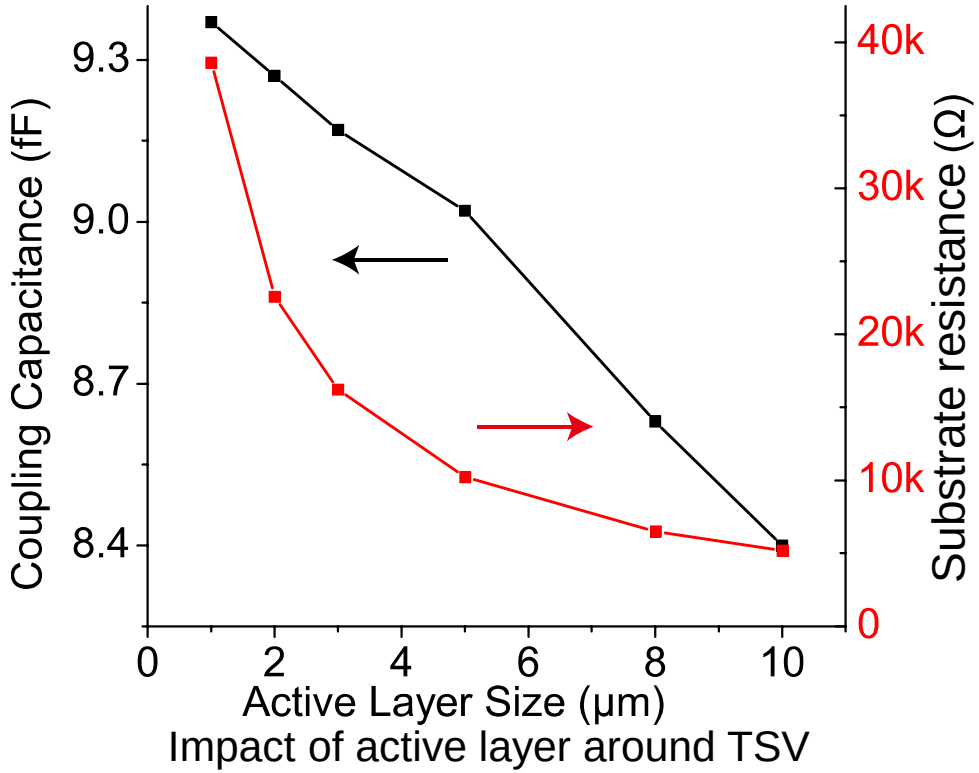
Impact of substrate resistance and capacitance

Silicon Substrate Effects (cont.)

- **The active region around TSV further reduces the coupling between TSVs but it introduce larger body capacitance**



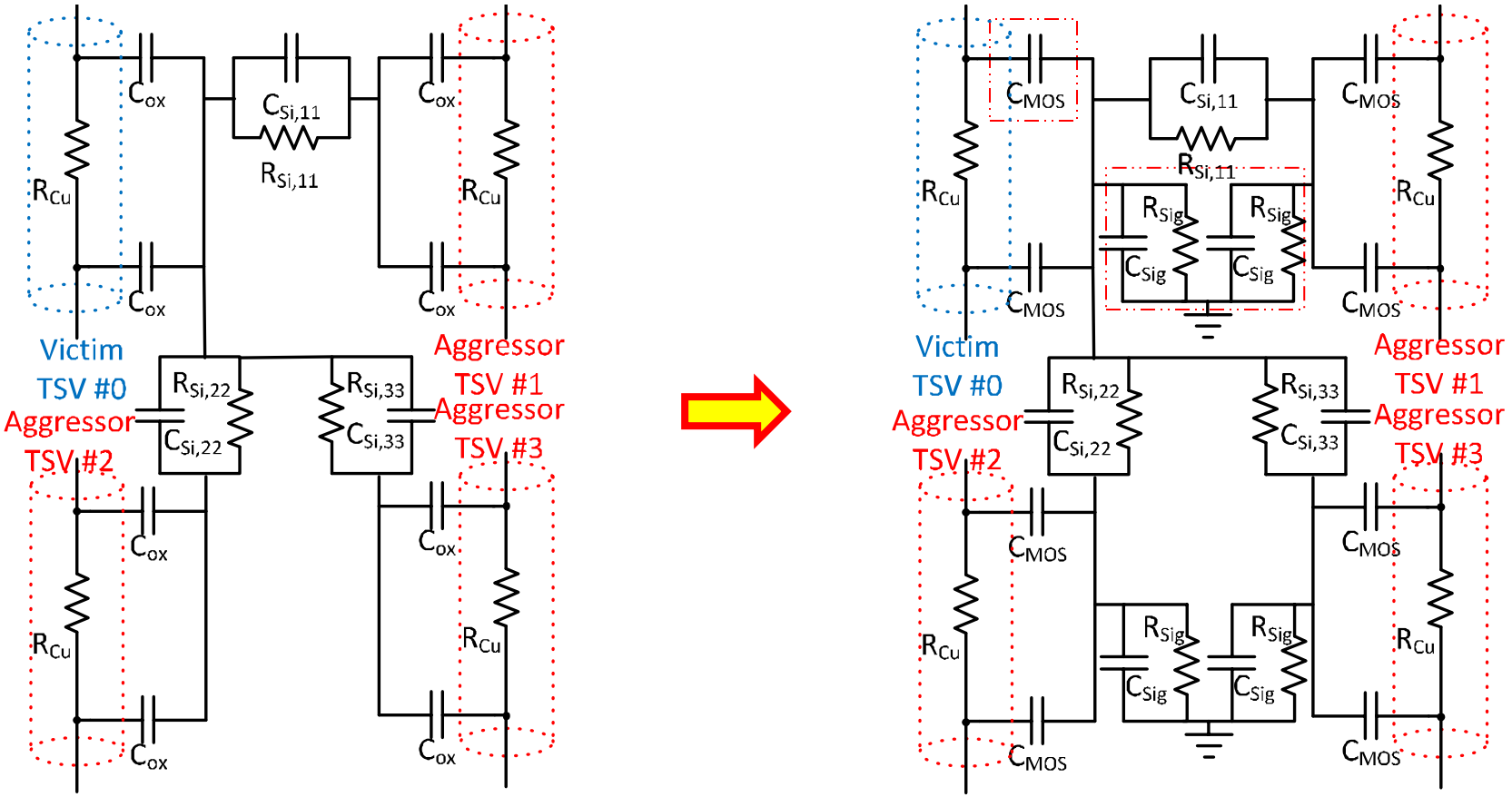
active area around TSV shares E-field



Impact of active layer around TSV

TSV Depletion Region Effects (cont.)

- **Multi-TSV model with deletion and substrate effects considered**



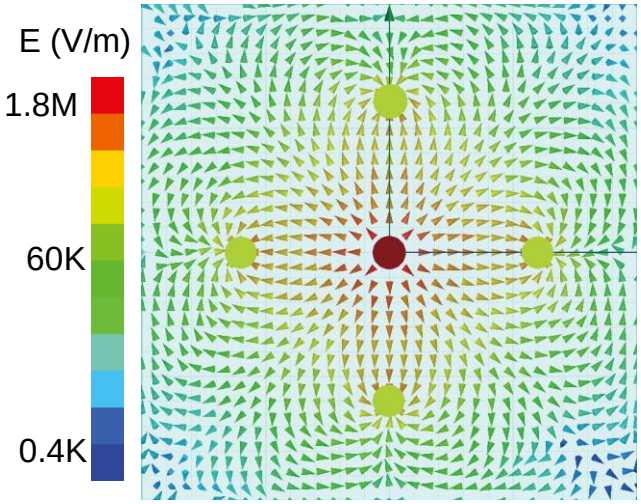
Multi-TSV model in [1]

TSV model with depletion and substrate effect

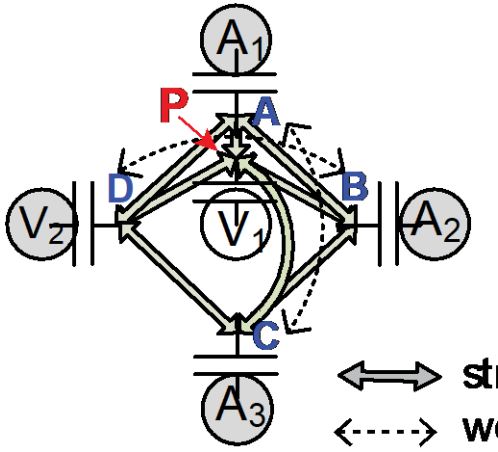
[1] T. Song et al., "Full-chip multiple TSV-to-TSV coupling extraction and optimization in 3D ICs," DAC13

E-field Distribution Effects

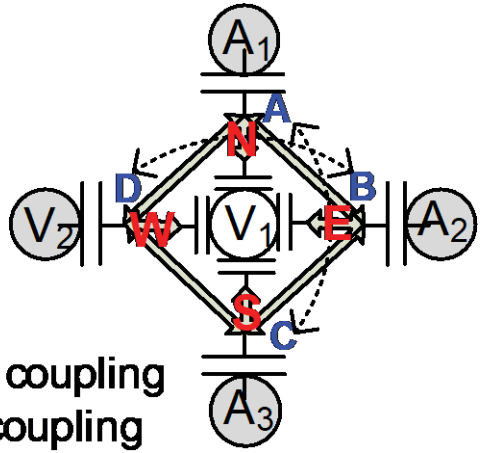
- **E-field are distributed among each side of victim TSV, using a single node for all field introduces stronger TSV-coupling path through the common node**



E-field distribution around TSV



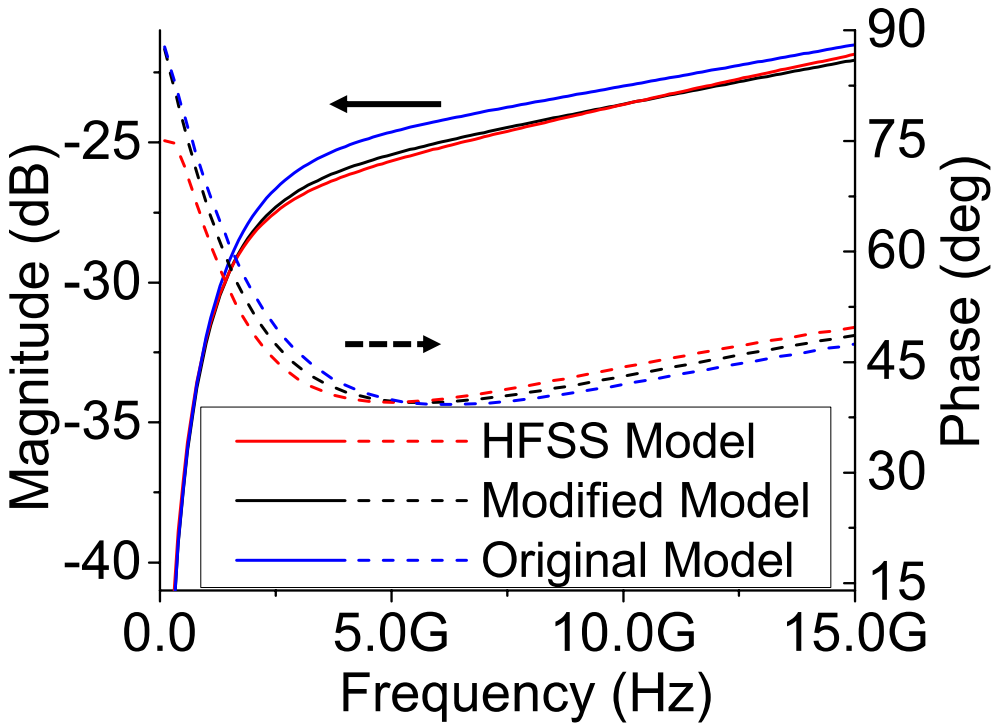
Traditional model



This work

E-field Distribution Effects (cont.)

- **HFSS field solver shows the over-estimation on coupling noise without considering E-field distribution effects**



Model comparison in coupling noise

Full-chip Analysis

- **Why full-chip analysis is necessary?**
  - **Critical path delay**
  - **SI related issues especially for critical nets, e.g. clock and power nets**
  - **Guide to P&R tool**
- **What model to use?**
  - **SPICE model: accurate but slow, for noise analysis**
  - **Primetime model: simplified from SPICE, for STA analysis on delay & power**

Primetime Model

- **Inductance impact is negligible within 5GHz target frequency range**

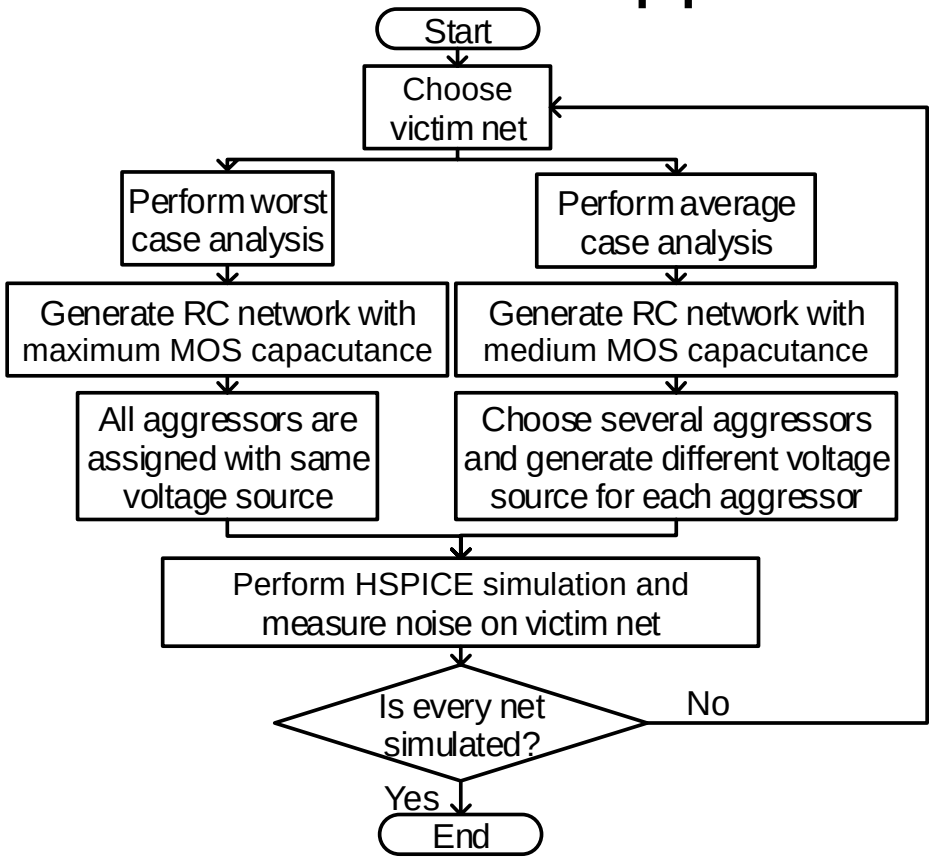
	No TSV coupling	No inductor	With both
Rise delay (ps)	22.63	168.06	168.05
Fall delay (ps)	11.92	108.96	108.88
Power (μW)	3.47	21.059	21.058
Peak noise (mV)	0	27.64	27.06

- **Ignoring silicon capacitance is a better choice for Primetime**

Body resistance (Ω)		1K	5K	10K
Multi-TSV model	Power (μW)	96.32	93.64	89.65
	Delay (ps)	45.5	40.0	39.1
No silicon cap	Power (μW)	93.64	93.67	89.87
	Delay (ps)	45.7	39.7	38.6
No MOS cap	Power (μW)	70.24		
	Delay (ps)	37.7		

Full-chip Analysis Flow

- **Extract SPICE model for each TSV net and measure noise level**
- **Extract Primetime SPEF file for full-chip power and delay analysis**

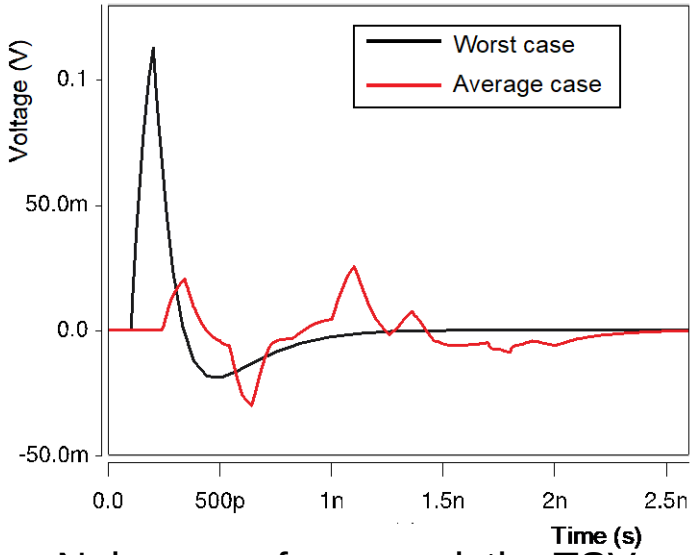


Noise SPICE simulation flow

Full-chip Analysis Strategy

- **Worst case vs. average case comparison**

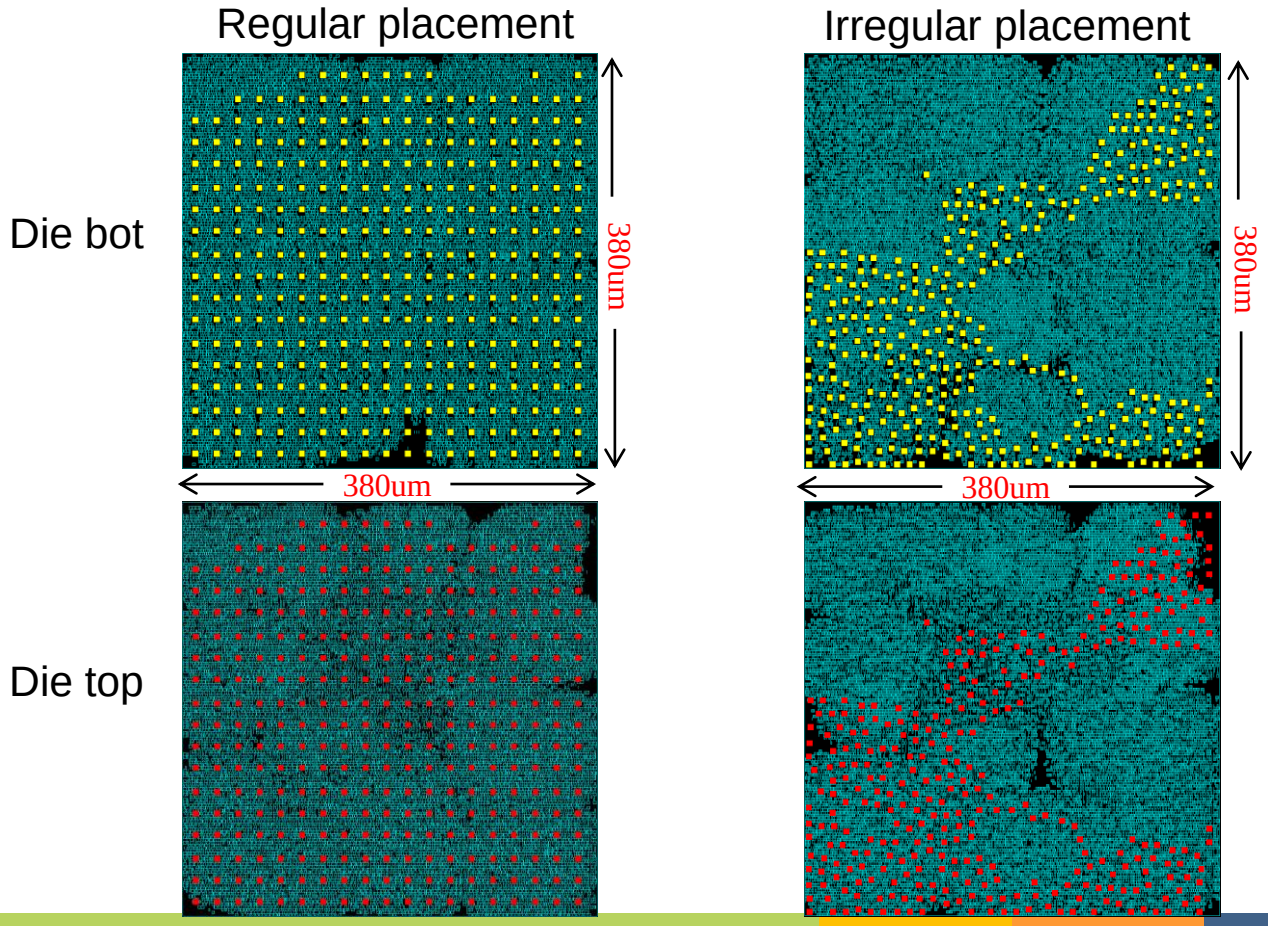
	Worst case	Average case
Signal arrive time	Start of each period	Randomly chosen in a period
Aggressor signal activity	1	From 0 to 1
Aggressor switching direction	Only rise	Both rise and fall
Noise measurement	Maximum voltage	Peak-to-peak voltage



Noise waveform on victim TSV net

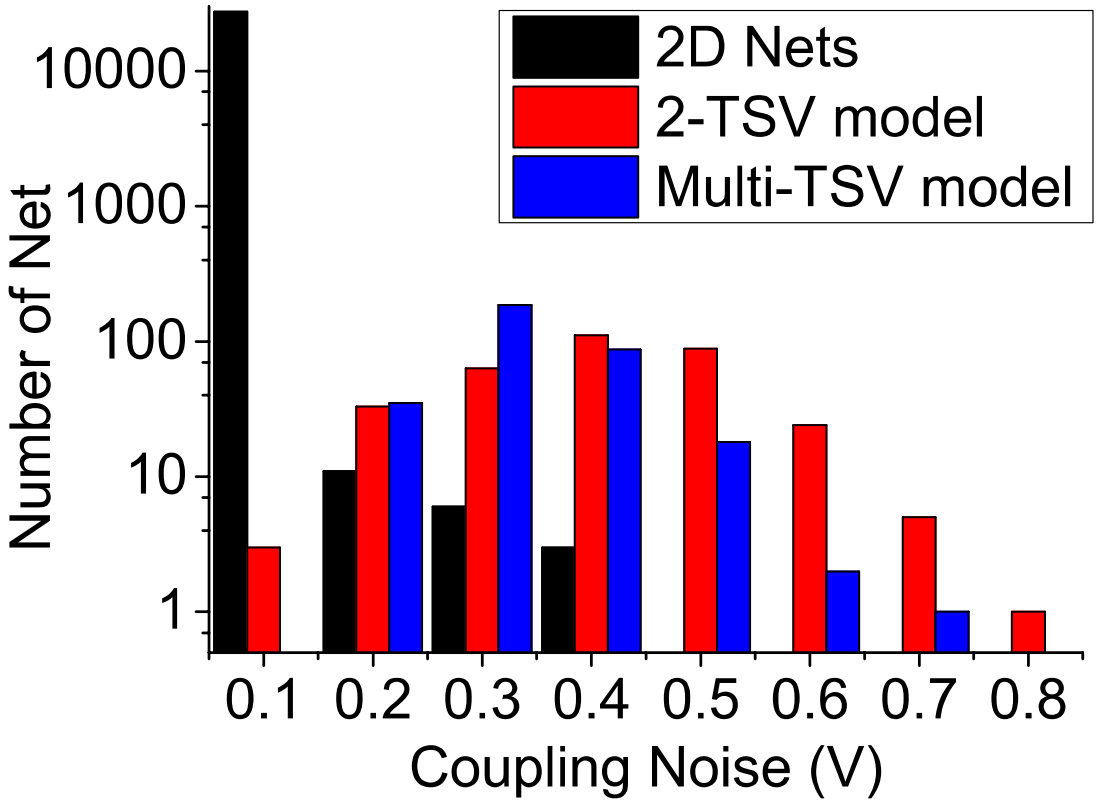
3D IC Design

- **64-point FFT, 47K gates**
- **330 TSVs: 2μm radius, 5um landing pad width, 1um KOZ**



Model Comparison in Full Chip

- **2-TSV model over-estimates noise on TSV net**



Full-chip Analysis Result

- **Aggressor activity, slew and signal arrival time affect TSV noise**

	Activity	Slew (ns)	Total TSV net noise on irregular design (V)	Total TSV net noise on regular design (V)
Average case	0.2	0.1	26.51	24.65
	0.2	0.5	14.04	14.62
	0.5	0.1	39.61	35.37
Worst case	1.0	0.1	139.01	132.44

Full-chip Analysis Result (cont.)

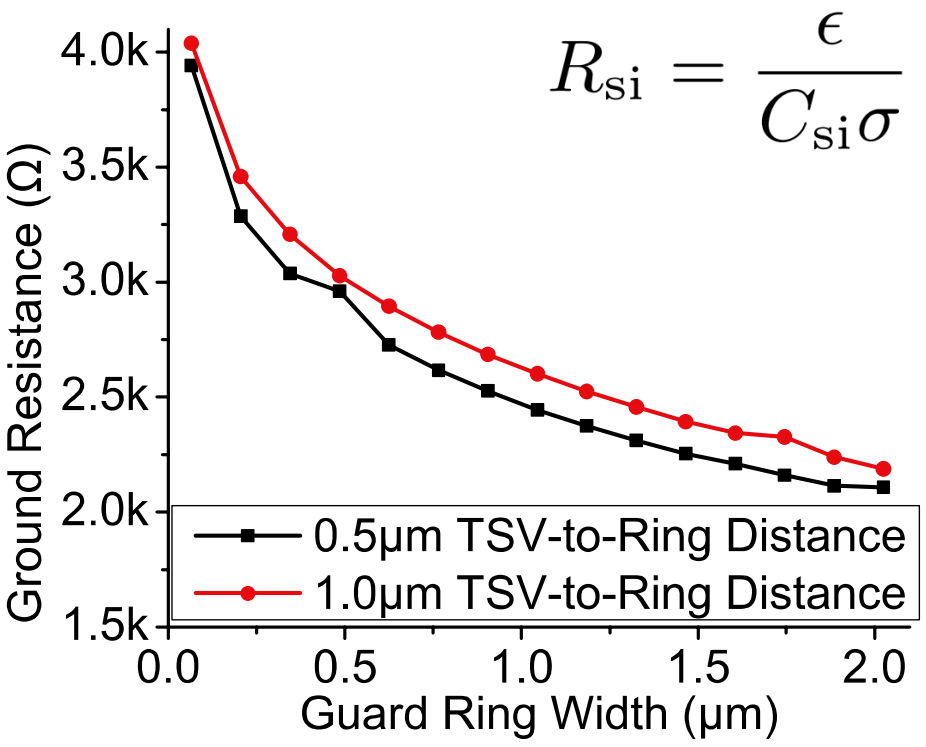
- **TSV coupling effects on fullchip timing, power and noise***
- **Irregular design suffers more from noise, but it gives potential opportunity for optimization**

Placement style	Irregular			Regular		
	Timing (ns)	Power (μW)	Noise (V)	Timing (ns)	Power (μW)	Noise (V)
No depletion region	0.85	13.53	153.7	0.98	13.66	145.9
No body resistance	0.78	12.54	145.9	0.98	13.66	138.9
No E-field distribution	0.79	12.68	146.3	0.91	12.77	138.9
All effects	0.79	12.68	139.0	0.91	12.77	132.4

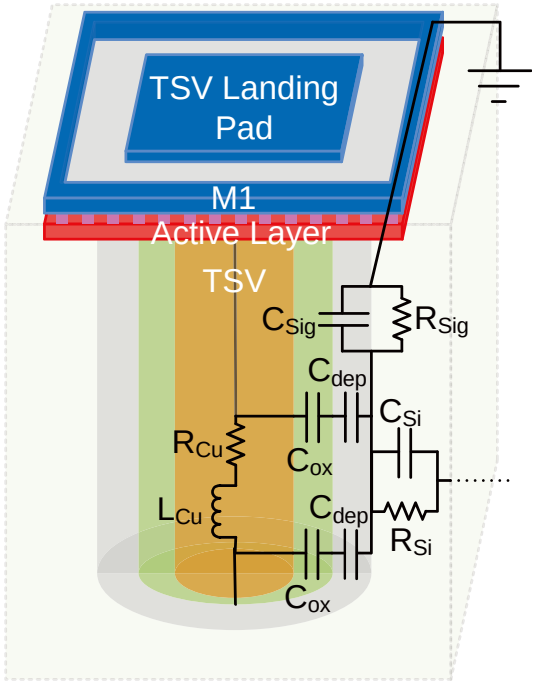
***Timing is measured by longest path delay increase due to TSV coupling, Power and Noise is measured for all TSVs**

Optimization Using Guard Ring

- **Guard ring using active region helps reducing TSV coupling by stronger connection from substrate to ground**



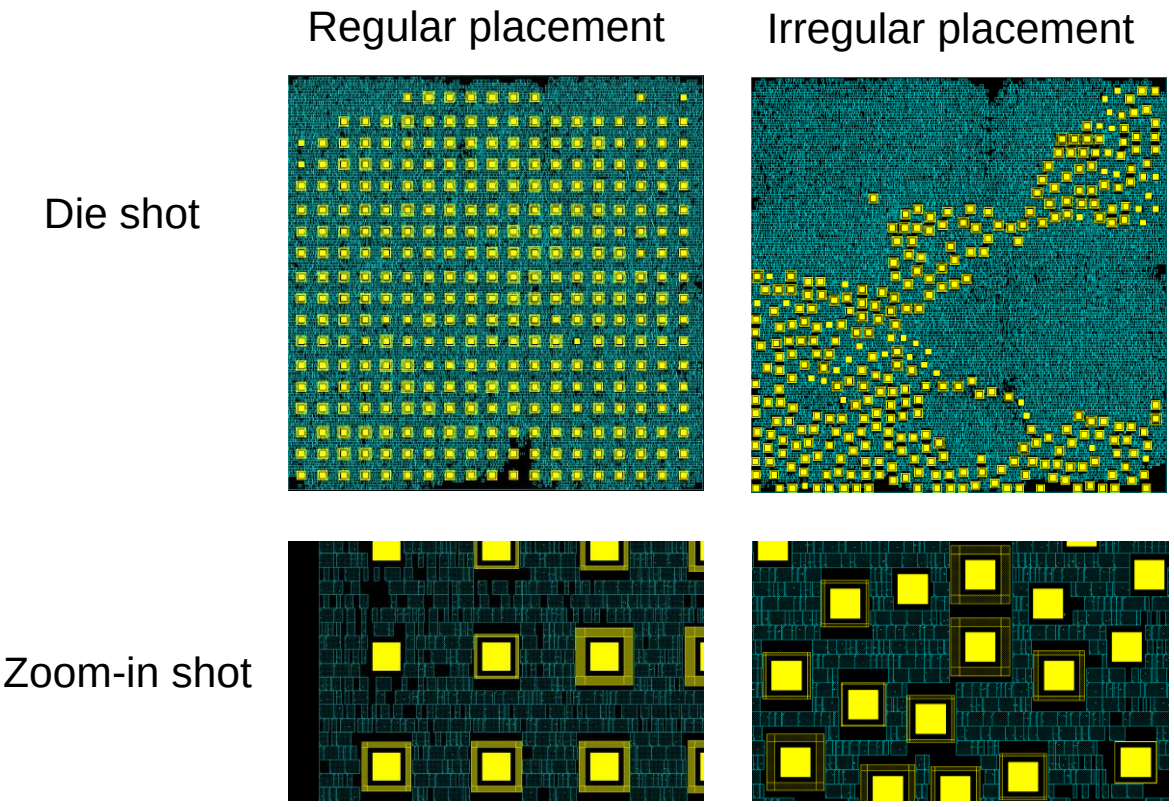
Guard ring size impact (Raphael)



TSV model with guard ring

Optimization Using Guard Ring

- **Add a guard ring in diffusion layer according to the noise level to balance area overhead and coupling noise on TSV net**



Guard Ring Optimization Result

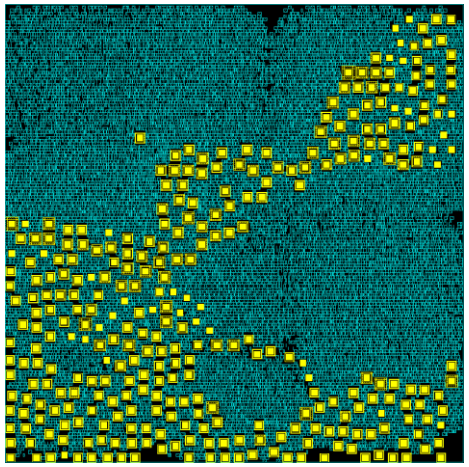
- **Guard ring reduces noise effectively at small delay overhead**

	Irregular	Regular
Total TSV noise wo/ guard ring (V)	139.0	132.4
Total TSV noise w/ guard ring (V)	101.1	96.5
TSV noise reduction	27.3%	27.1%
Guard ring induced LPD increase (ns)	0.02	0.02
Guard ring induced power increase(μW)	0.07	0.09

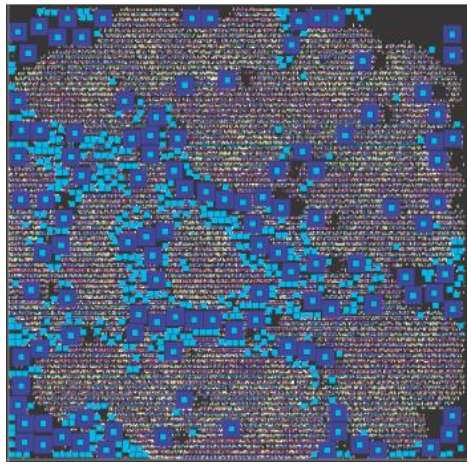
Guard Ring vs. TSV Shielding

- **Guard ring uses very small placement area**

Guard Ring



TSV shielding in [1]



	Guard ring	TSV shielding [1]
Protected TSV	298/330	118/548
Area of original TSV (μm^2)	49	49
Area of guarded TSV (μm^2)	68.9 to 121	361
Total TSV noise reduction	27.3%	42.04%
Total area overhead	7.65%	26.4%

[1] C. Liu et al., "Full-chip TSV-to-TSV coupling analysis and optimiza-tion in 3D IC," DAC11

Conclusion

- Multi-TSV model is needed for accurate TSV parasitic extraction
- Substrate and E-field effects need to be considered in TSV model
- TSV MOS cap is the major component for TSV-induced delay and coupling
- Worse case analysis gives largest coupling noise while average case study flow gives closer analysis to realistic case
- Guard ring protection can reduce TSV net noise with slight area & delay overhead

Thank you !