Prof. Yarui Peng

227 N. Harmon Ave.
Fayetteville, AR, 72701

yrpeng@uark.edu
(479) 575-6043

Education

Georgia Institute of Technology, Atlanta, Georgia Aug. 2012 – Dec. 2016

Ph.D. in School of Electrical & Computer Engineering Dec. 2016
Advisor: Professor Sung Kyu Lim
Thesis: "CAD Tools and Methodologies for Reliable 3D IC Design, Analysis, and Optimization"

M.S. Degree in Electrical & Computer Engineering May 2014
Advisor: Prof. Sung Kyu Lim

National University of Singapore, Singapore Jan. 2011 – May 2011

Exchange Student in Electrical & Computer Engineering

Tsinghua University, Beijing, China Aug. 2008 – July 2012

B.S. Degree in Microelectronic Engineering July 2012
Advisor: Prof. Liyang Pan
Thesis: "A Non-Volatile Random-Access Memory (NVRAM) Fabricated in a Standard CMOS Logic Process"

Experience

Assistant Professor, University of Arkansas, Fayetteville, AR Jan. 2017 – Present

Summer Intern, Mentor Graphics, Fremont, CA May. 2016 – Aug. 2016

"Parasitic extraction for Fan-Out Wafer-Level-Packaging 2.5D IC"

- Designed CAD flow for TSMC InFO RC extraction with Calibre xACT and Hyperlynx
- Performed experiments on inductive coupling impacts study in InFO structures

Summer Intern, Mentor Graphics, Fremont, CA May 2015 – Aug. 2015

- Designed extraction CAD flow with Calibre xACT/xRC tools and performed extraction, simulation, and analysis
- Worked with Global Foundry, IME, and Qualcomm to help build custom flows for 3D IC extraction

Graduate Teaching Assistant, Georgia Institute of Technology, Atlanta, GA Jan. 2016 – Dec. 2016

Graduate Research Assistant, Georgia Institute of Technology, Atlanta, GA Aug. 2012 – Dec. 2016

"Parasitic Extraction and Analysis for 2.5D InFO Fanout WLP Package" *with Mentor Graphics and TSMC, CA*

- Designed Multi-die 2.5D InFO WLP benchmarks for analysis
- Designed CAD tools and flows for RLGC parasitic extraction combining both die and package layout

"Parasitic Extraction in Face-to-face-bonded 3D ICs" *with Mentor Graphics and Qualcomm, CA*

- Designed die-by-die, holistic, and in-context extraction CAD flows for face-to-face-bonded 3D ICs
- Designed 3D ICs in 45nm, 28nm, 14nm and 7nm and performed full-chip analysis across multiple nodes

"Parasitic Extraction in TSV-based 3D ICs" *with Mentor Graphics, CA*

- Designed parasitic extraction tools for TSV parasitics in C++, Perl, and shell scripts
- Designed 3D ICs and performed full-chip analysis and optimization for TSV-to-TSV and TSV-to-wire coupling

"Architecture-aware Power Distribution Network Design for Wide-I/O 3D DRAM" *with Samsung, Korea*

- Designed CAD tools and models for 3D DRAM IR-drop analysis
- Performed design, packaging, and architectural-level optimization for 3D DRAM

"Thermal Analysis and Optimization for 3D Low-power OpenSPARC T2 Design" *with Intel, CA*

- Performed thermal analysis and optimization for OpenSPARC T2 on core and full-chip levels

"Sub-vt 3D IC Design for Ultra-Low Power Wireless Sensor Network" *with CISS, Korea*

- Co-designed a sub-vt cell library and an 8052 processor in 0.4V/0.8V supply voltage

Research Internship Program, Tsinghua University, Beijing, China July 2011 – Aug. 2011

"Verification of DSP Level 1 Program Cache"

- Designed Verilog test bench and performed verification for a DSP L1 cache using Synopsys VCS

Research Training Program, Tsinghua University, Beijing, China Mar. 2010 – June 2011

"Design and Development of the Energy-harvesting System and Its Energy Management Circuit"

- Co-designed a simulation model in MATLAB for an electrostatic energy harvester

"Development of Virtual Oscilloscope Based on FPGA"

- Designed a virtual oscilloscope in VHDL and implemented it using Altera FPGA

Publications

Refereed Journals

[01] **Yarui Peng**, Taigon Song, Dusan Petranovic, and Sung Kyu Lim, "Silicon Effect-aware Full-chip Extraction and Mitigation of TSV-to-TSV Coupling," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 33, no. 12, pp.1900-1913, Dec. 2014

[02] Sandeep Samal, **Yarui Peng**, Mohit Pathak, and Sung Kyu Lim, "Ultra-Low Power Circuit Design with Sub/Near-Threshold 3D IC Technologies," IEEE Transactions on Components, Packaging, and Manufacturing Technology, vol.5, no.7, pp.980-990, July 2015

[03] **Yarui Peng**, Dusan Petranovic, and Sung Kyu Lim, "Multi-TSV and E-Field Sharing Aware Full-chip Extraction and Mitigation of TSV-to-wire Coupling," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol.34, no.12, pp.1964-1976, Dec. 2015

[04] Moongon Jung, Taigon Song, **Yarui Peng**, and Sung Kyu Lim, "Fine-Grained 3D IC Partitioning Study with A Multi-Core Processor," IEEE Transactions on Components, Packaging, and Manufacturing Technology, vol.5, no.10, pp.1393-1401, Oct. 2015

[05] Taigon Song, Chang Liu, **Yarui Peng**, and Sung Kyu Lim, "Full-Chip Signal Integrity Analysis and Optimization of 3D ICs," IEEE Transactions on Very Large Scale Integration Systems, vol. 24, no. 5, pp. 1636-1648, May 2016.

[06] Can Rao, Tongqing Wang, **Yarui Peng**, Jie Cheng, Yuhong Liu, Sung Kyu Lim and Xinchun Lu, "Residual Stress and Pop-Out Simulation for TSVs and Contacts in Via-Middle Processing", IEEE Transactions on Semiconductor Manufacturing, vol. 30, no. 2, pp. 143-154, May 2017.

[07] **Yarui Peng**, Taigon Song, Dusan Petranovic and Sung Kyu Lim, "Parasitic Extraction for Heterogeneous Face-to-face Bonded 3-D ICs", In IEEE Transactions on Components and Packaging and Manufacturing Technology, vol. 7, no. 6, pp. 912–924, Jun 2017.

[08] Moongon Jung, Taigon Song, **Yarui Peng** and Sung Kyu Lim, "Design Methodologies for Low-power 3-D ICs with Advanced Tier Partitioning", In IEEE Transactions on Very Large Scale Integration Systems, vol. 25, no. 7, pp. 2109-2117, Jul 2017.

[09] **Yarui Peng**, Dusan Petranovic, Kambiz Samadi, Pratyush Kamal, Yang Du and and Sung Kyu Lim, "Inter-die Coupling Extraction and Physical Design Optimization for Face-to-face 3D ICs", In IEEE Transactions on Nanotechnology, vol. 17, no. 4, pp. 634–644, Jul 2018.

[10] Tristan Evans, Quang Le, Shilpi Mukherjee, Imam Al Razi, Tom Vrotsos, **Yarui Peng**, and H. Alan Mantooth, "Powersynth: A Power Module Layout Generation Tool", IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5063–5078, Jun 2019, ***Highlighted Paper***.

[11] Kevin Hermanns, **Yarui Peng**, and H. Alan Mantooth, "The Increasing Role of Design Automation in Power Electronics: Gathering What Is Needed", IEEE Power Electronics Magazine, vol. 7, no. 1, pp. 46-50, Mar 2020.

[12] **Yarui Peng**, Quang Le, Imam Al Razi, Shilpi Mukherjee, Tristan Evans, and H. Alan Mantooth, "PowerSynth Progression on Layout Optimization for Reliability and Signal Integrity", IEICE Nonlinear Theory and Its Applications, vol. 11, no. 2, pp. 124-144, Apr 2020, ***Invited Paper***.

Refereed Conferences

[01] Taigon Song, Chang Liu, **Yarui Peng**, and Sung Kyu Lim, "Full-Chip Multiple TSV-to-TSV Coupling Extraction and Optimization in 3D ICs," ACM Design Automation Conference, 2013

[02] Taigon Song, Chang Liu, **Yarui Peng**, and Sung Kyu Lim, "Full-Chip Multiple TSV-to-TSV Coupling Extraction and Optimization in 3D ICs," SRC TECHCON Conference, 2013

[03] Sandeep Samal, **Yarui Peng**, Yang Zhang, and Sung Kyu Lim, "Design and Analysis of Ultra Low Power Processors Using Sub/Near-Threshold 3D Stacked ICs," International Symposium on Low Power Electronics and Design, 2013

[04] **Yarui Peng**, Taigon Song, Dusan Petranovic, and Sung Kyu Lim, "On Accurate Full-Chip Extraction and Optimization of TSV-to-TSV Coupling Elements in 3D ICs," IEEE International Conference on Computer-Aided Design, 2013

[05] Sandeep Samal, **Yarui Peng**, and Sung Kyu Lim, "Design and Analysis of Ultra Low Power Processors Using Sub/Near-Threshold 3D Stacked ICs," SRC TECHCON Conference, 2014

[06] **Yarui Peng**, Dusan Petranovic, and Sung Kyu Lim, "Fast and Accurate Full-chip Extraction and Optimization of TSV-to-Wire Coupling," SRC TECHCON Conference, 2014. ***Best in Session Award***

[07] Moongon Jung, Taigon Song, Yang Wan, **Yarui Peng**, and Sung Kyu Lim, "On Enhancing Power Benefits in 3D ICs: Block Folding and Bonding Styles Perspective," ACM Design Automation Conference, 2014

[08] **Yarui Peng**, Dusan Petranovic, and Sung Kyu Lim, "Fast and Accurate Full-chip Extraction and Optimization of TSV-to-Wire Coupling," ACM Design Automation Conference, 2014

[09] **Yarui Peng**, Bon Woong Ku, Younsik Park, Kwang-Il Park, Seong-Jin Jang, Joo Sun Choi, and Sung Kyu Lim, "Design, Packaging, and Architectural Policy Co-Optimization for DC Power Integrity in 3D DRAM," ACM Design Automation Conference, 2015

[10] **Yarui Peng**, Moongon Jung, Taigon Song, Yang Wan, and Sung Kyu Lim, "Thermal Impact Study of Block Folding and Face-to-Face Bonding in 3D IC," IEEE International Interconnect Technology Conference, 2015

[11] Taigon Song, Moongon Jung, Yang Wan, **Yarui Peng**, and Sung Kyu Lim, "3D IC Power Benefit Study Under Practical Design Considerations," IEEE International Interconnect Technology Conference, 2015

[12] **Yarui Peng**, Taigon Song, Dusan Petranovic, and Sung Kyu Lim, "Full-chip Inter-die Parasitic Extraction in Face-to-Face-Bonded 3D ICs," IEEE International Conference on Computer-Aided Design, 2015

[13] Can Rao, **Yarui Peng**, Tongqing Wang, Sung Kyu Lim, and Xinchun Lu, "Investigation of Post-Annealing Stress and Pop-Out in TSV Front-side CMP," IEEE International Conference on Planarization/CMP Technology, 2016. ***Best Student Paper Award***

[14] **Yarui Peng**, Dusan Petranovic and Sung Kyu Lim, "Chip/Package Co-Analysis and Inductance Extraction for Fan-Out Wafer-Level-Packaging", In Conference on Electrical Performance of Electronic Packaging and Systems, 2017.

[15] Quang Le, Tristan Evans, Shilpi Mukherjee, **Yarui Peng**, Tom Vrotsos, H. Alan Mantooth, "Response Surface Modeling for Parasitic Extraction for Multi-Objective Optimization of Multi-Chip Power Modules (MCPMs)", In IEEE Workshop on Wide Bandgap Power Devices and Applications, pp. 323–330, 2017.

[16] **Yarui Peng**, Dusan Petranovic and Sung Kyu Lim, "Die-to-Package Coupling Extraction for Fan-Out Wafer-Level-Packaging", In IEEE Electrical Design of Advanced Packaging and Systems Symposium, 2017. ***Best Paper Award***

[17] Shilpi Mukherjee, Tristan Evans, Balaji Narayanasamy, Quang Le, Asif Imran Emon, Amol Deshpande, Fang Luo, **Yarui Peng**, Steve Pytel, Tom Vrotsos and Alan Mantooth, "Toward Partial Discharge Reduction by Corner Correction in Power Module Layouts", In IEEE Workshop on Control and Modeling for Power Electronics, 2018.

[18] Imam Al Razi, Quang Le, H. Alan Mantooth, and **Yarui Peng**, "Constraint-Aware Algorithms for Heterogeneous Power Module Layout Synthesis and Optimization in PowerSynth", in Proc. IEEE Workshop on Wide Bandgap Power Devices and Applications, pp. 323–330, Oct 2018.

[19] Quang Le, Tristan Evans, **Yarui Peng**, and H. Alan Mantooth, "PEEC Method and Hierarchical Approach Towards 3D Multichip Power Module (MCPM) Layout Optimization", in Proc. IEEE International Workshop on Integrated Power Packaging, pp. 1–6, Apr 2019.

[20] Imam Al Razi, Quang Le, H. Alan Mantooth, and **Yarui Peng**, "Hierarchical Layout Synthesis and Design Automation for 2.5D Heterogeneous Multi-Chip Power Modules", in Proc. IEEE Energy Conversion Congress and Exposition, pp. 2257-2263, Sep 2019.

[21] Tristan Evans, Quang Le, Balaji Narayanasamy, **Yarui Peng**, Fang Luo, and H. Alan Mantooth, "Development of EDA Techniques for Power Module EMI Modeling and Layout Optimization ", in Proc. IMAPS International Symposium on Microelectronics, pp. 193-198, Oct 2019.

[22] Bakhtiyar Md Nafis, Ange Iradukunda, Imam Al Razi, David R. Huitink, and **Yarui Peng**, "System-level Thermal Management and Reliability of Automotive Electronics: Goals and Opportunities in the Next Generation of Electric and Hybrid Electric Vehicles", in Proc. ASME International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems, pp. 1-8, Oct 2019.

[23] Md Arafat Kabir, and **Yarui Peng**, "Chiplet-Package Co-Design For 2.5D Systems Using Standard ASIC CAD Tools", in Proc. Asia and South Pacific Design Automation Conference, pp. 351-356, Jan 2020.

[24] Tristan Evans, Shilpi Mukherjee, **Yarui Peng**, and H. Alan Mantooth, "Electronic Design Automation Tools and Considerations for Electro-Thermo-Mechanical Co-Design of High Voltage Power Modules", (accepted) in Proc. IEEE Energy Conversion Congress and Exposition, pp. 5046-5052, Oct 2020.

[25] Imam Al Razi, Quang Le, H. Alan Mantooth, and **Yarui Peng**, "Physical Design Automation for High-Density 3D Power Module Layout Synthesis and Optimization", (accepted) in Proc. IEEE Energy Conversion Congress and Exposition, pp. 1984-1991, Oct 2020.

[26] Md. Arafat Kabir, and **Yarui Peng**, “Holistic 2.5D Chiplet Design Flow: A 65nm Shared-Block Microcontroller Case Study”, (accepted) in Proc. IEEE International System-on-Chip Conference, 2020.

[27] Shilpi Mukherjee, **Yarui Peng**, and Alan Mantooth, “General Equation to Determine Design Rules for Mitigating Partial Discharge and Electrical Breakdown in Power Module Layouts”, (accepted) in Proc. IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia, 2020.

[28] Md. Arafat Kabir, Dusan Petranovic, and **Yarui Peng**, "Extraction and Optimization for Heterogeneous 2.5D Chiplet-Package Co-Design", (accepted) in Proc. International Conference on Computer-Aided Design, 2020.

Funded Projects

Honor College Faculty Equipment and Technology Grant Oct. 2020 – June 2021

Honors College, University of Arkansas

- Artificial Intelligence and Machine Learning for 2.5D Physical Design Automation in Power Electronics and VLSI ASIC
- Total Budget: $5,000 PI: $5,000

POETS Year 6 Research Project Aug. 2020 – July 2021

NSF Engineering Research Center for Power Optimization for Electro-Thermal Systems (POETS)

- Enhancing and Demonstration of PowerSynth-Integrated Physical Design Flow
- Total Budget: $132,686 Co-PI: $55,548

- Combined Electromigration and Mechanical Failure Risk in Interconnects: The Imminent Threat to Power Package Reliability
- Total Budget: $143,292 Co-PI: $41,016

Honor College Faculty Equipment and Technology Grant Oct. 2019 – June 2020

Honors College, University of Arkansas

- Machine Learning Database Creation and Model Training for Automated Layout Synthesis and Design Optimization
- Total Budget: $5,000 PI: $5,000

POETS Year 5 Research Project Aug. 2019 – July 2020

NSF Engineering Research Center for Power Optimization for Electro-Thermal Systems (POETS)

- Enhancing and Demonstration of PowerSynth-Integrated Physical Design Flow
- Total Budget: $145,000 Co-PI: $55,547

- Integration of Thermomechanical Reliability Enhancing Technologies into High Density Module, with Design for Reliability Layout Optimization Scheme
- Total Budget: $155,000 Co-PI: $26,580

Honor College Faculty Equipment and Technology Grant Oct. 2018 – June 2019

Honors College, University of Arkansas

- To develop a computer-aided-design (CAD) framework for PCM material modeling and simulation
- Total Budget: $5,500 PI: $5,500

CRII: SHF: Design, Extraction, and Optimization of Multi-Chip Fan-Out Wafer-Level-Packaging for Low-Power Heterogeneous Systems July 2018 – June 2021

National Science Foundation

- Design and modeling of a new multi-chip packaging solution that is low cost with superior electrical performance and power efficiency
- Total Budget: $175,000 PI: $175,000

POETS Year 4 Research Project Aug. 2018 – July 2019

NSF Engineering Research Center for Power Optimization for Electro-Thermal Systems (POETS)

- PowerSynth Progression Towards an Infrastructure for Heterogeneous & 3D Modules
- Total Budget: $140,000 Co-PI: $52,352

- Integration of Thermomechanical Reliability Enhancing Technologies into High Density Module, with Design for Reliability Layout Optimization Scheme
- Total Budget: $200,000 Co-PI: $35,099

Silicon Carbide Advanced Packaging of Power Semiconductors II May. 2018–May. 2021

Army Research Laboratory

- High Speed Integrated 15 kV SiC MOSFET Power Module: Architecture, Design, Fabrication, and Testing
- Total Budget: $700,000 Co-PI: $140,000

Honor College Faculty Equipment and Technology Grant Oct. 2017 – June 2018

Honors College, University of Arkansas

- To develop a computer-aided-design (CAD) framework for layout synthesis of power modules
- Total Budget: $5,000 PI: $5,000

POETS Year 3 Research Project Aug. 2017 – July 2018

NSF Engineering Research Center for Power Optimization for Electro-Thermal Systems (POETS)

- PowerSynth Progression Towards an Infrastructure for Heterogeneous & 3D Modules
- Total Budget: $125,000 Co-PI: $8,000

POETS Year 2 Research Project Aug. 2016 – July 2017

NSF Engineering Research Center for Power Optimization for Electro-Thermal Systems (POETS)

- PowerSynth – Layout Synthesis of Power Modules
- Total Budget: $171,345 Co-PI: $8,000

Students Advised

Served as the Ph.D. Advisor

Imam Al Razi

- CSCE Ph.D.
- Started in Aug. 2017

MD Arafat Kabir

- CSCE Ph.D.
- Started in Aug. 2018

Served on the Ph.D. Dissertation Committee

Quang Minh Le

- ELEG Ph.D.

Tristan Evans

- ELEG Ph.D.

Mahsa Montazeri

- MEEG Ph.D.

Balaji Narayanasamy

- ELEG Ph.D.
- Dissertation Title: Conducted EMI Mitigation in Power Converters using Active EMI Filters
- Defended on 7/1/2020

Arman Ur Rashid

- ELEG Ph.D.

Md Maksudul Hossain

- ELEG Ph.D

Andrew Felder

- CSCE Ph.D

Served on the Master Thesis Committee

Sang Yun Kim

- CSCE Master

Tumininu Olatunji

- MEEG Master

Undergraduate Students Advised in NSF POETS REU Projects

John Alumbaugh

- From University of Arkansas, CSCE Major
- POETS Project: Corner Stitch Data Structure with Constraint Graph Methodology — Summer 2017

Aijalon Kilpatrick

- From University of Miami, EE Major
- POETS Project: Machine Learning Model Calibration for High-Density Power Systems — Summer 2019

Shayne Erickson

- From Clemson University, Math Major
- POETS Project: Machine Learning Model Calibration for High-Density Power Systems — Summer 2019

Undergraduate Students Advised in NSF POETS Research Projects

Yugo Isogai

- From University of Arkansas, ELEG Major
- POETS Project: QT-based GUI for PowerSynth Material Design Library (MDK) — Summer 2019

Undergraduate Honors Students Advised in the NSF PATH Program

Xavier Hendrix, William Matthews, Gehrett Thompson

- Served as the academic advisor — Fall 2018 – Spring 2019

Served on the Undergraduate Honors Thesis Committee

Cole Sherrill

- Thesis title: Optimization of Ultra-Low Power Application-Specific Asynchronous Deep Learning Integrated Circuit Design — 2019 Spring

Bentley Lager

- Thesis title: Dependency Mapping Software for Jira, Project Management Tool — 2020 Spring

Teaching Experience

Assistant Professor, University of Arkansas

CSCE 4013/5013: Design Automation of VLSI Circuits and Systems	Spring 2017
CSCE/ELEG 4914: Advanced Digital Design	Fall 2017
CSCE 2114: Digital Design	Spring 2018
CSCE 4013/5013: Design Automation of VLSI Circuits and Systems	Fall 2018
CSCE 2114: Digital Design	Spring 2019
CSCE/ELEG 4914/5914: Advanced Digital Design	Fall 2019
CSCE 4133/5133: Algorithms	Fall 2019
CSCE 4373/5373: Electronic Design Automation	Fall 2020

Graduate Teaching Assistant, Georgia Institute of Technology

ECE 2020 IE3: Fundamentals of Digital Design Fall 2016

- Sole instructor for giving lectures and guiding labs

ECE 6133: Physical Design Automation of VLSI Systems Spring 2016

- Head teaching assistant for grading homework, exams and guiding labs and projects
- Guest lecture on Steiner routing algorithm

Academic Activities

Served on the Organizing Committee

- 1st IEEE Design Automation for Power Electronics Workshop Sep. 2018
- 2nd IEEE Design Automation for Power Electronics Workshop Sep. 2019
- 1st IEEE Design Methodologies Conference July 2021

Served on the Technical Program Committee

- IEEE Computer Society Annual Symposium on VLSI July 2018
- IEEE International Conference on Computer Design Nov. 2019
- IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia May 2020
- IEEE International System-on-Chip Conference Sep. 2020
- IEEE Energy Conversion Congress and Exposition Oct. 2020

Served as the Reviewer

- ACM Design Automation Conference Since Nov. 2013
- IEEE International Conference on Electronics, Circuits, and Systems Since Aug.2015
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems Since Jan. 2015
- Elsevier Integration, the VLSI Journal Since Feb. 2017
- ACM Transactions on Design Automation of Electronic Systems Since July 2018
- IEEE Transactions on Power Electronics Since Sep. 2018
- MDPI Applied Sciences Since Feb. 2019
- ASME International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems Since Apr. 2019
- IEEE Transactions on Nanotechnology Since Apr. 2019
- MDPI Electronics Since Aug. 2019
- Elsevier Microelectronics Journal Since Nov. 2019
- IEEE Journal of Emerging and Selected Topics in Power Electronics Since Dec. 2019

- IEEE Power Electronics Magazine — Since May 2020
- MDPI Energies — Since Sep. 2020

Organized Tutorials

- "Wide Bandgap Power Electronics: A New Trend on Design Automation", IEEE Workshop on Wide Bandgap Power Devices and Applications — Sep. 2018

Invited Talks

- "Parasitic Extraction in F2F and F2B 3D ICs," Mentor Graphics, Fremont, CA — Aug. 2015
- "CAD Tools for Design, Analysis, and Optimization of Emerging Technologies in VLSI and Power Electronics", College of Electrical and Information Engineering, Hunan University, Changsha, China — Dec. 2017
- "CAD Tools for Design, Analysis, and Optimization of Emerging Technologies in VLSI and Power Electronics", School of Physics and Electronics, Hunan University, Changsha, China — Dec. 2017
- "CAD Tools for Design, Analysis, and Optimization of Emerging Technologies in VLSI and Power Electronics", School of Physical Science and Electronics, Central South University, Changsha, China — Jan. 2018
- "PowerSynth: A Layout Synthesis and Optimization Tool for Multi-Chip Power Modules", Huazhong University of Science and Technology, Wuhan, China — Dec. 2018
- "CAD Tools for Design, Analysis, and Optimization of Emerging Technologies in VLSI and Power Electronics", Changsha University of Science and Technology, Changsha, China — Jan. 2019
- "PowerSynth: A Layout Synthesis and Optimization Tool for Multi-Chip Power Modules", IEEE Design Automation for Power Electronics Workshop, Genova, Italy — Sep. 2019
- "Design Automation for 2.5D&3D Heterogeneous Integrated Circuits and Power Electronics", College of Computer Science and Electronic Engineering, Hunan University, Changsha, China — Jan. 2020

Honors and Awards

- New Faculty Commendation for Teaching Commitment — Sep. 2019
- EDAPS 2017 Best Symposium Paper Award — Dec. 2017
- ICPT 2016 Best Student Paper Award — Oct. 2016
- SRC TECHCON 2014 Best-in-Session Award — Sep. 2014
- Academic Excellence Scholarships at Tsinghua University — Oct. 2009, Oct. 2011
- Temask Foundation - Leadership Enrichment and Regional Networking Award — May 2011
- Chinese Universities Study Award — Mar. 2011
- First Place Award in the 26th National College Physics Competition: Non-Physics Students — Nov. 2009

Patents

- A Non-Volatile Memory Storage Unit — CN Patent No. ZL201210518687.9

Skills

Operating Systems:

- Windows, Linux, MacOS

Computer Languages:

- C/C++, VHDL/Verilog, Matlab, Tcl, Bash/Tcsh, Perl, Python, HTML, PHP, JavaScript

CAD Tools:

- Cadence: Innovus, Virtuoso, EPS, ELC, Spectre, NCVerilog, QRC, Allegro Package Designer
- Synopsys: Design Compiler, Primetime, VCS, Hspice, Raphael, StarRC
- Mentor Graphics: Calibre (nmDRC/nmLVS/xRC/xACT/xACT 3d/xL), Eldo, Olympus, HyperLynx, Xpedition
- Ansys: Fluent, HFSS, Q3D
- Others: Altium Designer, Altera Quartus, Keysight ADS